# A 100-Hz, 2nW RC Oscillator Using Resistance Amplifier

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***Abstract* — This paper introduces an ultra-low-power RC oscillator that utilizes a resistance amplification technique. The resistance amplifier achieves the effect of a large resistance by amplifying the I-V characteristics of a small resistance, resulting in significant area savings. To improve precision in oscillation frequency, a continuous time auto-zeroing technique is incorporated to dynamically calibrate the offset voltage of an integrated amplifier. Fabricated using a 180-nm CMOS process, the designed oscillator produces a 100-Hz clock signal while consuming only 2 nW power under compact silicon area (0.12 mm$^2$). Additionally, it achieves a competitive temperature coefficient (TC) of 280 ppm/$^o$C and line sensitivity (LS) of 1.1%/V without the need for any calibration.**

***Keywords — Low Power, CMOS, Auto-zeroing, Amplifier, RC Oscillator.***

## I. Introduction

Compact active sensors at the millimeter scale have garnered attention for applications in confined spaces, such as biomedical, biological, and security contexts. These sensors are strategically duty-cycled to minimize power consumption. Given that timers are continuously operational circuits, their power usage significantly influences the overall power scale of the system. Moreover, due to stringent form factor requirements, these timers cannot employ off-chip components like crystals. As a solution, RC oscillators have emerged as the preferred choice. They offer low power consumption and reliable frequency stability. Various RC oscillators, operating in the kHz range and consuming mere hundreds of nano-watts, have been proposed [1]-[4]. Nevertheless, further power reduction poses a challenge, as it necessitates impractically large areas of giga-ohm resistance in a miniature system. To address this issue, gate-leakage based relaxation oscillators have been suggested as an alternative to large resistors [5]-[6]. However, these face drawbacks, including susceptibility to high process and temperature and low cost IoT technologies like 180nm require extremely large devices to generate gate leakage in the order of 100's of pA.

This manuscript presents an ultra-low power, resistance-based relaxation oscillator employing novel resistance amplification technique that eliminates the need of large resistance. The proposed resistance amplifier creates an electrical equivalent of large resistance by amplifying the I-V characteristics of small resistance, therefore saving appreciable amount of area without compromising the accuracy of the oscillator. For enhancing precision in oscillation frequency, a continuous time auto-zeroing technique is implemented to dynamically calibrate the offset in resistance amplifier. The period of offset calibration depends on temperature sensitive switch leakage current, hence an off-switch leakage-based ring oscillator is designed to adapt the frequency of the auto-zeroing with temperature. Moreover, class AB comparator is used to reduce the effect of temperature sensitive rise/fall delay on the RC oscillation period. In 180nm CMOS, the 100Hz RC oscillator is designed under 2nW power, achieving 280ppm/$^o$C for temperature range of 0$^o$C to 70$^o$C and line sensitivity of 1.1 %/V for supply range of 1.3V to 2V. In comparison to state-of-the-art RC oscillators, it reduces power consumption by 2.9x [3] with a compact silicon area of 0.12 mm$^2$.

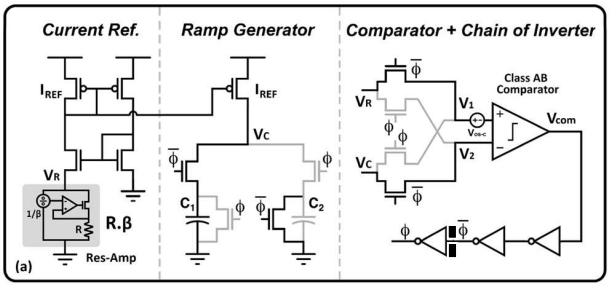
## II. Circuit Architecture and Design

### A. RC Oscillator Architrcture

Fig. 1 illustrates the circuit architecture of the proposed RC oscillator utilizing a resistance amplifier. In this setup, the amplified resistance (βR) generates a 330-pA $I_{REF}$ in a constant-$g_m$ circuit, and $I_{REF}$ drives an RC oscillator with comparator offset cancellation [2]. When Φ=0, $I_{REF}$ flows through $C_1$, charging $V_C$ until it exceeds voltage '$V_R$+$V_{os\text{-}c}$', where $V_{os\text{-}c}$ represents the comparator offset. Following a comparator delay ($t_d$), Φ shifts to 1, reversing the comparator inputs. This action connects $V_C$ to $C_2$ and discharges $C_1$. The same $I_{REF}$ then charges $V_C$ through $C_2$ until it surpasses the voltage '$V_R$–$V_{os\text{-}c}$'. The compensated comparison voltage effectively neutralizes the impact of the comparator offset on the total time period of oscillation (2RC + 2td). For the continuous comparator, we implemented a class-AB topology in a 2-stage op-amp design to minimize additional comparator delay ($2t_d$), which can be sensitive to process, voltage, and temperature (PVT) variations.

### B. Resistance Amplifier

Fig. 2 illustrates the circuit diagram of the proposed resistance amplifier with offset calibration. This circuit comprises a voltage divider with gain (β), a precision main op-amp, and a small on-chip resistor (R). The voltage divider divides the input voltage ($V_R$) by β, providing $V_R$/β to the main op-amp. The op-amp assigns $V_R$/β to R, generating $I_{REF}$



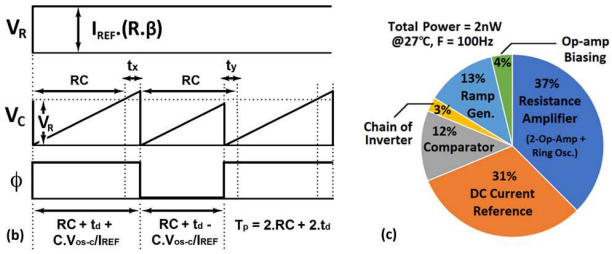
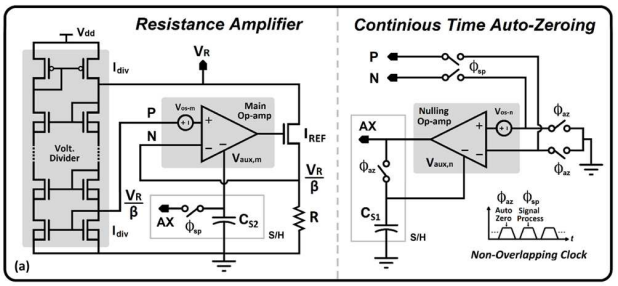




Fig. 1. (a) Circuit diagram of RC oscillator using resistance amplifier, (b) Timing diagram of RC oscillator, (c) Power breakdown.



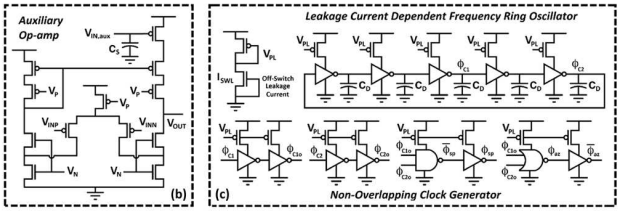
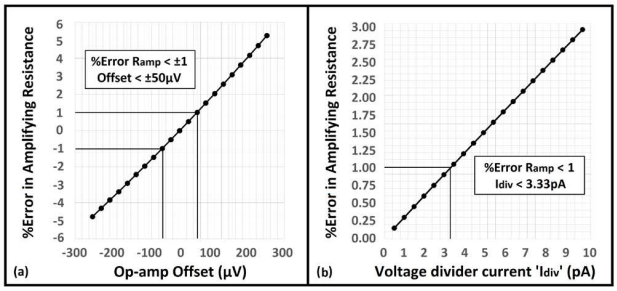




Fig. 2. (a) Resistance amplifier with CT auto-zeroing, (b) Auxiliary op-amps used in resistance amplifier for offset calibration, (c) Temperature dependent switch leakage ring oscillator with non-overlapping clock




## C. Circuit Specifications

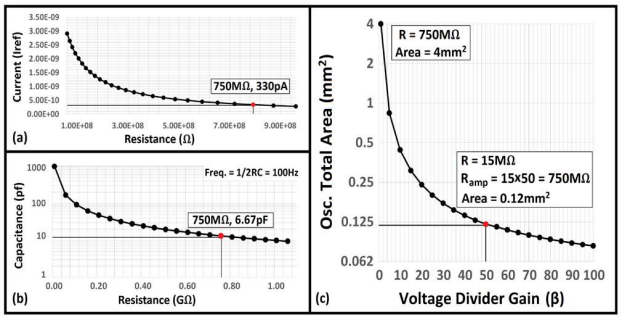



Fig. 4. (a) DC bias current vs Resistance, (b) Capacitance vs Resistance for 100Hz RC frequency, (c) Voltage divider gain (β) vs Total area of RC oscillator vs Voltage divider gain.

## III. Experimental Results

The proposed RC oscillator achieves a 100-Hz output clock signal with a power consumption of 2 nW at a 1.3 V supply voltage. Despite its low power consumption, the design incorporates an on-chip resistor of only 15 MΩ, and the entire oscillator occupies a silicon area of 0.12 mm². This footprint is approximately 33 times smaller than that of a conventional RC oscillator with a 750-MΩ resistor (4 mm², Fig. 4(c)), enabled by the innovative resistance amplification technique. In Fig. 5(a) and (b), the measured TC is 280 ppm/°C over a range of 0 °C to 70 °C, and the LS is 1.1 %/V across the voltage range from 1.3 V to 2 V. Fig. 5(c) depicts the measured oscillator frequencies from 10 different chips with and without the auto-zeroing technique. The auto-zeroing circuit effectively reduces output frequency variation from 260% to 2%. Table provides a performance comparison of the proposed RC oscillator with previously published low-power relaxation oscillators. It achieves a 2.9x reduction in power consumption, maintaining a compact silicon area of 0.12 mm². This is achieved without the need for calibration.

## IV. Conclusion

The paper presents an innovative ultra-low-power RC oscillator design. By employing a resistance amplification technique and continuous time auto-zeroing, the oscillator achieves significant area savings along with the precise oscillation frequency. Fabricated in 180-nm CMOS process, it generates a 100-Hz clock signal with minimal power consumption (2 nW) and occupies a compact silicon area (0.12 mm²). Additionally, it maintains the competitive temperature coefficient and line sensitivity without requiring calibration.

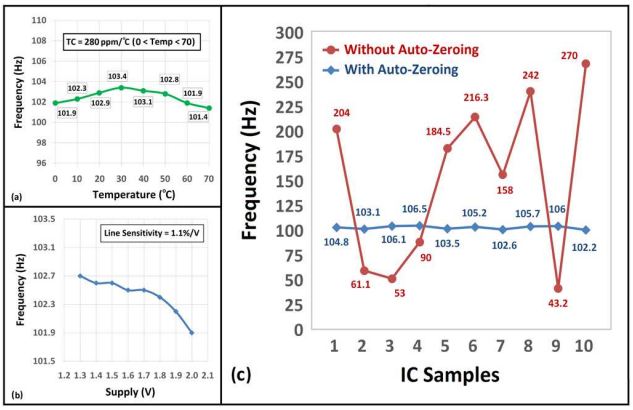



Fig. 5. Measured oscillator frequency with (a) Temperature, (b) Supply, (c) Different IC samples with and without auto-zeroing.

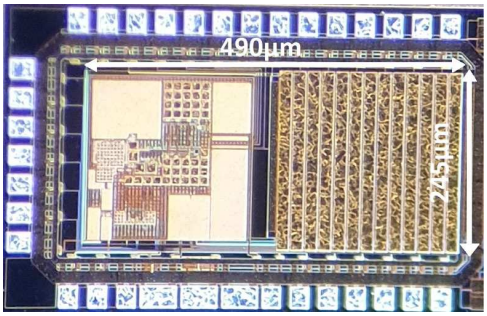



Fig. 6. Die Micrograph

Table I

| Specs | This Work | [1] | [2] | [3] | [4] | [1] | [5] | [6] |
|---|---|---|---|---|---|---|---|---|
| Publication year | – | JSSCC'16 | ISSCC'13 | JSSC'15 | TCAS-I'10 | JSSC'16 | CICC'07 | VLSI-C'18 |
| Oscillator type | RC | RC | RC | RC | RC | Gate-leak. | Gate-leak. | Gate-leak. |
| Technology (µm) | 0.18 | 0.25 | 0.065 | 0.18 | 0.35 | 0.065 | 0.13 | 0.055 |
| Freq (Hz) | 100 | 6400 | 18500 | 11 | 3300 | 2.8 | 9 | 90 |
| Temp. Range (°C) | 0 to 70 | -20 to 80 | -40 to 90 | -10 to 90 | -20 to 80 | -40 to 60 | 0 to 80 | -5 to 95 |
| Calibration | No | No | NA | NA | Multi-point | Yes | NA | Yes |
| TC (ppm/°C) | 280 | 148 | 77 | 45 | 500 | 2000 | 1600 | 1100 |
| Supply (V) | 1.3 - 2 | 0.6 - 0.9 | 1.5 - 3.3 | 1.2 - 2.2 | 1 - 3.5 | 0.48 – 0.52 | 0.4 - 0.5 | 1.2 - 3 |
| Power (nW) | 2 | 75.6 | 120 | 5.8 | 11 | 0.044 | 0.12 | 0.22 |
| LS (%/V) | 1.1 | 1.8 | 1 | 1 | 3.5 | 160 | 150 | 0.93 |
| Area (mm²) | 0.12 | 1.08 | 0.032 | 0.24 | 0.1 | 0.025 | 0.00048 | 0.057 |

Performance summary and comparison of low power, low frequency oscillators


## Acknowledgement

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