A Hybrid-Computing Solution to Nonlinear Optimization Problems

Kamlesh Sawant, *Graduate Student Member, IEEE*, Dillon Nguyen, *Member, IEEE*, Alex Liu, *Student Member, IEEE*, Jason Poon, *Member, IEEE*, and Sairaj Dhople, *Senior Member, IEEE*

***Abstract*— We put forth a hybrid-computing solution to a class of constrained nonlinear optimization problems involving nonlinear cost and linear constraints. This is accomplished by realizing gradient-flow dynamics for a reformulated penalty program with a combination of operational amplifiers, discrete linear and nonlinear circuit elements, and a digital microcontroller. Convergence of the voltages of the circuit to stationary points of the original mathematical optimization problem, as well as local asymptotic stability of the equilibria, are established analytically. Leveraging numerical tools catering to delayed differential equations, design strategies to ensure the circuit is parametrized to be robust to delays attributable to the digital microcontroller are presented. Hardware results for a representative problem involving minimizing selected harmonics from a pulse-width modulated waveform validate the analytical developments.**

***Index Terms*— Delayed differential equations, digital microcontroller, gradient flow, nonlinear circuits, nonlinear optimization.**

I. Introduction

HYBRID circuits are symbiotic combinations of analog and digital circuits operating in concert [1]. In this paper, we outline an architectural framework and companion analytical machinery to realize and benchmark a hybrid-computing solution to a class of constrained optimization problems involving nonlinear cost and linear constraints. Our proposed hybrid-computing solution is composed of a combination of operational amplifiers (op-amps), discrete linear and nonlinear circuit elements, and a digital microcontroller. The circuit realizes gradient-flow dynamics for a penalty-based reformulation of the original nonlinear optimization problem. (See Fig. 1.) Two primary contributions are offered to the state-of-the-art. First, we outline a constructive circuit-synthesis approach that systematically apportions digital and analog subsystems while establishing a direct correspondence of the realized hybrid-computing solution with the originating nonlinear optimization problem and its penalty-program reformulation. Second, we leverage a variety of system-theoretic constructs to benchmark performance relating to the convergence and stability of the proposed hybrid-computing solution. We also outline numerical methods to guide parametrization while ensuring robustness to delays that are uniquely debilitating in such applications.

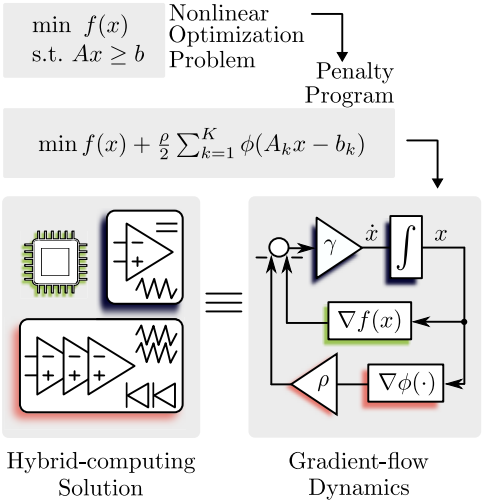

Fig. 1. A *Hybrid-computing Solution* is put forth for *Nonlinear Optimization Problems*. *Gradient-flow Dynamics* as a solution strategy for a reformulated *Penalty Program* are realized with a mix of analog and digital circuits.

Electronic analog computers used to be the mainstay in computing for a variety of engineering applications [1], [2], [3], [4]. Hybrid solutions were subsequently employed to address real-time control challenges in applications ranging from aircrafts to power systems [5], [6], [7], [8], [9], [10]. With advances in semiconductor technology driving unprecedented gains in digital computing, analog and hybrid computing fell out of vogue. That said, it can be argued for several emerging real-time technologies (e.g., edge computing, internet-of-things) that hybrid options featuring a combination of desirable attributes from analog (speed, low power consumption) and digital (programmability) domains serve better than the endpoints [11], [12], [13].

An overview of the proposed approach is outlined next, with Fig. 1 providing companion illustrative context. We begin

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Kamlesh Sawant and Sairaj Dhople are with the Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN 55455 USA (e-mail: sawan035@umn.edu; sdhople@umn.edu).

Dillon Nguyen, Alex Liu, and Jason Poon are with the Electrical Engineering Department, Cal Poly, San Luis Obispo, CA 93407 USA (e-mail: dnguy318@calpoly.edu; aliu150@calpoly.edu; jasonp@calpoly.edu).

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by translating the nonlinear optimization problem into an unconstrained penalty program with the aid of a suitable penalty function applied to the constraints. Following such a reformulation, continuous-time gradient-flow dynamics are adopted as a solution strategy for the penalty program. These dynamics are then realized with a combination of op-amps, discrete linear and nonlinear circuit elements, and a digital microcontroller. Some facets of the solution strategy and design choices outlined above deserve justification:

1) *Why the penalty-program reformulation?* Such a reformulation allows the application of a variety of solution techniques (e.g., the gradient-flow approach we adopt), even if these are natively designed to handle unconstrained problems.
2) *Are gradient-flow dynamics the only solution strategy?* Gradient-flow methods are a class of first-order solution methods (so named since they rely on first-order derivatives). Typically, first-order methods offer faster convergence compared to zeroth-order (i.e., derivative-free) methods (e.g., genetic algorithms) and less computational burden compared to second-order methods (e.g., Newton's method) [14].
3) *What motivates the particular decomposition into analog and digital circuits?* The architecture is engineered to emphasize analog elements for their computation speed. In this regard, we prioritize their utilization to realize iterative operations, piece-wise nonlinear functions, and constraints. The digital intervention generates gradients of the cost function that may involve nonlinear algebraic terms which are challenging to realize in analog.

With the approach presented above, we offer two key contributions at the intersection of disciplinary boundaries of linear and nonlinear circuit theory, numerical optimization methods, and linear and nonlinear control theory—all of which are key to engineering circuits and systems:

- *Generalized Architecture.* The outlined hybrid-computing solution is generalized and the class of optimization problems features prominently in a variety of engineering applications, including power systems, power electronics, artificial neural networks, and the process industry. The approach we adopt clearly demonstrates the need for appropriate digital inputs as well as the role of (non)linear analog circuit elements in realizing (non)linear mathematical operations and energy-storage elements in realizing dynamic elements in the gradient-flow dynamics.
- *Benchmarking Performance.* We comment on the correspondence of the equilibria of the hybrid circuit with optimizers of the nonlinear optimization problem and validate the local asymptotic stability of circuit solutions. Furthermore, we derive a lower bound on convergence time, which depends on the circuit and problem parameters. Finally, we outline strategies to counter delays (stemming from digital inputs) leveraging theory and methods from so-called delayed differential equations.

With regard to validation and applications, we pursue two directions. First, we present a running example adopted from [15] to outline our analytical and algorithmic developments in a tutorial and repeatable fashion. Second, we provide results from an experimental hardware prototype of a hybrid-computing solution to the selective harmonic minimization (SHM) problem. This problem involves minimizing harmonics in a pulse-width modulated switching waveform and is of interest in power-electronics circuits [16], [17], [18], [19], [20]. Its formulation involves a nonlinear cost function (with trigonometric terms stemming from Fourier-series coefficients) and linear constraints; therefore, it is of the general form our approach can handle. Due to the limitations on the speed of digital circuits, offline optimization is usually employed to solve SHM [21]. Our previous work introduced a hybrid circuit allowing real-time optimization, and demonstrated high speed and low power consumption [11], [12]. However, we neither put forth the requisite analytical machinery to discuss convergence and stability (particularly relevant due to computational delays and delays attributable to analog-to-digital (A/D) and digital-to-analog (D/A) conversions) nor did we recognize the fact that the solution was solving a penalty-program reformulation of the original problem with gradient-flow dynamics. We do both in the present effort and as the forthcoming discussion will reveal, the latter aspect is particularly relevant to accurately characterize solutions of the circuit in relation to the originating optimization problem.

To place our work in the context of the state of the art, it is necessary to narrow focus to the presently considered application, i.e., analog and hybrid circuits that have been proposed to seek the solution of constrained nonlinear optimization problems. In [22], [23], [24], [25], and [26], analog circuits without any dynamic elements are designed such that specific voltages (and/or currents) present solutions of the Karush-Kuhn-Tucker (KKT) conditions for constrained optimization problems. (KKT conditions are first-order necessary conditions, and seeking solutions to them is a reasonable approach to tackle problems with limited structure, e.g., convexity.) The guiding design philosophy in these approaches is to leverage the fact that circuits naturally settle into an equilibrium state that minimizes energy loss. Even though this class of circuits does not explicitly involve dynamic elements, the convergence of the solutions is affected by factors such as the op-amps' slew rates and parasitic capacitances. This observation appears to have prompted the deliberate introduction of capacitance to counteract parasitic elements and ensure stability [11], [12], [15], [27], [28]. (It is worth pointing out that [15] is inspired by [24], [29], [30].) However, while efforts in [11], [12], and [15] demonstrate solving the KKT conditions of the original nonlinear optimization problem, they did not establish that the dynamics of the proposed circuits were, in fact, solving a penalty-program reformulation of the original nonlinear optimization problem. Although reference to the connection between penalty methods and the circuit realization in [15] is made in [31], a detailed exploration of how exactly these circuits' dynamics align with the penalty program reformulation, and thereby satisfy the KKT conditions of the original problem, is less apparent. This distinction is relevant in context since the KKT points for the original problem, and those for the penalty program reformulation are not necessarily the same.

The contributions of this effort fill the gaps indicated in the literature surveyed above. They span the synthesis of a generalized system architecture to realize hybrid circuits for computation as well as the application of system-theoretic methods and numerical tools to benchmark performance. Overall, our work is aligned with a significant body of contemporary research that has focused on uncovering synergies between optimization problems and dynamical systems [32], [33], [34], [35], [36], [37], [38]. It is also worth pointing out that there remains persistent interest in synthesizing analog circuits to solve optimization problems for a variety of engineering applications [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51].

The remainder of this paper is organized as follows. Section II introduces the nonlinear optimization problem, its penalty-based reformulation, and gradient-flow dynamics as a solution strategy for the penalty program. The circuit-based realization for the gradient-flow dynamics is derived in Section III. Approaches for performance analysis, benchmarking the hybrid-computing solution, and parameter selection are in Section IV. Simulation and hardware results for the SHM problem are presented in Section V. The paper is concluded in Section VI with some directions for future work.

II. Nonlinear Optimization Problem, Penalty-Based Reformulation, and Gradient-Flow Solution Dynamics

This section introduces the general nonlinear optimization problem that is examined in the work. A reformulated penalty problem and gradient-flow dynamics targeting the solution of the penalty-based reformulation are presented subsequently.

A. Optimization Problem & Penalty-Based Reformulation

The general optimization problem we attempt to solve with the proposed circuit-based solution is presented below

$$\min_{x\in\mathbb{R}^N} \quad f(x) \tag{1a}$$

$$\text{s.t. } Ax \geq b. \tag{1b}$$

The optimization variables are collected in vector $x = [x_1, x_2, \ldots, x_N]^\top \in \mathbb{R}^N$, the nonlinear cost function is denoted $f : \mathbb{R}^N \to \mathbb{R}$, and we suppose K affine inequality constraints captured via $A \in \mathbb{R}^{K\times N}, b \in \mathbb{R}^K$. In what follows, we denote A_k to be the k^{th} row of A, $a_{k,\ell}$ to be the entry in the k^{th} row and ℓ^{th} column of A, and b_k to be the k^{th} entry of b. We assume $f(\cdot)$ is twice continuously differentiable, i.e., $f \in \mathcal{C}^2$. This is because we will leverage the gradient, $\nabla f(\cdot)$, in the synthesis of the gradient-flow dynamics. Furthermore, the Hessian, $\nabla^2 f(\cdot)$, features in a result on local asymptotic stability.

To illustrate all developments that follow, we consider a running example, *Example* 3, adopted from [15].

Running Example (i): Nonlinear Optimization Problem from [15]. Consider the optimization problem

$$\min_{x\in\mathbb{R}^2} \quad 0.4\ x_2 + x_1^2 + x_2^2 - x_1x_2 + \tfrac{1}{30}x_1^3 \tag{2a}$$

$$\text{s.t. } 0.5x_1 + x_2 \geq 0.5, \tag{2b}$$

$$x_1 + 0.5x_2 \geq 0.4, \tag{2c}$$

$$x_1, x_2 \geq 0. \tag{2d}$$

Note that it fits the template in (1) with

$$f(x) = 0.4\ x_2 + x_1^2 + x_2^2 - x_1x_2 + \tfrac{1}{30}x_1^3, \tag{3}$$

$$A = \begin{bmatrix} 0.5 & 1 \\ 1 & 0.5 \\ 1 & 0 \\ 0 & 1 \end{bmatrix}, \quad b = \begin{bmatrix} 0.5 \\ 0.4 \\ 0 \\ 0 \end{bmatrix}. \tag{4}$$

We revert to this example in Section II-B to establish continuous-time gradient-flow dynamics for its solution. ■

The first step in our proposed solution approach is to convert the constrained problem (1) into an unconstrained penalty program by penalizing infringements in the constraints via an augmented cost function that invokes a penalty function. Such a reformulation takes the form

$$\min_{x\in\mathbb{R}^N} f(x) + \frac{\rho}{2}\sum_{k=1}^{K}\phi(A_kx - b_k), \tag{5}$$

where $\phi : \mathbb{R} \to \mathbb{R}$ is a penalty function that is set up to minimize violations of the constraints, and $\rho \in \mathbb{R}_{>0}$ is a penalty parameter that prioritizes the extent to which such violations are penalized viz-à-viz the cost function. As with the cost function, the only structure we assume about the penalty function is continuous differentiability. To guarantee that constraints $A_kx \geq b_k$ are met $\forall k = 1, \ldots, K$, we must pick ρ such that

$$\frac{\rho}{2}\sum_{k=1}^{K}\phi(A_kx - b_k) \gg 0.$$

This would ensure that the penalty for any violations of $A_kx - b_k \geq 0$ is substantial relative to $f(x)$, compelling the solution strategy employed to solve (1) to satisfy $A_kx \geq b_k$, $\forall k = 1, \ldots, K$.

Without loss of generality, we adopt the following quadratic penalty function for all subsequent developments:

$$\phi(A_kx - b_k) = (\min(0, A_kx - b_k))^2. \tag{6}$$

The function $(\min(0, A_kx - b_k))^2$ returns zero as long as the k^{th} inequality constraint, $A_kx \geq b_k$, is satisfied; otherwise, it imposes a quadratic cost on $A_kx - b_k$. Several other choices for the penalty function are possible [14].

B. Gradient-Flow Dynamics

We consider the following gradient-flow dynamics targeting the solution of (5):

$$\frac{\mathrm{d}x}{\mathrm{d}t} = -\gamma\left(\nabla f(x) + \frac{\rho}{2}\sum_{k=1}^{K}\nabla\phi(A_kx - b_k)\right), \tag{7}$$

where $\gamma \in \mathbb{R}_{>0}$ is a constant (that is analogous to a step-size in discrete-time implementations), $\nabla f(x) \in \mathbb{R}^{N\times 1}$ is the gradient of the function $f(\cdot)$ given by

$$\nabla f(x) = \left[\tfrac{\partial f(x)}{\partial x_1}, \tfrac{\partial f(x)}{\partial x_2}, \ldots, \tfrac{\partial f(x)}{\partial x_N}\right]^\top,$$

and $\nabla\phi(A_k x - b_k) \in \mathbb{R}^{N\times 1}$ is the gradient of the penalty function. The box labeled *Gradient-flow Dynamics* in Fig. 1 illustrates a block-diagram representation of these dynamics. For the existence and uniqueness of solutions to (7), we require the cost function, f, and penalty function, ϕ, to be such that the vector field driving the gradient-flow dynamics is locally Lipschitz continuous [52].

In essence, (7) nudges the optimization variables to evolve in the direction of the steepest descent of the cost function in (5). Equilibria of the dynamics (7) coincide with stationary points of the optimization problem (5). Stationary points are the collection of all maxima, minima, and saddle points of an optimization problem, and they are referred to as KKT points, provided they satisfy additional regularity conditions. Since no assumptions are imposed on the structure of $f(\cdot)$, we cannot comment on the number of equilibria, whether they correspond to local/global minima in the context of (5), and/or their local/global stability in the context of dynamics (7). Note also that no claims are made at this stage about whether such equilibria are feasible in the sense of the original problem (1). With these qualifiers out of the way, the general thought process to formulating (7) is to target a stationary solution to (5); with the understanding that for high enough ρ, the solutions of (5) and (1) coincide. Further discussion on the nature of equilibria is reserved for Section IV-B.

For the choice of penalty function $\phi(\cdot)$ in (6), the corresponding gradient-flow dynamics in (7) are given by

$$\frac{\mathrm{d}x}{\mathrm{d}t} = -\gamma\Big(\nabla f(x) + \rho\sum_{k=1}^{K}\min(0,\, A_k x - b_k)A_k^\top\Big). \tag{8}$$

In what follows, we will periodically reference the dynamics element-wise. For the ℓ^{th} variable, x_ℓ, we get

$$\frac{\mathrm{d}x_\ell}{\mathrm{d}t} = -\gamma\Big(\frac{\partial f(x)}{\partial x_\ell} + \rho\sum_{k=1}^{K}\min(0,\, A_k x - b_k)a_{k,\ell}\Big), \tag{9}$$

where $a_{k,\ell}$ is the entry in the k^{th} row and ℓ^{th} column of A.

Running Example (ii): Gradient-flow Dynamics. The gradient-flow dynamics targeting the solution to (2) involve the following differential equations of the form (9):

$$\begin{aligned}\frac{\mathrm{d}x_1}{\mathrm{d}t} =& -\gamma\big(2x_1 - x_2 + \tfrac{1}{10}x_1^2 + \rho\big(0.5\min(0,\, 0.5\ x_1 + x_2 - 0.5)\\ &+ \min(0,\, x_1 + 0.5\ x_2 - 0.4) + \min(0,\, x_1)\big)\big), \qquad (10a)\\ \frac{\mathrm{d}x_2}{\mathrm{d}t} =& -\gamma\big(0.4 + 2x_2 - x_1 + \rho\big(\min(0,\, 0.5\ x_1 + x_2 - 0.5)\\ &+ 0.5\min(0,\, x_1 + 0.5\ x_2 - 0.4) + \min(0,\, x_2)\big)\big). \qquad (10b)\end{aligned}$$

These are readily obtained with the aid of the gradient of $f(x)$ from (3) given by

$$\nabla f(x) = [2x_1 - x_2 + \tfrac{1}{10}x_1^2,\, 0.4 + 2x_2 - x_1]^\top, \tag{11}$$

and A and b specified in (4). We will revert to this example subsequently in Section III with a circuit that realizes the above dynamics. ■

III. Circuit-Based Realization of Gradient-Flow Dynamics

In this section, we synthesize a circuit with dynamics that align with (8). Parametric equivalences between the dynamics and circuit elements are established to facilitate realization. Implementation details that are relevant to realizations in practice are also discussed.

A. Synthesis of Circuit

We wish to synthesize a hybrid circuit that presents voltages $v_1, v_2, \ldots, v_N$ which align with optimization variables $x_1, x_2, \ldots, x_N$ that have dynamics given in (8). Consider N capacitors, each with capacitance C_γ, with the ℓ^{th} capacitance sporting voltage, v_ℓ, and featuring $K+1$ current withdrawals, $i_\ell^k, k \in 0, \ldots, K$. We focus the remainder of the discussion around the ℓ^{th} capacitance. A sketch of an elemental portion of the overall hybrid circuit that can be utilized to contextualize the discussion is given in Fig. 2. The voltage across this capacitance, v_ℓ, has dynamics given by:

$$C_\gamma\frac{\mathrm{d}v_\ell}{\mathrm{d}t} = -\sum_{k=0}^{K} i_\ell^k. \tag{12}$$

Suppose i_ℓ^0 is the current resulting from applying voltage $\partial f(v)/\partial v_\ell$ across some resistance, R_γ, i.e.,

$$i_\ell^0 = \frac{1}{R_\gamma}\frac{\partial f(v)}{\partial v_\ell}. \tag{13}$$

The choice of subscript γ in C_γ and R_γ will soon be justified via the connection established with parameter γ in (8). The synthesis of the remainder of the current withdrawals, $i_\ell^k, k \in 1, \ldots, K$, is presented next. The discussion is tailored to some k^{th} current, i_ℓ^k, and we recommend digesting the presentation alongside Fig. 2. We begin by applying voltage $-(A_k v - b_k)$ to an op-amp-based circuit (composed of op-amps $\mathcal{O}_k^{R_\rho/R_\circ}$ and $\mathcal{O}_k^{\min}$ in Fig. 2) to generate the voltage

$$v_{\min}^k = \min\Big(0,\, \tfrac{R_\rho}{R_\circ}(A_k v - b_k)\Big). \tag{14}$$

As the terminology suggests, $\mathcal{O}_k^{R_\rho/R_\circ}$ realizes an inverting amplifier with gain $-R_\rho/R_\circ$, while $\mathcal{O}_k^{\min}$ realizes the $\min(\cdot,\cdot)$ function. The choice of subscript ρ in $R_\rho$will soon be justified via the connection established with parameter ρ in (8); on the other hand, $R_\circ$ is a nominal resistance that will be utilized across several amplifier stages. We then scale the voltage $v_{\min}^k$ (at the output of $\mathcal{O}_k^{\min}$) by gain $a_{k,\ell}$ with the aid of another inverting op-amp circuit involving op-amp $\mathcal{O}_k^{a_{k,\ell}}$. In particular, $\mathcal{O}_k^{a_{k,\ell}}$ realizes an inverting amplifier with gain

$$a_{k,\ell} = -\frac{R_{k,\ell}}{R_\circ}.$$

If $a_{k,\ell} > 0$, additional inverting stages will be needed. The current that results by applying the output of this latest manipulation across resistance, R_γ, constitutes i_ℓ^k. In particular,

$$\begin{aligned} i_\ell^k &= -\frac{1}{R_\gamma}v_{\min}^k\frac{R_{k,\ell}}{R_\circ}\\ &= -\frac{1}{R_\gamma}\min\Big(0,\, \tfrac{R_\rho}{R_\circ}(A_k v - b_k)\Big)\frac{R_{k,\ell}}{R_\circ}. \end{aligned} \tag{15}$$

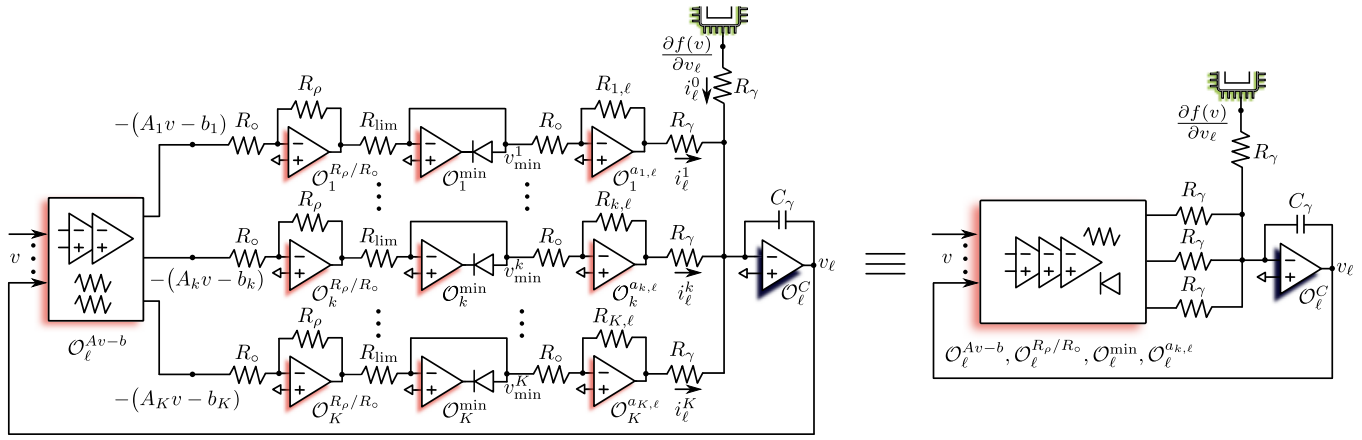


Fig. 2. Circuit realization (and shorthand) for the dynamics of the ℓ^{th} optimization variable. In particular, dynamics of voltage v_ℓ across capacitance C_γ coincide with the dynamics of optimization variable x_ℓ given in (9) for $R_\gamma C_\gamma = \gamma^{-1}$ and $R_\rho / R_\circ = \rho$.

Substituting all K instances of i_ℓ^k from (15) along with i_ℓ^0 from (13) in (12) yields:

$$C_\gamma \frac{\mathrm{d}v_\ell}{\mathrm{d}t} = -\frac{1}{R_\gamma}\Big(\frac{\partial f(v)}{\partial v_\ell} - \sum_{k=1}^{K} \min\Big(0, \tfrac{R_\rho}{R_\circ}(A_k v - b_k)\Big)\frac{R_{k,\ell}}{R_\circ}\Big). \tag{16}$$

Recognizing that

$$\min\Big(0, \tfrac{R_\rho}{R_\circ}(A_k v - b_k)\Big) = \frac{R_\rho}{R_\circ}\min\Big(0, A_k v - b_k\Big),$$

we can rewrite (16) as

$$\frac{\mathrm{d}v_\ell}{\mathrm{d}t} = -\frac{1}{R_\gamma C_\gamma}\Big(\frac{\partial f(v)}{\partial v_\ell} - \frac{R_\rho}{R_\circ}\sum_{k=1}^{K} \min\Big(0, A_k v - b_k\Big)\frac{R_{k,\ell}}{R_\circ}\Big). \tag{17}$$

Collecting all N instances of (17), we get the system-level dynamics for the interconnected circuit:

$$\frac{\mathrm{d}v}{\mathrm{d}t} = -\frac{1}{R_\gamma C_\gamma}\Big(\nabla f(v) + \frac{R_\rho}{R_\circ}\sum_{k=1}^{K} \min\Big(0, A_k v - b_k\Big)A_k^\top\Big). \tag{18}$$

Notice that the dynamics (18) can be placed in exact correspondence with (8) with the design choices:

$$R_\gamma C_\gamma = \frac{1}{\gamma}, \quad \frac{R_\rho}{R_\circ} = \rho. \tag{19}$$

The overall system architecture of the hybrid circuit is illustrated in Fig. 3, with constraints duplicated for clarity. It is obtained by stitching together multiple instances of the shorthand illustrated in Fig. 2. In summary, the dynamics of voltages v coincide with those of optimization variables x given in (8) with the design choices (19).

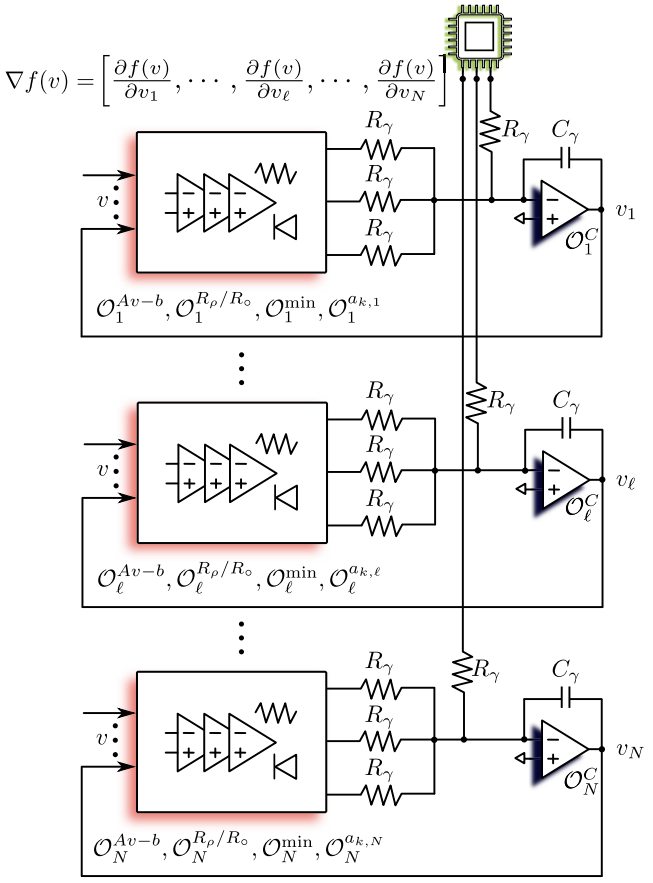


Fig. 3. System-level architecture of hybrid-computing solution. Op-amp circuits ($\mathcal{O}_\ell^{Av-b}$, $\mathcal{O}_\ell^{R_\rho/R_\circ}$, $\mathcal{O}_\ell^{\min}$, $\mathcal{O}_\ell^{a_{k,\ell}}$) are the shorthands in Fig. 2. Dynamics of the N voltages $v = [v_1, \ldots, v_\ell, \ldots, v_N]^\top$ coincide with those of optimization variables x in (8) with: $R_\gamma C_\gamma = \gamma^{-1}$ and $R_\rho / R_\circ = \rho$.

B. Implementation Details

The gradient terms $\partial f(v)/\partial v_\ell$ in the realization may be nonlinear functions of the voltages. (See, e.g., (11).) In principle, it is possible to realize a wide range of mathematical operations with analog circuitry. However, it is natural to leverage a digital microcontroller to generate these terms. Delays introduced by this digital intervention can compromise the stability of the overall system dynamics, and we devote special attention to this aspect in Section IV-C.

The circuit realization also invokes terms of the form $-(A_k v - b_k)$, which can readily be realized with inverting

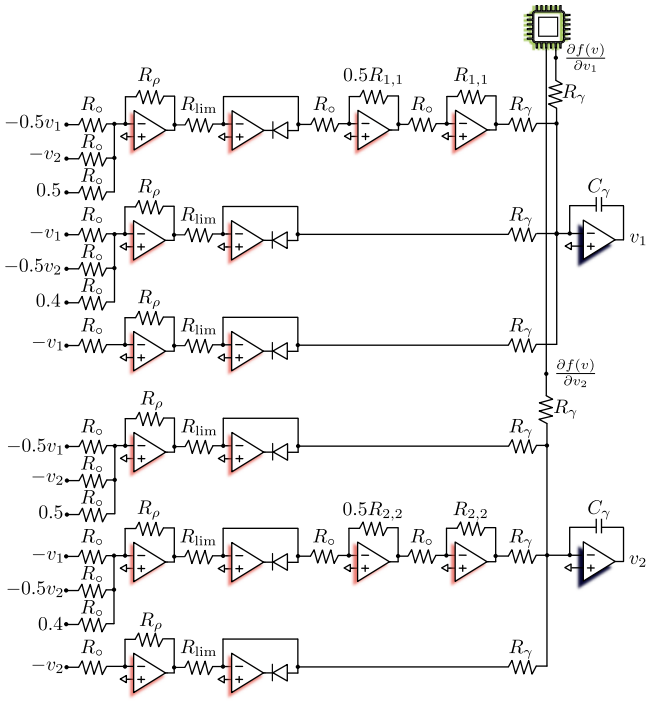


Fig. 4. Hybrid circuit that implements dynamics (18) built following the templates in Figs. 2 and 3. The circuit component values are $R_\circ = R_{\text{lim}} = R_{1,1} = R_{2,2} = R_\gamma = 10$ kΩ, $R_\rho = 1$ MΩ, and $C_\gamma = 100$ nF.

op-amp-based circuits since they involve linear manipulation of the voltages. These op-amp-based circuits are denoted by the shorthand $\mathcal{O}_\ell^{Av-b}$ in Fig. 2. Finally, resistances, R_{lim}, that appear in Fig. 2 limit the currents flowing through the output terminal of op-amps $\mathcal{O}_\ell^{\min}$ and associated diodes.

Evidently, the architecture is programmable to a degree. Gradient terms that arise from the digital microcontroller can be reprogrammed for different optimization problems. Digital potentiometers can be utilized to realize different coefficients for the constraint-related circuits built with op-amps.

With regard to choices of parameters, $R_\gamma, C_\gamma, R_\rho, R_\circ$, we recognize from the dynamics (18) that the rate of change of v is affected by $R_\gamma C_\gamma$. As the product $R_\gamma \times C_\gamma$ is reduced, we observe a faster transient response of the circuit to reach the equilibrium point. However, this cannot be indiscriminately decreased. In Section IV-C, we will find that in the presence of (unavoidable) delays due to the digital intervention discussed above, $R_\gamma \times C_\gamma$ should be selected considering both the convergence speed and stability. We also note that the ratio $R_\rho/R_\circ$ governs the enforcement of the constraints per the discussion in Section II-A. As the ratio $R_\rho/R_\circ$ is increased, we observe a stronger emphasis on satisfying constraints.

Running Example (iii): Circuit Realization. The hybrid circuit that realizes the dynamics (10) for the optimization problem introduced in *Running Example (i)* is in Fig. 4. ■

IV. Performance Analysis and Benchmarking Circuit-Based Realization

In this section, we comment on the nature and number of the equilibria of the dynamics of the hybrid circuit. We also explore stability under nominal conditions and in the face of delays that may creep in due to a digital interface computing the partial derivatives of the nonlinear cost function. We also offer some comments on parameter selection.

A. Equilibria of Circuit Dynamics

In this section, we examine the equilibria of (18) and comment on their relationship to the optimization problems we set out to solve. We also investigate the stability of the equilibria. All discussions are presented in the context of (18) and the circuit realization in Fig. 3; but they equally apply to the dynamics (8).

Setting the derivatives in (18) to zero, we see that the equilibria of (18), denoted $v^\star = [v_1^\star, \ldots, v_N^\star]^\top$, satisfy the nonlinear algebraic equations given by:

$$\nabla f(v^\star) + \frac{R_\rho}{R_\circ} \sum_{k=1}^{K} \min\Big(0, A_k v^\star - b_k\Big) A_k^\top = \mathbb{0}_N. \tag{20}$$

These are the KKT conditions for the optimization problem

$$\min_{v \in \mathbb{R}^N} f(v) + \frac{R_\rho}{R_\circ} \sum_{k=1}^{K} \Big(\min\Big(0, A_k v - b_k\Big)\Big)^2. \tag{21}$$

With the equivalence $v \equiv x$ and the design choice (19), we see that (21) is the same as (5) (assuming the choice of the quadratic penalty function (6)). Solutions to the KKT conditions are merely stationary points, and they are not necessarily optima of the corresponding optimization problem; therefore, in what follows, we refer to $v^\star$ as KKT points. Given the limited structural limitations we impose on $f(\cdot)$, it is circumspect not to expect KKT points to correspond to optima. Additionally, given the potentially nonlinear nature of $\nabla f(\cdot)$ and the complexity introduced by the terms $\min(\cdot,\cdot)$, it becomes challenging to definitively qualify the existence of or quantify the number of potential solutions to (20).

B. Relationship of Equilibria to Constrained Optimization Problem and Local Stability

Recall that the optimization problem we originally set out to solve was (1). With the equivalence $v \equiv x$, we restate this in terms of the circuit voltages as

$$\min_{v \in \mathbb{R}^N} \quad f(v) \tag{22a}$$

$$\text{s.t. } Av \geq b. \tag{22b}$$

We are interested in qualifying when (and whether) the KKT points $v^\star$ for the optimization problem (21) as characterized by the solution of (20) are also the KKT points for problem (22). To that end, we will find the definition of the *feasible set* useful:

$$\mathcal{F} = \{v \in \mathbb{R}^N : Av \geq b\}. \tag{23}$$

The boundary of $\mathcal{F}$ is denoted $\partial\mathcal{F}$. The result presented next establishes the correspondence of feasible equilibria of the circuit dynamics with the KKT conditions of the original nonlinear optimization problem.

Lemma 1: If an equilibrium point of the dynamics (18), $v^\star$, is feasible, i.e., $v^\star \in \mathcal{F}$, then it is a KKT point of the problem (22).

Proof: Since $v^\star$ is an equilibrium point of (18), we know it is the solution of (20), which, with the following definition

$$\lambda^\star_{\mathcal{L},k} = \frac{R_\rho}{R_\circ} \min\Big(0,\, A_k v^\star - b_k\Big), \tag{24}$$

can be rewritten as

$$\nabla f(v^\star) + \sum_{k=1}^{K} \lambda^\star_{\mathcal{L},k} A_k^\top = \mathbb{0}_N. \tag{25a}$$

Since $v^\star \in \mathcal{F}$ and with $\lambda^\star_{\mathcal{L},k}$ in (24), we also have

$$Av^\star \geq b, \tag{25b}$$

$$\lambda^\star_{\mathcal{L}} = [\lambda^\star_{\mathcal{L},1}, \ldots, \lambda^\star_{\mathcal{L},K}]^\top = \mathbb{0}_K. \tag{25c}$$

Finally, the combination of (25b) and (25c) yields

$$(Av^\star - b) \circ \lambda^\star_{\mathcal{L}} = \mathbb{0}_K, \tag{25d}$$

where $\circ$ denotes element-wise multiplication. The collection (25a), (25b), (25c), and (25d) are precisely the KKT conditions of (22), with $\lambda^\star_{\mathcal{L}}$ denoting the Lagrange multipliers. In particular, (25a) is the stationarity condition, (25b) captures primal feasibility, (25c) captures dual feasibility, and (25d) is the complementary slackness condition [53]. In sum, $v^\star$ is a KKT point of (22). □

The next result establishes local asymptotic stability of feasible equilibria.

Lemma 2: If an equilibrium point of the dynamics (18), $v^\star$, is feasible, i.e., $v^\star \in \mathcal{F}$, and $\nabla^2 f(v^\star) \succ 0$, then it is locally asymptotically stable.

Proof: The dynamics of $\Delta v = v - v^\star$ obtained by linearizing (18) around $v^\star$ are given by

$$\frac{\mathrm{d}\Delta v}{\mathrm{d}t} = -\frac{1}{R_\gamma C_\gamma} \nabla^2 f(v^\star) \Delta v. \tag{26}$$

In deriving the above, we have leveraged the fact that $v^\star \in \mathcal{F}$ which renders $\min(0, A_k v^\star - b_k) = 0$, $\forall k$. Since we assume $\nabla^2 f(v^\star) \succ 0$, we infer from (26) that the matrix $-\frac{1}{R_\gamma C_\gamma} \nabla^2 f(v^\star) \in \mathbb{R}^{N\times N}$ is Hurwitz, and therefore, $v^\star$ is locally asymptotically stable. □

The above results apply to the case where the equilibrium point of the dynamics (18) is assumed to be feasible, i.e., $v^\star \in \mathcal{F}$. The dynamics (18) do not innately guarantee this. However, if the set $\mathcal{F}$ is *positively invariant*—by which we mean that $v(t=0) \in \mathcal{F} \implies v(t) \in \mathcal{F}$, $\forall t \geq 0$—then it is possible to ensure $v^\star \in \mathcal{F}$ by engineering the initial condition to be feasible. If $v^\star \notin \partial\mathcal{F}$, one straightforward means to verify positive invariance is to check whether $\dot{v} \cdot \eta \leq 0$, for all $v \in \partial\mathcal{F}$ and vectors $\eta \in \mathbb{R}^N$ that are outward normal to $\mathcal{F}$. In our problem setting, this condition amounts to $\nabla f(v)^\top A^\top \leq \mathbb{0}_K^\top$, $\forall v \in \partial\mathcal{F}$.

The linearized dynamics (26) also affords us the opportunity to establish limits on time to converge to the optimal solution. The solution to (26) can be expressed as

$$\Delta v(t) = \mathrm{e}^{-\frac{1}{R_\gamma C_\gamma}\nabla^2 f(v^\star)t} \Delta v_\circ.$$

Applying the Euclidean norm on both sides and using the sub-multiplicative property of matrix norms,

$$\begin{aligned}\|\Delta v(t)\|_2 &= \|\mathrm{e}^{-\frac{1}{R_\gamma C_\gamma}\nabla^2 f(v^\star)t} \Delta v_\circ\|_2 \\ &\leq \|\mathrm{e}^{-\frac{1}{R_\gamma C_\gamma}\nabla^2 f(v^\star)t}\|_2 \|\Delta v_\circ\|_2.\end{aligned} \tag{27}$$

Define the convergence time, τ_c, to be the time taken for the voltage vector to be within $\epsilon > 0$ away from the optimal, i.e.,

$$\|\Delta v(\tau_\mathrm{c})\|_2 \leq \varepsilon.$$

To isolate τ_c, we consider the right-hand side of (27):

$$\|\mathrm{e}^{-\frac{1}{R_\gamma C_\gamma}\nabla^2 f(v^\star)\tau_\mathrm{c}}\|_2 \|v_\circ - v^\star\|_2 \leq \varepsilon. \tag{28}$$

Since we assume $\nabla^2 f(v^\star) \succ 0$, we obtain the eigendecomposition $\nabla^2 f(v^\star) = Q\Lambda Q^\top$, where Q is an orthogonal matrix and Λ is a diagonal matrix with non-negative eigenvalues. Using this eigendecomposition and the unitarily invariant norm property, we can write

$$\begin{aligned}\|\mathrm{e}^{-\frac{1}{R_\gamma C_\gamma}\nabla^2 f(v^\star)\tau_\mathrm{c}}\|_2 &= \|Q\mathrm{e}^{-\frac{1}{R_\gamma C_\gamma}\Lambda\tau_\mathrm{c}} Q^\top\|_2 = \|\mathrm{e}^{-\frac{1}{R_\gamma C_\gamma}\Lambda\tau_\mathrm{c}}\|_2 \\ &\leq \mathrm{e}^{-\frac{1}{R_\gamma C_\gamma}\lambda_{\min}(\nabla^2 f(v^\star))\tau_\mathrm{c}},\end{aligned} \tag{29}$$

where $\lambda_{\min}(\nabla^2 f(v^\star))$ denotes the smallest eigenvalue of $\nabla^2 f(v^\star)$. Utilizing the inequality from (29) in (28) and rearranging terms, we see that the convergence time is lower bounded as follows

$$\tau_\mathrm{c} \geq \frac{R_\gamma C_\gamma}{\lambda_{\min}(\nabla^2 f(v^\star))} \ln\left(\frac{\|v_\circ - v^\star\|_2}{\varepsilon}\right). \tag{30}$$

Equation (30) provides a lower bound on the convergence time to reach an ε-neighborhood of the optimal solution $v^\star$. We see that the convergence time depends on the product $R_\gamma C_\gamma$, the minimum eigenvalue of the Hessian matrix $\nabla^2 f(v^\star)$, $\lambda_{\min}(\nabla^2 f(v^\star))$, and the initial condition $v_\circ$ (specifically, the distance between the initial condition and the optimal solution, $\|v_\circ - v^\star\|_2$). This lower bound can guide the selection of circuit parameters R_γ, C_γ to achieve a desired convergence time, given properties of the optimization problem encoded within $\lambda_{\min}(\nabla^2 f(v^\star))$. It highlights, e.g., that problems with a shallow optimum (smaller $\lambda_{\min}$) will take longer to converge for a given $R_\gamma C_\gamma$.

Running Example (iv): Equilibria and Stability. Equilibria of the circuit in Fig. 4 are given by the solution of the following nonlinear algebraic equations

$$\begin{aligned}&2v_1^\star - v_2^\star + \tfrac{1}{10}(v_1^\star)^2 + \tfrac{R_\rho}{R_\circ}(0.5\min(0,\, 0.5\ v_1^\star + v_2^\star - 0.5) \\ &\quad + \min(0,\, v_1^\star + 0.5\ v_2^\star - 0.4) + \min(0,\, v_1^\star)) = 0,\end{aligned} \tag{31a}$$

$$\begin{aligned}&0.4 + 2v_2^\star - v_1^\star + \tfrac{R_\rho}{R_\circ}(\min(0,\, 0.5\ v_1^\star + v_2^\star - 0.5) \\ &\quad + 0.5\min(0,\, v_1^\star + 0.5\ v_2^\star - 0.4) + \min(0,\, v_2^\star)) = 0,\end{aligned} \tag{31b}$$

which are obtained by substituting $\nabla f(\cdot)$, A, and b from (11) and (4) in (20). These equations do not yield analytical closed-form solutions, however, we can attempt to obtain solutions numerically. For $R_\rho/R_\circ = 10^2$, we obtain a single solution: $(v_1^\star, v_2^\star) = (0.336, 0.325)$ that is very close to boundary $\partial\mathcal{F}$ and we deem feasible. The Hessian at $v^\star$ is

$$\nabla^2 f(v^\star) = \begin{bmatrix} 2 + \frac{1}{5}v_1^\star & -1 \\ -1 & 2 \end{bmatrix} = \begin{bmatrix} 2.067 & -1 \\ -1 & 2 \end{bmatrix}. \tag{32}$$

Evidently, $\nabla^2 f(v^\star) \succ 0$, which, given the result in Lemma 2, indicates $v^\star$ is locally asymptotically stable. Figure 5a illustrates contours of $f(\cdot)$ superimposed to vector fields of the dynamics (18) within and outside the feasible set, $\mathcal{F}$. Clearly,

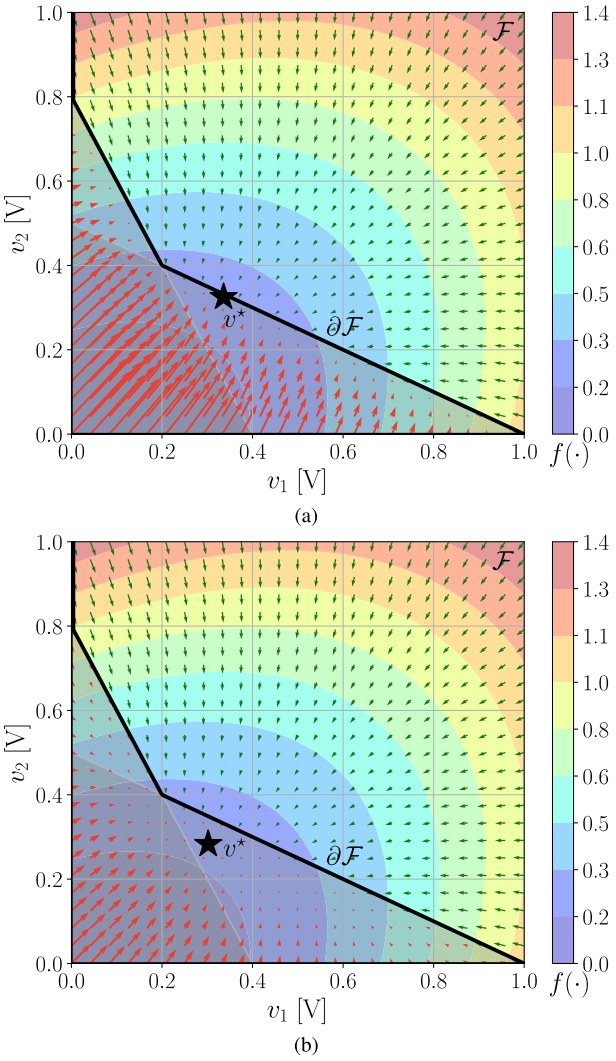


Fig. 5. Vector fields corresponding to dynamics (31) for: (a) $R_\rho/R_\circ = 10^2$ and (b) $R_\rho/R_\circ = 10$ superimposed to contours of $f(\cdot)$. Arrow lengths are rescaled for clarity; they are colored green within the feasible set (marked $\mathcal{F}$) and red outside (shaded gray and separated from $\mathcal{F}$ by boundary $\partial\mathcal{F}$). Optimal solution, $v^\star = (0.336, 0.325)$ for $R_\rho/R_\circ = 10^2$ and $v^\star = (0.302, 0.283)$ for $R_\rho/R_\circ = 10$. With higher $R_\rho/R_\circ$, there is more impetus provided to the dynamics to migrate into the feasible set.

we have a unique minimum, and the trajectories are engineered to drive the system to it. In Fig. 5b, we repeat the exercise, but with $R_\rho/R_\circ = 10$. In this case, we obtain a minimum outside the feasible set $\mathcal{F}$; evidently, the trajectories that originate from outside the feasible set do not receive as much of a nudge into it as before. This illustrates the impact of parameter ρ (congruently, $R_\rho/R_\circ$) on the circuit dynamics. ■

C. Impact of Delays

Taking particular care to annotate time parameterization, the circuit dynamics in question are given collectively by the ordinary differential equations (ODEs):

$$\frac{\mathrm{d}v(t)}{\mathrm{d}t} = -\frac{1}{R_\gamma C_\gamma}\Big(\nabla f(v(t)) + \frac{R_\rho}{R_\circ}\sum_{k=1}^{K}\min\Big(0,\, A_k v(t) - b_k\Big)A_k^\top\Big). \tag{33}$$

Per the discussion in Section III-B, we suppose the gradient $\nabla f(\cdot)$ in (33) is sourced from a digital microcontroller which presents a worst-case time delay of $\tau > 0$. This delay originates from analog-to-digital (A/D) and digital-to-analog (D/A) conversions and computation latency in the digital microcontroller [54]. The circuit dynamics with such a setup take the form

$$\frac{\mathrm{d}v(t)}{\mathrm{d}t} = -\frac{1}{R_\gamma C_\gamma}\Big(\nabla f(v(t-\tau)) + \frac{R_\rho}{R_\circ}\sum_{k=1}^{K}\min\Big(0,\, A_k v(t) - b_k\Big)A_k^\top\Big). \tag{34}$$

Dynamics of the form (34) are commonly called as delayed differential equations (DDEs) in the literature [55], [56], [57]. They present non-trivial complexities compared to ODEs; however, there is vibrant research in DDEs, with numerical toolboxes available for their analysis and simulation [58], [59].

We are particularly interested in the stability of (34) as a function of the delay, τ. To this end, one can linearize the dynamics around an equilibrium point and compute eigenvalues of the resultant linearized model to glean insights into local asymptotic stability. Denoting such an equilibrium point by $v^\star$, and assuming it to be feasible, i.e., $v^\star \in \mathcal{F}$, the eigenvalues, λ, are given by the solution of the characteristic equation:

$$\det\Big(\lambda\mathbb{I}_N + \tfrac{1}{R_\gamma C_\gamma}\mathrm{e}^{-\lambda\tau}\nabla^2 f(v^\star)\Big) = 0, \tag{35}$$

where $\det(\cdot)$ denotes the determinant and $\mathbb{I}_N$ is the $N \times N$ identity matrix. An important clarifying remark is in order. Without the delay, the characteristic equation is given by

$$\det\Big(\lambda\mathbb{I}_N + \tfrac{1}{R_\gamma C_\gamma}\nabla^2 f(v^\star)\Big) = 0,$$

and we are assured $\lambda \in \mathbb{C}^N$. However, depending on the problem setup and parameters, (35) may offer infinitely many solutions to λ.

To improve the transient response of the realized hybrid circuit, it is important to tune the product $R_\gamma \times C_\gamma$. Decreasing $R_\gamma \times C_\gamma$ makes the transient response faster. However, it is crucial to ensure that the eigenspectrum of the circuit has all eigenvalues lying strictly on the left-hand side of the complex plane for the circuit to remain stable. If $R_\gamma \times C_\gamma$ is set too low for a fast transient response, the eigenvalues might move to the right half of the complex plane, causing the circuit to become unstable.

Running Example (v): Stability with Delays. Substituting $\nabla^2 f(v^\star)$ from (32) in (35) we get:

$$\det\left(\begin{bmatrix}\lambda & 0\\ 0 & \lambda\end{bmatrix} + \tfrac{1}{R_\gamma C_\gamma}\mathrm{e}^{-\lambda\tau}\begin{bmatrix}2+\frac{1}{5}v_1^\star & -1\\ -1 & 2\end{bmatrix}\right) = 0,$$

which evaluates to the nonlinear algebraic equation:

$$\Big(\tfrac{1}{R_\gamma C_\gamma}\mathrm{e}^{-\lambda\tau}\Big(2+\tfrac{1}{5}v_1^\star\Big)+\lambda\Big)\Big(\tfrac{2}{R_\gamma C_\gamma}\mathrm{e}^{-\lambda\tau}+\lambda\Big) - \Big(\tfrac{1}{R_\gamma C_\gamma}\mathrm{e}^{-\lambda\tau}\Big)^2 = 0.$$

The above equation is solved numerically for λ within the `DDE-BIFTOOL` MATLAB package, which facilitates numerical bifurcation and stability analysis of DDEs [59].

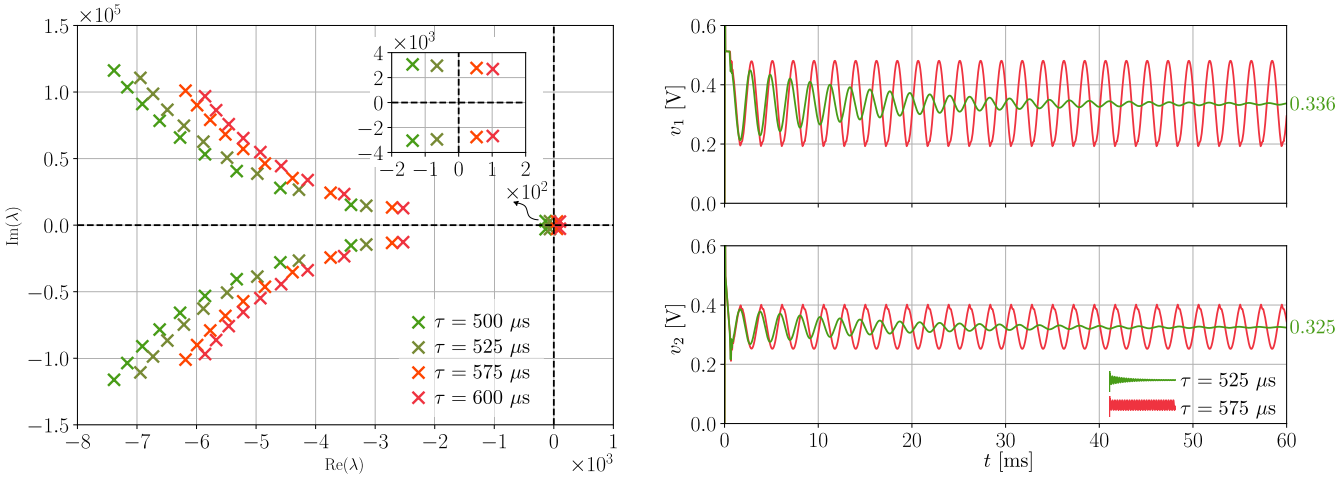


Fig. 6. (Left) Eigenspectrum of the dynamics for the hybrid circuit in Fig. 4 for different delays τ computed following the discussion in *Running Example (v)*. (Right) Time-domain simulations from PSpice for two delays, $\tau = 525$ μs (stable, and settles to the optimal) and $\tau = 575$ μs (oscillatory) are aligned with the instability suggested by the eigenspectrum. Steady-state values from PSpice simulations for the stable case match those computed numerically and reported in *Running Example (iv)*. Initial conditions are $(v_1, v_2) = (0\text{ V}, 0\text{ V})$.

Figure 6 (Left) plots the eigenvalues for different delays, τ. For delays less than or equal to 550 μs, all eigenvalues remain in the left half of the complex plane, implying stable dynamics. This is confirmed by the time-domain trajectories in Fig. 6 (Right), which plots voltage trajectories for two different delays, one verified to be stable ($\tau = 525$ μs) and one unstable ($\tau = 575$ μs) per the analysis. ■

D. Selection of Circuit Parameters

Three key circuit parameters featured in the dynamics (34), $R_\gamma, C_\gamma, R_\rho$, have to be designed. Note that $R_\circ$ appears as a ratio and merely establishes a baseline for normalization. First, we dwell on the design of parameters R_γ, C_γ (equivalently, hyperparameter γ). Our approach involves determining the Hopf bifurcation point attributable to tuning the parameter $\gamma = (R_\gamma C_\gamma)^{-1}$. This can be accomplished using the `DDE-BIFTOOL` in MATLAB, given the known delay τ introduced by the digital circuit. Hopf bifurcation happens when a pair of complex conjugate eigenvalues crosses the imaginary axis, causing oscillatory behavior [52], [60]. We solve (34) numerically using `DDE-BIFTOOL` to determine the critical value of γ_c at which Hopf bifurcation occurs for the given delay τ [61]. Note that the penalty term $\rho = \frac{R_\rho}{R_\circ}$, which enforces constraint satisfaction, does not affect the Hopf bifurcation point at the equilibrium point $v^\star$ when the constraints are satisfied. It suffices to select parameters R_γ, C_γ such that $\gamma < \gamma_c$ to guarantee stability in the face of delays.

Next, we comment on the design of the penalty parameter ρ. Several options may be considered [62], [63], [64], one that we pursue is to tune this via frequency-domain analysis. Since the penalty method requires high gain for constraint enforcement, the natural impulse is to go with a high value of ρ. However, this can have detrimental impacts on the gain and phase margins of pertinent transfer functions. A natural set of transfer functions to consider is the ones from the nodes in the circuit, which establishes the constraints (nodes with voltage $-(A_k v - b_k)$ in Fig. 2) to the optimization variables (nodes with voltage v_ℓ in Fig. 2). Such analysis can readily be performed in circuit simulation software such as PSpice.

Running Example (vi): Selection of Circuit Parameters. The simulation results for determining the Hopf bifurcation point and selecting γ are as shown in Fig. 7a. The critical value $\gamma_c = 1000\ \text{s}^{-1}$ at which the Hopf bifurcation occurs corresponds to a critical value of capacitance $C_{\gamma_c} = 100$ nF for $R_\gamma = 10$ kΩ. Any value of $\gamma < \gamma_c$ ($C_\gamma > C_{\gamma_c}$) ensures stability by keeping the eigenvalues in the left-half of the complex plane up to a maximum delay of 550 μs.

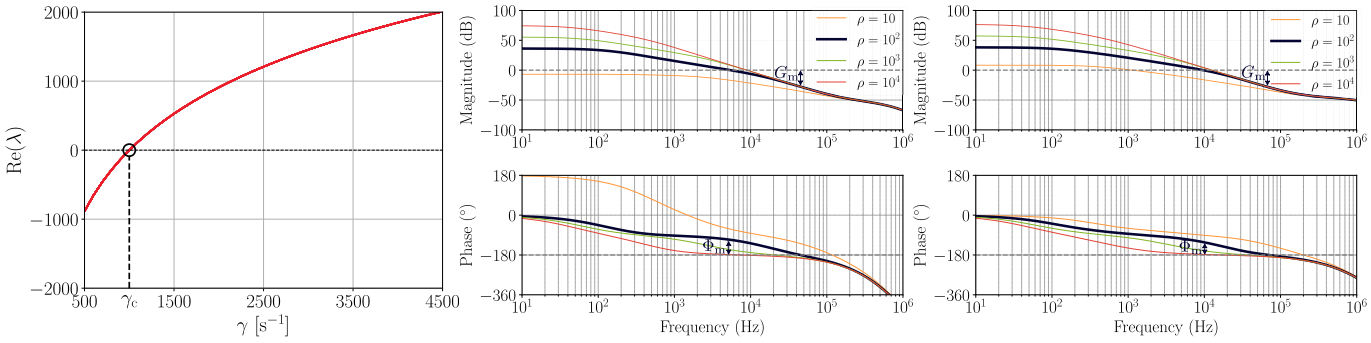
The simulation results containing Bode plots of the transfer function from the constraint $-(0.5\,v_1 + v_2 - 0.5)$ (at the boundary of which the optimal solution lies) to the optimization variable v_1 and v_2 for selecting ρ are as illustrated in Figs. 7b and 7c. Note that of the four constraints, we pick the one on which the solution lies to consider a worst case. The choice $\rho = 10^2$ gives a phase margin of approximately 68° and a gain margin of 27 dB for v_1, and a phase margin of roughly 58° and a gain margin of 29 dB for v_2. This frequency domain analysis uses a loop-at-a-time approach, which ensures stability if each loop independently shows good margins. ■

V. Validation: Selective Harmonic Minimization

In this section, we provide simulation results and experimental results from a hardware prototype of a hybrid-computing solution to the selective harmonic minimization (SHM) problem. As discussed in Section I, this problem, in general, aspires to minimize an a priori-specified number of harmonics from a pulse width modulated (PWM) waveform (of relevance in power electronics circuits [65], [66]). We begin with an overview of the problem, then present results from a hardware prototype, and finally, we conclude with simulation results that investigate scalability.

A. Optimization Problem

To introduce ideas, we examine the specific case of minimizing the third harmonic in a quarter-wave symmetric PWM



(a) (b) v_1 (c) v_2

Fig. 7. (a) Bifurcation diagram showing the trajectory of the real part of the eigenvalue closest to the imaginary axis as a function of the parameter, γ, for the *Running Example* with a delay $\tau = 550$ μs, obtained using `DDE-BIFTOOL` in MATLAB. Hopf bifurcation occurs at the critical value, $\gamma_c = 1000$ s^{-1}; this corresponds to a critical value of capacitance $C_{\gamma_c} = 100$ nF for $R_\gamma = 10$ kΩ. (b), (c) Bode plots of the transfer function from the circuit node corresponding to constraint $-(0.5\ v_1 + v_2 - 0.5)$ to the optimization variables v_1, v_2, using PSpice simulation with LM324 op-amp model for various ρ values. The value of $\rho = 10^2$ is selected based on the gain and phase margins denoted by G_m and Φ_m, respectively.

waveform with two switching angles while fixing the amplitude of the fundamental frequency. Consider such a waveform, $\sigma(\omega t)$, with switching angles denoted x_1, x_2, and the amplitude of the fundamental frequency denoted μ. Figure 8 provides an illustration for the case. The Fourier-series expansion of $\sigma(\omega t)$ is given by

$$\sigma(\omega t) = \sum_{n \text{ odd}} \frac{4}{n\pi} \left(1 + 2\left(\cos(nx_2) - \cos(nx_1)\right)\right) \sin(n\omega t).$$

By construction (see Fig. 8), we require

$$x_1 \geq 0,\ \ x_2 \geq x_1,\ \ x_2 \leq \tfrac{\pi}{2}. \tag{36}$$

Enforcing the amplitude of the fundamental frequency to μ $(0 < \mu < 1)$ requires satisfying

$$\mu = 1 + 2\left(\cos(x_2) - \cos(x_1)\right). \tag{37}$$

Minimizing the third harmonic requires minimizing the function

$$1 + 2\left(\cos(3x_2) - \cos(3x_1)\right). \tag{38}$$

Problem objectives discussed in (36)–(38) can be combined into the single optimization problem below (which fits the template established in (1)):

$$\begin{aligned} \min_{x_1, x_2} \quad & (1 + 2(\cos(x_2) - \cos(x_1)) - \mu)^2 \\ & + (1 + 2(\cos(3x_2) - \cos(3x_1)))^2 && \text{(39a)} \\ \text{s.t.} \quad & x_1 \geq 0, && \text{(39b)} \\ & x_2 - x_1 \geq 0, && \text{(39c)} \\ & -x_2 \geq -\frac{\pi}{2}. && \text{(39d)} \end{aligned}$$

The generalized form of this SHM optimization problem, which aims to minimize up to the N^{th} harmonic is: [66]

$$\begin{aligned} \min_{x \in \mathbb{R}^{N+1}} f(x) = & \left(1 + 2\sum_{i=1}^{N+1} (-1)^i \cos(x_i) - \mu\right)^2 \\ & + \sum_{n=3,5,7\ldots}^{2N+1} \left(1 + 2\sum_{i=1}^{N+1} (-1)^i \cos(nx_i)\right)^2 \end{aligned} \tag{40a}$$

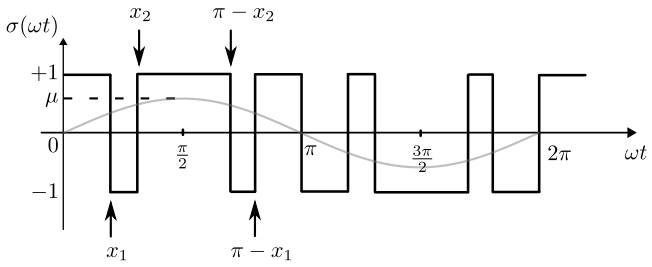


Fig. 8. Quarter-wave symmetric PWM waveform, $\sigma(\omega t)$, with two switching angles, x_1, x_2, and amplitude of the fundamental frequency, μ.

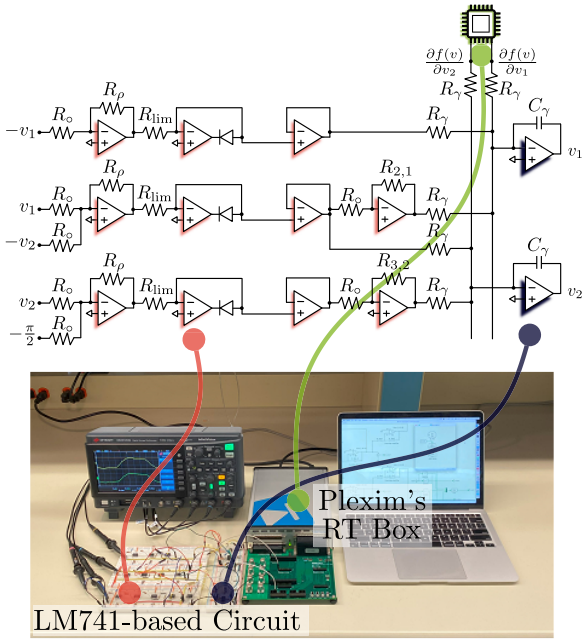
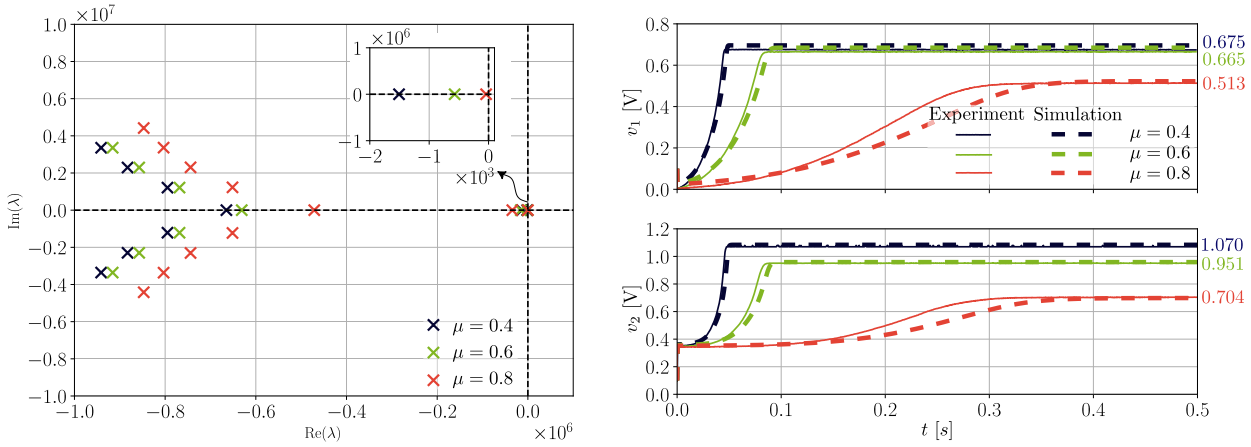


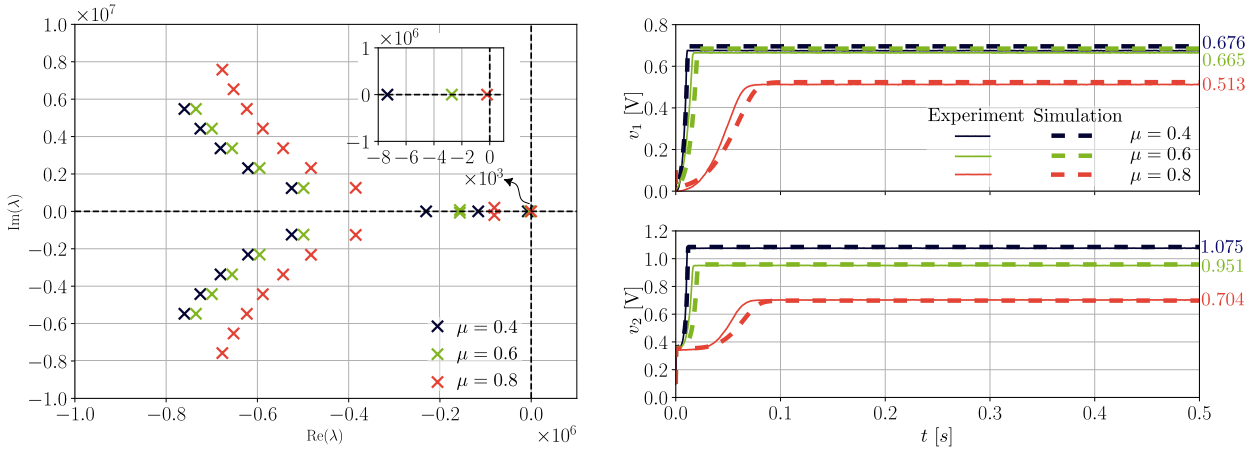
Fig. 9. (Top) The circuit schematic to solve the SHM problem (39). The circuit component values are $R_\circ = R_{\text{lim}} = R_{2,1} = R_{3,2} = R_\gamma = 10$ kΩ, $R_\rho = 10$ MΩ, and $C_\gamma = 100$ nF. (Bottom) Picture of the hardware setup highlighting Plexim's RT Box (that realizes the digital portion of the hybrid-computing solution) and the LM741-based analog circuit.

$$\text{s.t. } 0 \leq x_1 \leq x_2 \leq \cdots \leq x_{N+1} \leq \frac{\pi}{2} \tag{40b}$$

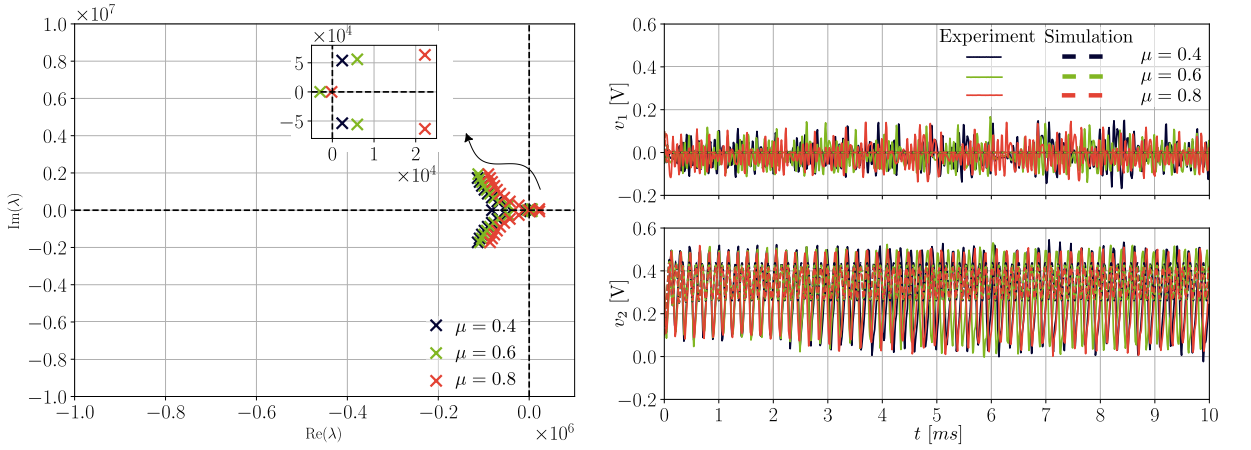
In this generalized formulation, the optimization variables are collected in the vector $x = [x_1, x_2, \ldots, x_{N+1}]^\top \in \mathbb{R}^{N+1}$. Recall that x_i represents the i^{th} switching angle. The cost



(a) $C = 470$ nF and $\tau = 6$ μs



(b) $C = 100$ nF and $\tau = 6$ μs



(c) $C = 100$ nF and $\tau = 30$ μs

Fig. 10. Eigenspectrum (left) and comparison of LTspice and experimental waveforms (right) for the hybrid computing solution with varying μ. Initial conditions are $(v_1, v_2) = (0.1\text{ V}, 0.1\text{ V})$ in all cases.

function, $f(x)$, now includes the minimization of multiple harmonics up to the N^{th} harmonic.

B. Hardware Prototype: Minimizing the 3rd Harmonic

A schematic of the hardware prototype of the hybrid circuit intended to solve (39) is illustrated in the top portion of Fig. 9. The gradient of the objective function is computed using Plexim's RT Box CE [67]. This choice is merely to facilitate rapid prototyping with different values of delay and is not representative of a low-cost digital microcontroller that can be leveraged for such an application. (In our prior work that focused on demonstrating low power consumption and fast convergence, we utilized the TI Delphino F28379D [12].) The constraint and integrator circuits are realized with LM741 op-amps. We also insert unity-gain op-amp circuits at the output of op-amps implementing the $\min(\cdot,\cdot)$ function to ensure

TABLE I
COMPARISON OF OPTIMA FOR VARYING μ, DETERMINED USING FMINCON IN MATLAB COMPARED WITH HYBRID-CIRCUIT SIMULATION IN LTSPICE

μ	fmincon		LTspice	
	$x_1^\star$ [rad]	$x_2^\star$ [rad]	$v_1^\star$ [V]	$v_2^\star$ [V]
0.4	0.696	1.084	0.696	1.084
0.6	0.685	0.959	0.685	0.959
0.8	0.524	0.698	0.523	0.698

adequate buffering [12], [15]. To ensure all op-amps operate within the linear regime, even when dealing with high penalty values for starting points outside the feasible region, we utilize ± 15 V supply rails.

Plots in Fig. 10 show the eigenspectrum for three different values of μ; 0.4, 0.6, and 0.8, as well as corresponding time-domain waveforms collected from LTspice and the experimental prototype for three cases: (a) $C_\gamma = 470$ nF, $\tau = 6$ μs, (b) $C_\gamma = 100$ nF, $\tau = 6$ μs, and (c) $C_\gamma = 100$ nF, $\tau = 30$ μs. As with *Running Example (v)*, the eigenspectrum is obtained via DDE-BIFTOOL in MATLAB [59]. We can make the following inferences:

- Reducing C_γ for a fixed τ makes the response faster (compare Figs. 10(a) and (b)). Increasing τ for a fixed C_γ pushes the eigenvalues into the complex right-half plane (compare Figs. 10(b) and (c)). Both simulations and experiments feature oscillatory behavior in such a setting.
- Steady-state values of the LTspice simulations for both stable cases (i.e., Figs. 10(a)-(b)) are the same, and all reported in Table I. (This is to be expected since the equilibria of dynamics (18) are independent of C_γ.) The steady-state values match numerically computed optima obtained via MATLAB's fmincon function, also reported in Table I.
- Slight variations aside (to be expected with uncertainty in estimating precise values of τ applied using the RT Box), trajectories from the physical hybrid circuit align with the LTspice waveforms (particularly well in steady state; steady-state values from the hardware realization are reported alongside the trajectories in Figs. 10(a)-(c)).
- Even for the same values of R_γ, C_γ, and starting from the same initial conditions, we get different rates of convergence with different problem parameters μ. This is consistent with the theoretical convergence time τ_c bound in (30), which depends on the minimum eigenvalue $\lambda_{\min}$ of the Hessian matrix $\nabla^2 f(v^\star)$. For $\mu = 0.4$, 0.6, and 0.8, we computed $\lambda_{\min}$ to be approximately 7.1, 2.7, and 0.2, respectively. The larger $\lambda_{\min}$ for smaller μ values aligns with the faster convergence observed in experiments. This highlights the influence of the problem parameters on the convergence time, even when circuit parameters are fixed.

C. Simulation Study: Minimizing up to N^{th} Harmonic

Figure 11 depicts the generalized circuit realization that can tackle the problem in (40) to minimize N harmonics with $N+1$ switching angles as optimization variables. Figure 12

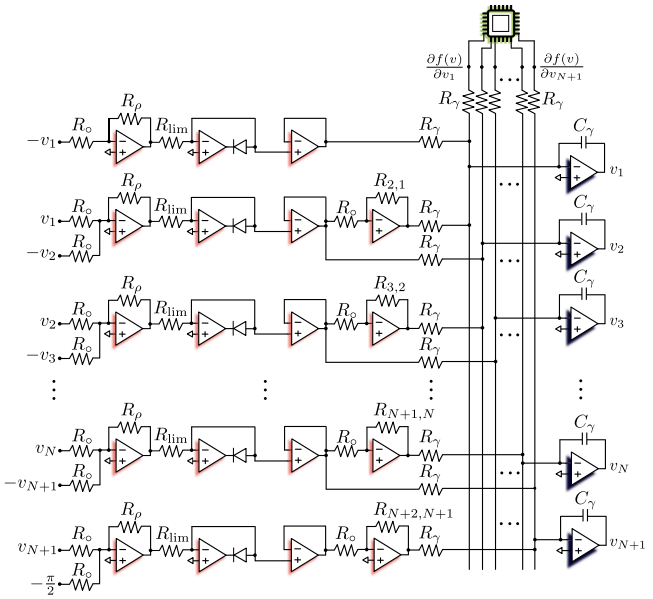


Fig. 11. Circuit schematic for the generalized SHM problem. The circuit parameters are $R_\gamma = 10$ kΩ, $C_\gamma = 100$ nF ($\gamma = 1000$ s^{-1}) and $R_\gamma = 10$ kΩ, $C_\gamma = 470$ nF ($\gamma = 213$ s^{-1}), $R_\rho = 10$ MΩ, and $R_\circ = R_{\lim} = R_{k,\ell} = 10$ kΩ.

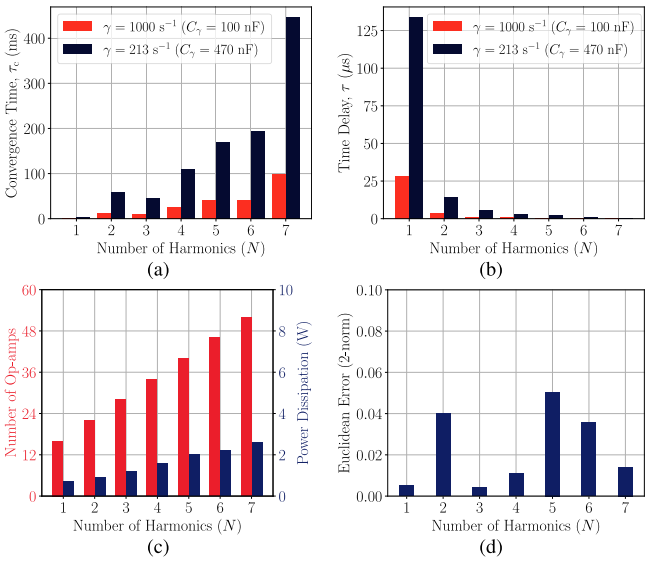


Fig. 12. Key performance indicators and attributes of the hybrid computing solution for SHM as a function of the number of harmonics minimized, N, for modulation index, $\mu = 0.9$: (a) convergence time, τ_c, with initial conditions identically set to zero in all cases (b) permissible digital-subsystem delay, τ, (c) required number of op-amps and associated power dissipation, and (d) error in solutions compared to MATLAB's fmincon function.

depicts a variety of performance indicators and attributes as a function of N, the total number of harmonics that are minimized, based on simulations performed in LTspice. Figure 12a shows convergence time for two different choices of $\gamma = (R_\gamma C_\gamma)^{-1}$. The two choices of γ are the same as the ones utilized in the experimental prototype in Section V-B. The results illustrate that the higher value of N typically leads to a longer convergence time for both choices of γ. As illustrated in Fig. 12b, the circuit exhibits a diminishing tolerance for delays τ introduced by the digital subsystem as the number of optimization variables increases. The maximum bound on

τ required to maintain the stability of the output switching angles (i.e., the optimization variables) was determined using the delay function in LTspice simulations. While these two trends are exponential, we recognize scalability in terms of the required number of op-amps and power dissipation, both of which grow linearly with N as indicated in Fig. 12c. The power dissipation analysis was performed using the Universal OpAmp2 model in LTspice with a power supply voltage of ± 15 V. It is worth noting that the power dissipation is a function of the supply voltage and op-amp parameters, and the reported values are specific to the chosen voltage level and op-amp model. Finally, Fig. 12d indicates that the hybrid computing solution achieves switching angles that closely approximate those determined by `fmincon` (implementing an interior-point algorithm) in MATLAB. The 2-norm of the error between the two solutions is no more than 5% across the board, validating the accuracy of the proposed hybrid computing solution for real-time applications.

VI. Concluding Remarks & Future Work

This article presented a hybrid-computing solution for solving constrained nonlinear optimization problems. By combining operational amplifiers, discrete linear and nonlinear circuit elements, and a digital microcontroller, we demonstrated the construction of a hybrid circuit that realizes gradient-flow dynamics for a penalty-based reformulation of the original optimization problem. Analytical results established the correspondence of the circuit's equilibrium voltages with the stationary points of the nonlinear optimization problem and the local asymptotic stability of these equilibria. We also analyzed the stability of the circuit when time delays representing the digital microcontroller were introduced. This analysis is crucial for real-time applications where any delay in the implementation of the gradient of the objective function (whether analog or digital) can significantly impact the stability of the circuit. The performance of this hybrid circuit was validated with hardware experiments focusing on minimizing the third harmonic from a pulse-width modulated waveform.

Future work includes investigating the stability of such hybrid circuits in conjunction with the physical plant(s) they are intended to operate alongside, benchmarking speed and performance (e.g., energy efficiency) alongside digital solutions in a systematic manner, as well as developing customized solutions for real-time applications pertaining to power electronics (which is what prompted our forays into this area). Putting forth circuit synthesis approaches and corresponding analytical machinery for other problems, e.g., non-convex problems and multi-objective problems, can also be pursued.

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