Digitally-Augmented Wideband Self-Interference Cancellation In Full-Duplex Transceiver

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***Abstract*—This paper presents a novel digitally-augmented analog self-interference (SI) cancellation (DASIC) scheme in a full-duplex transceiver, supporting simultaneous transmission and reception. A linear behavioral model is designed to characterize and reconstruct a multipath SI propagation channel in the digital domain. An auxiliary transmit chain is deployed to transmit the reconstructed signal and perform analog SI cancellation at the low-noise amplifier (LNA) input. The cancellation algorithm is developed on a Zynq Ultrascale+ RFSoC FPGA evaluation kit as part of the experimental hardware testbed. Extensive measurements demonstrate up to 38 dB cancellation of the TX passband leakage signal. This provides an improved wideband analog SI cancellation performance for a cancellation bandwidth of 400 MHz. To the best of the author's knowledge, this is the first-ever hardware realization of a digitally-augmented analog cancellation of such wide bandwidth.**

***Index Terms*—Full-duplex, self-interference cancellation, 5G, direct-RF sampling, RFSoC, FPGA, wideband OFDM**

I. Introduction

In-band full-duplex (IBFD) can double the spectral efficiency by simultaneously transmitting and receiving at the same band [1]. Hence, FD technology is of great interest in building the fifth-generation (5G) and beyond wireless communication systems. However, a major challenge in FD communication is the strong self-interference (SI) of the transmitter signal leaking to its own receiver.

The SI can be typically >100-120 dB stronger than the desired signal from a remote transmitter [2], thus, desensitizing the receiver. There are three main cancellation stages: 1) propagation (*stage-1*), 1) RF/analog (*stage-2* + *stage-3*), and 3) digital (*stage-4*). Analog SI cancellation (ASIC) at multiple stages along the transceiver chain is necessary to relax the receiver linearity requirement and selectivity performance. ASIC can be mainly categorized into two major approaches: (a) radio frequency (RF)-tapping approach [3], [4], where dedicated RF circuits with tunable RF components are used to reconstruct the leakage signal from a coupled transmitted signal, and (b) baseband (BB)-tapping approach [5], [6]. For the latter, a BB equivalent model of the leakage channel is reconstructed in the digital back-end using digital preprocessing of the known transmit data.

In this paper, a digitally-augmented analog SI cancellation (DASIC) solution is proposed to enhance the cancellation performance of traditional analog cancellers. An auxiliary (aux) transmitter chain is employed to capture the characteristics of the main Tx chain and accurately reconstruct the SI signal. Unlike traditional FD systems with external RF evaluation boards, the proposed architecture employs digital-to-analog (DAC) and analog-to-digital converters (ADC) that operate at giga samples per second. This method reduces the number of RF/analog components in the radio chain and hence the contribution of hardware impairments to the leakage signal. An experimental testbed is designed with a class-AB nonlinear power amplifier driven by 5G modulated waveforms, 400 MHz in bandwidth. The test results validate the superior cancellation performance of the proposed technique for such wideband signals.

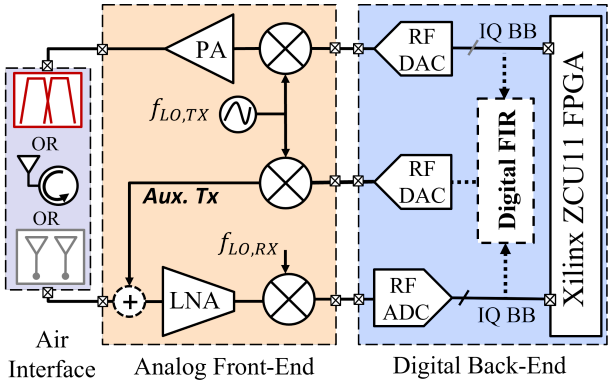

Fig. 1. Simplified block diagram of a typical full-duplex transceiver with different SI cancellation stages.

II. Proposed SI Cancellation Architecture

The system diagram of the proposed cancellation architecture is shown in Fig.1. Unlike conventional analog cancellers [3], [4], a linear baseband (BB) model and a direct-RF auxiliary Tx chain (shown in dashed box) are introduced to extract the transmitter behavior. The recreated model is inserted into the auxiliary Tx chain to generate the RF canceling signal $\hat{y}_{\mathrm{SI}}^{\mathrm{BB}}[n]$ from BB samples $x_{\mathrm{Tx}}^{\mathrm{BB}}[n]$. Digital cancellation of the transmitter leakage signal is broken down into two major stages, SI signal modeling and SI cancellation. The following subsections illustrate each of these stages.

A. SI Channel Modeling and Reconstruction

The signal at the local transmitter output is transmitted through the multi-path channel. This channel can be expressed

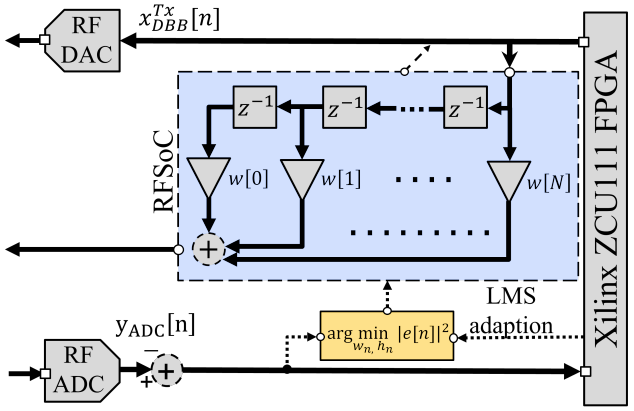

Fig. 2. Block diagram of the FIR filter structure implemented on XCZU28DR chip of the ZCU111 evaluation board.

TABLE I
FILTER PARAMETERS USED IN THE SIMULATION

Component	Specifications
Structure	Linear FIR
No. of taps (N_{tap})	64
Algorithm	LMS
Step-size (μ)	0.8
No. of samples (L)	130k

as $h_{SI}(t) = \sum_{m=1}^{M} h_m \delta(t - \tau_m)$, where h_m represents the channel gain and $\delta(t - \tau_m)$ is the unit impulse response with propagation delay τ_m. The transmitted signal eventually becomes the leakage signal and is expressed as

$$y_{\mathrm{SI}}^{\mathrm{RF}}(t) = y_{\mathrm{Tx}}^{\mathrm{RF}}(t) * h_{SI}(t) = \sum_{m=1}^{M} h_m y_{\mathrm{Tx}}^{\mathrm{RF}}(t - \tau_m) \quad (1)$$

The channel response $h_{SI}(t)$ can be estimated using M-order finite impulse response (FIR) filter. The filter parameters used in this work is mentioned in Table 1. From the above, the reconstructed SI signal model can be expressed as:

$$\hat{y}_{\mathrm{SI}}^{\mathrm{BB}}[n] = \sum_{m=1}^{M} \hat{h_m} x_{\mathrm{Tx}}^{\mathrm{BB}}[n - M] \quad (2)$$

where $\hat{y}_{\mathrm{SI}}^{\mathrm{BB}}[n]$ represents the reconstructed linear SI component, $x_{\mathrm{Tx}}^{\mathrm{BB}}[n]$ is the transmitted baseband samples, and $\hat{h}_m$ contains the estimated SI channel coefficient vector $\hat{h}_m = [h[0]\ h[1]\ ...\ h[M-1]]^T$. A Least-square (LS) algorithm can be used for coefficient estimation after collecting a block of N samples. The linear models can be expressed as:

$$\mathbf{y} = \mathbf{X}\mathbf{\Omega}, \quad (3)$$

$$\mathbf{y} = \big[y[0], y[1], ..., y[N-1]\big]^T, \quad (4)$$

$$\mathbf{\Omega} = [w_0, w_1, ..., w_{N-1}] \quad (5)$$

By applying the LS algorithm, the coefficients can be calculated from:

$$\hat{\mathbf{\Omega}} = (\mathbf{X}^H \mathbf{X})^{-1} \mathbf{X}^H \mathbf{y} \quad (6)$$

where $(.)^H$ is the Hermitian transpose, $\boldsymbol{X} \in \mathbb{C}^{N \times M}$

B. Tracking Multipath Components

To track changes in the SI channel due to reflections from the FD device itself, and its surroundings, an adaptive least mean square (LMS)-based learning algorithm is used to extract the FIR filter coefficients. First, the digitally estimated SI signal $\hat{y}_{\mathrm{SI}}^{\mathrm{BB}}[n]$ is transmitted through the auxiliary Tx chain as shown in Fig.2 to generate the RF canceling signal $\hat{y}_{\mathrm{SI}}^{\mathrm{BB}}(t)$. The output of the canceler is given by:

$$e[n] = y_{\mathrm{SI}}^{\mathrm{RF}}[n] - \hat{y}_{\mathrm{SI}}^{\mathrm{BB}}[n] \quad (7)$$

where $y_{\mathrm{SI}}^{\mathrm{RF}}[n]$ is the original SI and $\hat{y}_{\mathrm{SI}}^{\mathrm{BB}}[n]$ is the estimated SI. Notably, the error signal is obtained by subtracting the reconstructed SI from the leakage signal. Eventually, the objective for the error signal is to approach zero, i.e., $e[n] = 0$, provided that the SI channel parameters h_m are accurately estimated. In the LMS algorithm, the filter coefficients are updated using the basic gradient descent solution where the parameters are adjusted towards the negative gradient of a cost function. The cost function to be minimized can be defined as:

$$J(h_m) = e[n]e^*[n] \quad (8)$$

The filter coefficient update rule becomes

$$h_{m+1} = h_m - \mu \frac{\partial J(h_m)}{\partial h_m} = h_m + \mu e^*[n] x_{\mathrm{Tx}}^{\mathrm{BB}}[n] \quad (9)$$

where μ is the step size of the learning rate. The following section provides the measurement testbed details to verify the performance of the proposed architecture.

III. EXPERIMENTAL TESTBED AND RESULTS

The measurement setup to evaluate the performance of the proposed system is presented in Fig.3. A testbed of two transmitters and one receiver is employed. The FD was fully implemented into a Zynq UltraScale+ XCZU28DR RFSoC FPGA using the Xilinx ZCU111 Characterization Kit [8]. Xilinx's adaptable RFSoC platforms provide the flexibility for rapid prototyping of radio solutions with the same hardware resources. The RFSoC chip integrates 8x14-bit RF-sampling digital-to-analog converters (RF-DACs) with 6.554 Gsps and 8x12-bit analog-to-digital converters (RF-ADCs) with 4.096 Gsps sampling rates, and a programmable logic (PL). The on-board RF phase-locked loops (PLLs) provide the sampling clock for the DACs and ADCs. The major components on the RFSoC chip are summarized in Table 2.

The only analog components are the RF power amplifier (PA), a circulator, and a low-noise amplifier (LNA). The signal processing tasks, including baseband waveform synthesis, up/down-conversion, and filtering are performed at the digital front-end. A local host computer is connected to the evaluation board using a high data rate Ethernet cable for programming the FPGA with the generated bitstream. The synthesized waveform samples are then passed through Multi-Gigabit transceivers (MGTs). The MGT was connected to XM500 add-on daughter card to access the RF-DACs/ADCs. A PA (ZRL-2400LN+) from Mini-Circuits is connected directly to the output of the DAC.

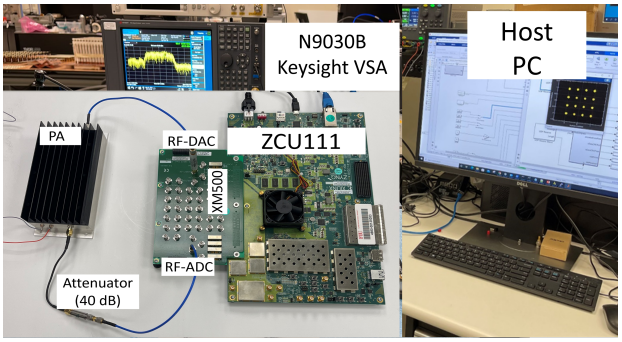

Fig. 3. Measurement setup showing (1) RFSoC-FPGA as the direct-RF transceiver with (2) PA, LNA, and circulator as the analog components, (3) Host PC for controlling the RFSoC, and (4) Keysight N9030B vector signal analyzer

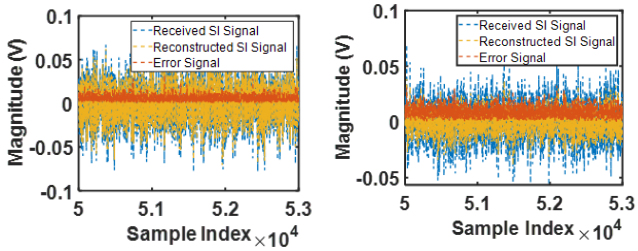

Fig. 4. Comparing the time-domain waveforms between the leakage signal (in blue) and the reconstructed SI signal (in yellow). The difference between the two gives the error signal (in red). Two different measurement cases (a) 200 MHz and (b) 400 MHz in bandwidths show NMSE values of -88.0285 dB and -88.024 dB.

TABLE II
FPGA FABRIC CONTENTS OF ZCU111 XCZU28DR CHIP

Component	Amount
RF-ADC (12-bit, 4.096 GSPS)	8
RF-DAC (14-bit, 6.554 GSPS)	8
System Logic Cells	930k
Transceivers (33 Gbps)	16
Maximum I/O pins	371
Memory	60.5 Mb
DSP slices	4,272

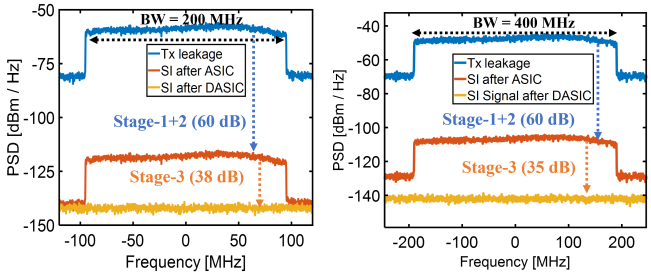

Fig. 5. Power spectral density (PSD) of two different measurement bandwidths (a) 200 MHz and (b) 400 MHz showing leaked transmitter signal, received SI signal after analog cancellation (ASIC), and SI signal after proposed cancellation method (DASIC).

The transmitter (Tx) and receiver (Rx) are connected through a 40 dB attenuator to mimic RF/analog passive suppression. The transmitted digital BB samples and the received SI samples are captured using the data acquisition setup shown in Fig.3. The processing is done offline to reduce computational complexity and flexibility. For proof-of-concept, the proposed architecture is tested with 5G new-radio (NR) OFDM signals with a maximum bandwidth of 400 MHz. The OFDM waveform consists of 1200 subcarriers with a subcarrier spacing of 15 KHz and an FFT size of 2048.

To quantify the quality of the estimated SI, we computed normalized mean square error (NMSE) in dB using:

$$NMSE_{\text{dB}} = 10log_{10}\left[\frac{\sum_{n=1}^{M}|\hat{y}_{\text{SI}}^{\text{BB}}[n] - y_{\text{SI}}^{\text{ADC}}[n]|^2}{\sum_{n=1}^{M}|y_{\text{SI}}^{\text{ADC}}[n]|^2}\right] \quad (10)$$

In the above, $\hat{y}_{\text{SI}}^{\text{BB}}[n]$ represents the reconstructed SI signal samples, and $y_{\text{SI}}^{\text{ADC}}[n]$ is the received SI signal samples, and M refers to the number of samples used to calculate the NMSE values. For an evaluation bandwidth of 200 MHz, we achieved an NMSE of -88.0285 dB which slightly deteriorated to -85.0245 dB for the 400 MHz case, as shown in the time-domain plots in Fig.4. The obtained values show the superior estimation capability of the DASIC method.

To evaluate the cancellation performance, the SI cancellation ratio (SICR) is used as a figure of merit and can be expressed as:

$$SICR_{dB} = 10log_{10}\left[\frac{\sum_{n=1}^{M}|y_{\text{SI}}^{\text{ADC}}[n]|^2}{\sum_{n=1}^{M}|y_{\text{SI}}^{\text{ADC}}[n] - \hat{y}_{\text{SI}}^{\text{BB}}[n]|^2}\right] \quad (11)$$

The cancellation performance of the proposed method was evaluated in terms of power spectral density (PSD) as shown in Fig.5. Two different bandwidths of 200 MHz and 400 MHz are used as test cases to demonstrate compatibility with 5G and beyond cellular networks. Notably, a SICR of 38 dB is achieved with the DASIC architecture for the 200 MHz bandwidth. As the modulation bandwidth increases to 400 MHz, there is a little degradation in the cancellation performance resulting in 35 dB of analog SI cancellation. It was observed that the auxiliary Tx chain introduced extra noise to the local receiver. This is a new barrier to achieving further SI cancellation.

IV. CONCLUSION

A digitally-augmented analog cancellation architecture was presented in this paper. The efficacy of the proposed method was experimentally validated by a measurement testbed with wideband modulated waveforms. Experimental results demonstrated superior cancellation of the proposed architecture over the traditional cancellation approaches. Analog SI cancellation of 38 dB is achieved for a cancellation bandwidth of 400 MHz. To the best of our knowledge, this is the first time that such high SI cancellation is experimentally demonstrated in a full-duplex radio for such wideband operation. This architecture provides feasibility to realize practical wideband full-duplex radios for 5G and beyond cellular communication applications.

V. Acknowledgement

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