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High-Performance TiO_2 Thin-Film Transistors: In-Depth Investigation of the Correlation between Interface Traps and Oxygen Vacancies

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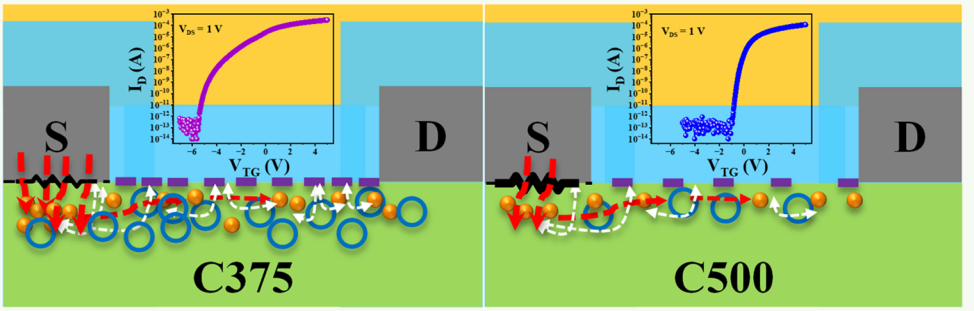

ABSTRACT: The role of surface contamination, along with surface oxygen vacancies, plays a key role in the overall carrier transport in thin-film transistors (TFTs). In this study, it is shown that the quality of the semiconductor/dielectric interface and the surface roughness of the channel can be improved by O_2 annealing of the TiO_2 channel and subsequent N_2O treatment. It has been observed that the surface contamination related to carbonaceous compounds by O_2 annealing at 500 °C (sample C500) is substantially reduced by 61% in comparison to that annealed at 375 °C (sample C375), which leads to a reduction of interface state traps (D_{it}) at the channel/dielectric interface. TFTs with a higher O_2 annealing temperature (C500) exhibit an SS of 88 mV/dec, an I_{ON}/I_{OFF} of ~10^9, and a mobility μ_{FE} of 1.5 cm^2/V-s under a battery-powered voltage of 1 V. In contrast, the sample C375 results in greater donor states such as surface oxygen vacancies (V_os), and the transistors exhibit a mobility μ_{FE} of 2.95 cm^2/V-s and an I_{ON}/I_{OFF} of ~10^9, despite a degradation of the SS value (123 mV/dec) due to the large number of interface states. Therefore, to fabricate high-performance devices, it is possible to tune the optimum values of surface contamination and oxygen vacancies by adjusting the O_2 annealing temperature. Also, these TFTs show excellent stability under both negative bias stress (NBS) and positive gate bias stress (PBS) in the dark as well as with laser illumination with minimal modifications of the electrical characteristics upon both gate stresses up to 1800 s, suggesting the feasibility of our TiO_2 TFTs for practical applications. A low gate leakage and I_{OFF} current, as well as high-performance electrical characteristics, make the ICs ideal for low-power internet of things (IoT) applications.

KEYWORDS: *wide-bandgap semiconductor, oxide electronics, TiO_2, TFT, interface state*

1. INTRODUCTION

The growing popularity of the internet of things (IoT) has led to increased demand for portable electronic devices. Consequently, there is a significant push to develop high-quality thin-film transistors (TFTs) capable of low-power operation. This is particularly important for emerging technologies such as foldable screens and wearable sensors. Among various devices, metal-oxide thin-film transistors (TFTs) have been receiving considerable attention in the field of electronics due to their superior properties over silicon-based TFTs. These properties include high optical transparency, impressive carrier mobility, excellent uniformity, and simpler production processes. High-performance metal-oxide TFTs, utilizing channel materials such as InGaZnO, SiInZnO, ZnSnO, SiZnSnO, InZnO, and In_2O_3, have demonstrated remarkable potential in various applications.[1−4] These applications include active matrix displays, RFID tags, and logic circuits, showcasing the versatility of these transistors. However, a major challenge with these advanced TFTs is their reliance on ZnO-related compound semiconductors. The use of scarce and costly elements such as indium and gallium in these compounds significantly hampers their widespread application and scalability. Consequently, the industry is facing a pressing need for high-performance TFTs that utilize more

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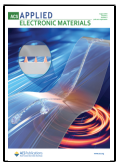

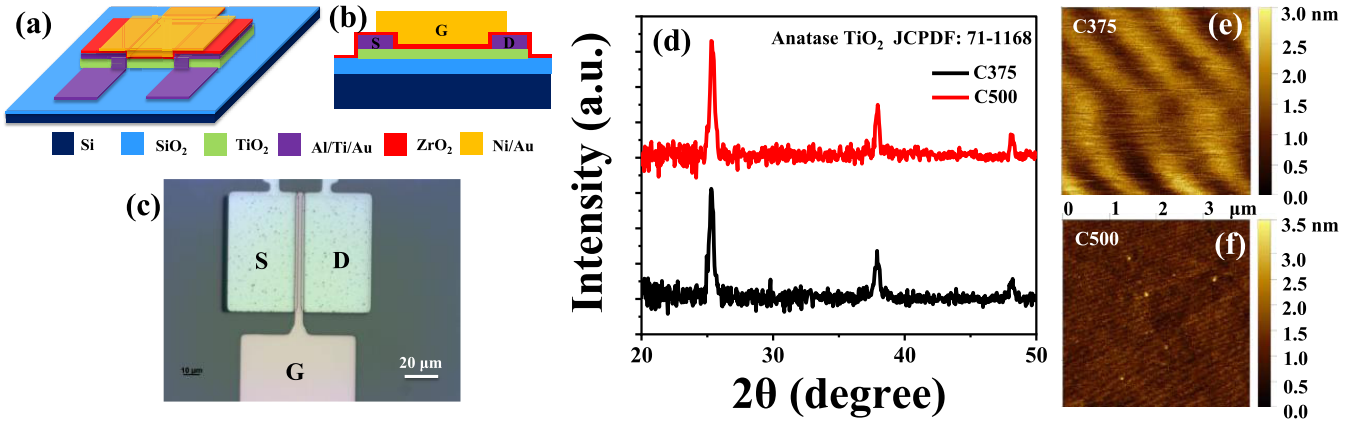

Figure 1. (a) Three-dimensional (3D) view and (b) cross-sectional view of the fabricated TiO_2 thin-film transistors (TFTs) with the same device dimensions. (c) Top-view microscopy image of the fabricated TiO_2 TFTs. (d) Grazing incidence X-ray diffraction (GI-XRD) spectrum of O_2-annealed TiO_2 films with different temperatures. AFM images for chips (e) C375 and (f) C500.

cost-efficient and readily available materials, especially for large-scale electronic applications.

Titanium oxide (TiO_2) has emerged as a promising solution in this context. TiO_2 stands out due to its chemical and mechanical stability, nontoxic nature, cost-effective growth methods, and abundance on earth. These properties position TiO_2 as an ideal candidate for channel materials in TFT applications. Recent developments have led to the successful fabrication of TiO_2-based TFTs, which have demonstrated performance levels comparable to their InGaZnO counterparts.[5−7] For instance, Katayama et al. developed a field-effect transistor (FET) using a rutile TiO_2 active channel, employing an amorphous $LaAlO_3$ insulator on ultrasmooth rutile single crystals. This structure, achieving reproducible n-type FET action with aluminum as the source/drain contact, displayed notable anisotropy in field-effect mobility.[8] The introduction of a MgO insulating buffer layer between TiO_2 and $LaAlO_3$ reduced the off-state current, achieving a decent on-to-off current ratio of 10^4 and a poor subthreshold swing (SS) (>3 V/dec). The team also proposed an oxygen modulation method for growing high-quality anatase films.[9] This method involved alternating deposition under low oxygen pressure with annealing under high oxygen pressure, enhancing the crystallinity of the film and resulting in high resistivity. The anatase film exhibited superior performance in FETs, with an on-to-off current ratio over 10^5 and a field-effect mobility exceeding 0.3 cm^2/V-s. There is another report on the fabrication of n-type TiO_x TFTs, with Al as the source/drain contact, using metal−organic chemical vapor deposition at 250 °C, achieving ideal characteristics.[10] Through optimal N_2O plasma treatment, they successfully reduced the off-current, significantly improving the on-to-off ratio without affecting the on-current.[11] This method resulted in a significant increase in the on-to-off ratio by almost 5 orders of magnitude. However, the reported device exhibited a poor subthreshold swing of 1.47 V/dec. In a separate study, Park et al. enhanced the performance of n-type TiO_x TFTs with plasma-enhanced atomic layer deposition (ALD).[12] Here, the source/drain contacts were made of Al. The N_2O plasma treatment improved the on-to-off ratio to 4.7×10^5 with a saturation mobility of 1.64 cm^2/V-s. Also, Choi et al. fabricated an amorphous TiO_2 channel-based oxide TFT, with molybdenum as the source/drain contact, using direct-current magnetron sputtering, achieving notable mobility and on-to-off ratios after rapid thermal annealing (RTA).[13] Another report, Zhong et al. observed an enhancement in the electrical characteristics of TiO_x TFTs using SiO_2 as the gate dielectrics post-annealing, which improved the interface structure and TiO_x crystallinity.[14] After annealing, the device exhibited inferior characteristics such as a high threshold voltage (22.82 V) and a high subthreshold swing (>2 V/dec).

In our recent work, using a two-step annealing process (oxygen (O_2) annealing at 500 °C followed by nitrous oxide (N_2O) annealing at 300 °C), we developed a titanium oxide (TiO_2) transistor that showed good performance, with a subthreshold swing of 92 mV/dec, an off-current $\sim 10^{-12}$ A, and a saturation current of approximately 2.8 μA/μm at a drain−source voltage (V_{DS}) of 2 V.[15] In this paper, to further enhance its performance and ultimately obtain a BEOL-compatible fabrication process, we experimented with O_2 annealing at different temperatures. After fine-tuning these annealing conditions, we achieved even better performance in our TiO_2 transistors. The improvements included a lower subthreshold swing of 88 mV/dec and a reduced off-current of around 10^{-13}−10^{-14} A at an operating voltage of 1 V, which make the ICs ideal for low-power IoT applications. To understand how these changes improved the transistor performance, we conducted an in-depth investigation of the interface quality between TiO_2 and zirconium dioxide (ZrO_2) and its correlation with the oxygen vacancies based on surface-sensitive techniques such as X-ray photoelectron spectroscopy (XPS), photoluminescence (PL), and AC conductance−voltage (G−V) measurements. Additionally, a carrier transport mechanism was proposed, allowing a better understanding of TiO_2 material properties for future electronic and optoelectronic devices.

2. RESULTS AND DISCUSSION

Figure 1a−c respectively shows the three-dimensional schematic, cross-sectional view, and top-view microscopic image of the fabricated TiO_2 TFTs. All TFTs have a top gate configuration with different source-to-drain or channel length (L_{SD}) values and a fixed gate width (L_W) of 70 μm with a gate-to-source/drain overlap ($L_{GS,OV}$/$L_{GD,OV}$) of 1.5 μm. The crystal structure of the ALD-deposited TiO_2 film was characterized by X-ray diffraction (XRD). Figure 1d shows the XRD data for TiO_2 films annealed at 375 and 500 °C, wherein both samples exhibit a polycrystalline nature with peaks at 24.8, 37.4, and

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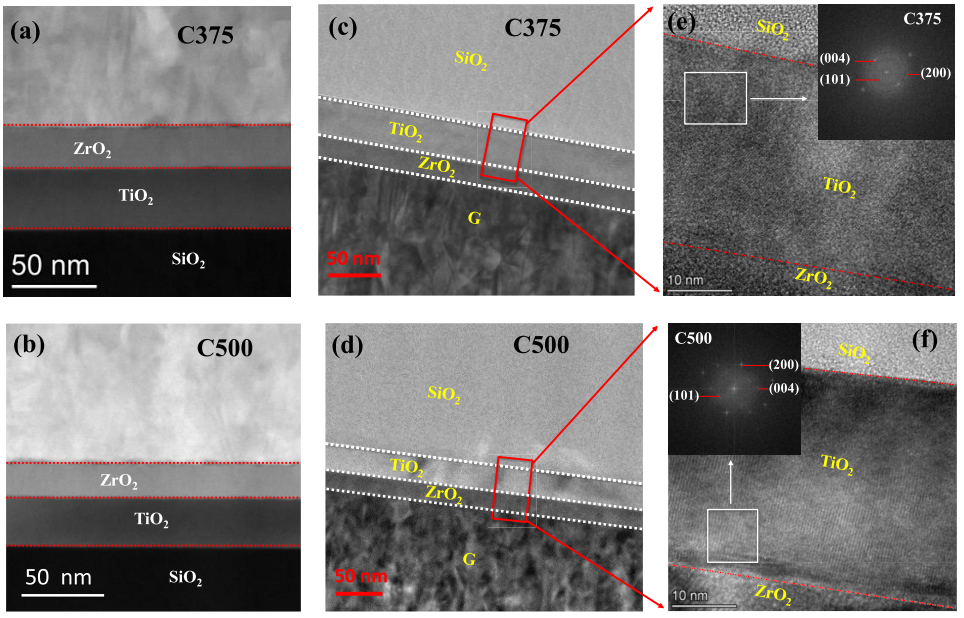

Figure 2. STEM-HAADF image of the TiO_2 device for chips (a) C375 and (b) C500. Cross-sectional TEM images of the layered structure for chips (c) C375 and (d) C500. High-resolution TEM images for the TiO_2/ZrO_2 interface of the selected region for chips (e) C375 and (f) C500. The inset shows the fast Fourier transform image of the selected region.

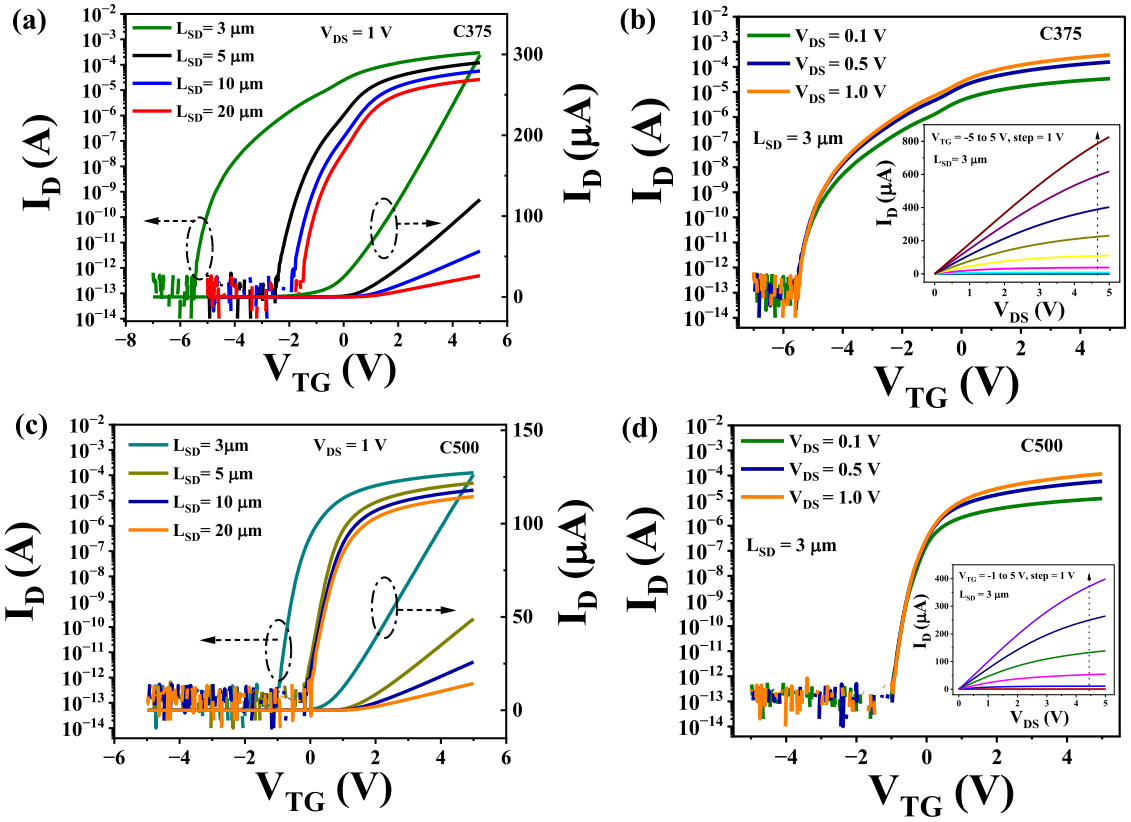

Figure 3. Transfer curves (I_D–V_{TG}) with different source-to-drain length (L_{SD}) values for chips (a) 375 and (b) 500. Transfer curves with different drain voltage V_{DS} values for a fixed channel length L_{SD} = 3 μm for chips (c) C375 and (d) C500. The insets show the output characteristics data (I_D–V_{DS}) recorded with different top gate voltage (V_{TG}) values.

47.6°, corresponding to the (101), (004), and (200) crystal planes of the anatase phase. The surface morphology of the channel is also important for achieving a high-quality channel/dielectric interface. Thus, surface roughness measurement is performed by atomic force microscopy (AFM) after O_2 annealing and N_2O treatment. Figure 1e,f shows the atomic force microscopy (AFM) image of the TiO_2 channel with N_2O treatment for chips C375 and C500, respectively. It is seen that O_2 annealing alone does not significantly affect the root mean square (RMS) surface roughness of the channel data given in

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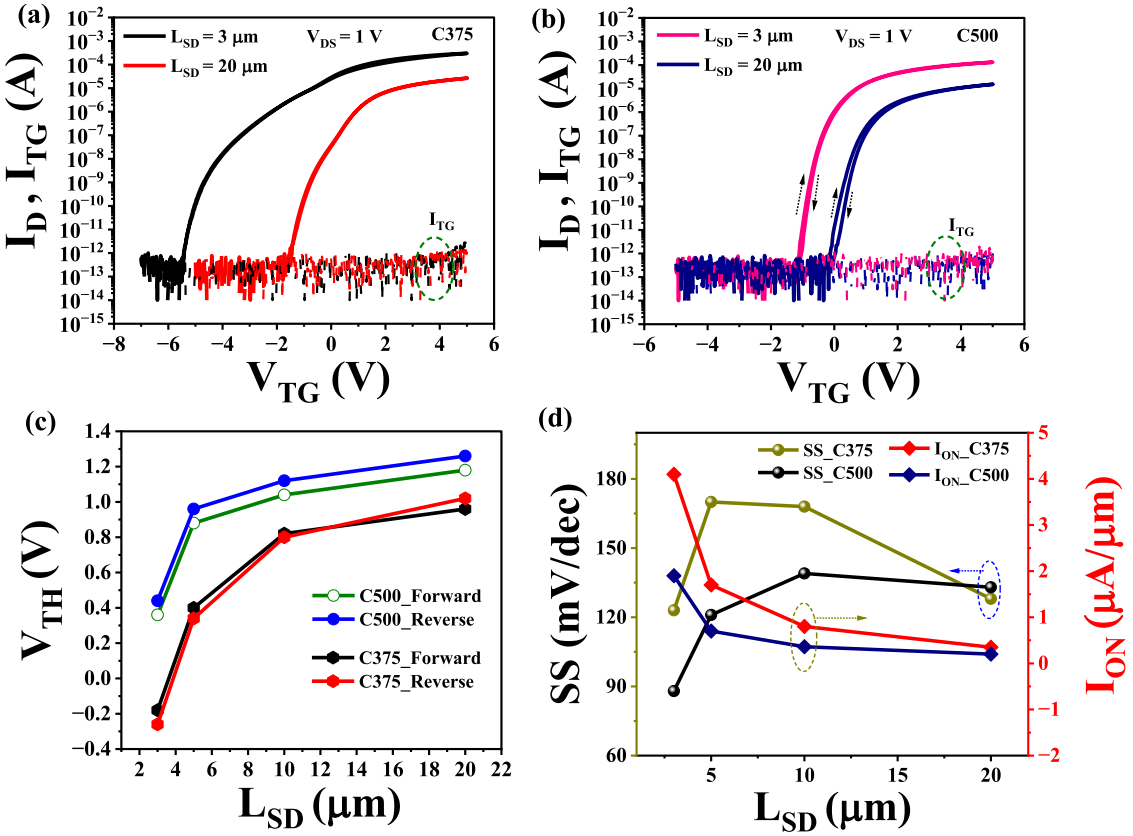

Figure 4. Double-sweep transfer curves (I_D−V_{TG}) of short-channel (L_{SD} = 3 μm) and long-channel (L_{SD} = 20 μm) devices with the gate leakage current for chips (a) C375 and (b) C500. (c) Threshold voltage (V_{TH}) as a function of the channel length for forward and reverse sweeps for both chips. (d) SS as a function of the channel length (L_{SD}) of the TFTs on chips C375 and C500. The right-hand axis in the same graph shows I_{ON} as a function of L_{SD}.

the Figure S1, Supporting Information. Interestingly, the RMS surface roughness of the channel reduced substantially from 0.6 to 0.3 nm with N_2O treatment for the chip C500. However, for chip C375, the RMS surface roughness is slightly decreased from 0.51 to 0.43 nm with N_2O treatment.

In order to understand the physical structure (film thickness) and interface quality of TiO_2 TFT, samples are investigated through cross-sectional transmission electron microscopy (TEM), and the focused ion beam (FIB) technique was employed for cross-sectional sample preparation for the above investigation.

Scanning transmission electron microscopy high-angle annular dark-field (STEM-HAADF) images of TiO_2 TFTs are shown in Figure 2a,b for chips C375 and C500, respectively. Figure 2c,d shows the cross-sectional TEM images of the TiO_2 TFT corresponding to chips C375 and C500, respectively. The thickness of the TiO_2 and ZrO_2 layers, as depicted in the TEM image, are ≈30 and ≈20 nm, respectively. Figure 2e,f further shows the high-resolution TEM image of the ZrO_2/TiO_2 interface for chips C375 and C500, respectively. As depicted in the images, the interface between ZrO_2 and TiO_2 is very sharp for the high-temperature chip C500 in comparison with the low-processing chip C375, and the lattice structure with different crystal orientations is observed in TiO_2, indicating the polycrystalline nature of TiO_2.[5] The fast Fourier transform (FFT) image of the selected region is shown in the inset of Figure 2e,f, which predicts better polycrystallinity of the TiO_2 anatase phase for chip C500 in comparison with chip C375. First, we measured the electrical characteristics of the two chips C375 and C500 with different channel length (L_{SD}) devices.

To understand the effects of N_2O plasma treatment on the electrical properties of the TiO_2 channel, the I_D−V_{DS} curves with V_{BG} = 0 V of the TiO_2 back gate device were tested with the N_2O treatment time and different N_2O flow rates. Data are given in the Figure S2, Supporting Information. The electrical performance of TiO_2 can be enhanced by a proper N_2O plasma treatment duration, while excessive treatment results in degradation, which agrees with previous reports based on other oxide channels.[16] Figure 3a,c shows the transfer (I_D−V_{TG}) curves with different channel lengths for C375 and C500 at V_{DS} = 1 V, respectively, and the right-hand axis in the same graph shows the linear behavior of the drain current I_D with respect to the channel length. As shown in the figure, the threshold voltage of the devices gradually shifts to the right side with increasing channel length due to more electron trapping in the channel and dielectric interface. Figure 3b,d shows the typical transfer characteristics with different drain voltage V_D values for a fixed channel length L_{SD} = 3 μm of chips C375 and C500, respectively. The output characteristics data (I_D−V_{DS}) recorded with different top gate voltage (V_{TG}) values from −5 to 5 V with steps of 1 V are shown in the inset of Figure 3b,d for chips C375 and C500, respectively. The double-sweep transfer curves (I_D−V_{TG}) at V_{DS} = 1 V were recorded to measure the hysteresis of short-channel (L_{SD} = 3 μm) and long-channel (L_{SD} = 20 μm) devices for both chips C375 and C500, as shown in Figure 4a,b, respectively, and the same graph also shows the gate leakage current (I_{TG}). The low

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Table 1. Comparisons of This Work with Other TiO_2 TFTs from the Published Literature[a]

channel/dielectric	method	V_{DS} (V)	SS (mV/dec)	μ_{FE} (cm^2/(V s))	I_{ON} (μA/μm)	I_{ON}/I_{OFF}	references
TiO_2/ZrO_2	PE-ALD	10	112	4	1.42	1.4×10^8	5
TiO_2/ZrO_2	Th-ALD	20	101	5	10	1.2×10^9	6
$TiO_2/LaAlO_3$	PLD	100	>1000	0.3	0.05	10^5	9
TiO_2/SiO_2	PE-ALD	35	1860	1.64	4.0	4.7×10^5	12
TiO_2/SiO_2	sputtering	10	2450	0.69	0.03	2×10^7	13
TiO_2/ZrO_2	PE-ALD	2	92	5.45	2.8	2.5×10^8	15
TiO_2/SiO_2	sputtering	10	>1000	10.7	1.8	10^4	18
TiO_2/SiO_2	sputtering	10	>1000	0.04	0.03	4×10^4	14
TiO_2/ZrO_2	Th-ALD	20	142	2.5	1.4	1.4×10^8	19
TiO_2/ZrO_2	Th-ALD	1	123	2.95	4.1	10^9	this work
TiO_2/ZrO_2	Th-ALD	1	88	1.5	1.5	10^9	this work

[a]PE = plasma-enhanced; Th = thermal.

I_{TG} with a flat curvature in all samples indicates the excellent insulating properties of ZrO_2. All TFTs show negligible hysteresis, indicating a smaller number of mobile charges in the dielectric/semiconductor interface. The TFT with a short channel (L_{SD} = 3 μm) in chip C500 shows exceptional switching characteristics, including a high I_{ON}/I_{OFF} ratio of ~10^9, a low subthreshold swing (SS) of 88 mV/dec, and a low off-current of ~10^{-13} A. In contrast, the value of SS with a short channel (L_{SD} = 3 μm) device on chip C375 increased to 123 mV/dec due to a large value of the interface state in a low-annealing channel/dielectric interface.

It is noted that SS are extracted over two decades of drain current from 10^{-12} to 10^{-10} A according to the equation[15]

$$SS = \left(\frac{\partial \log(I_{DS})}{\partial V_{GS}}\right)^{-1} \quad (1)$$

The steep SS for chip C500 can be ascribed to a possible high-quality channel/dielectric interface with low interface state traps (D_{it}), which will be discussed in detail in the next section. As shown in Figure 4c, the threshold voltage during reverse sweep is shifted to the right (positive) in chip C500, whereas it is shifted to the left (negative) in chip C375 for a short channel length. It has been suggested that this unusual shift may be the result of an irreversible charge−discharge effect in bulk traps that already existed.[17] Moreover, in standard performance devices, the threshold voltage (V_{TH}) shifts positively during fast $I-V$ double-sweep measurement. However, for short-channel length devices in chip C375, the threshold V_{TH} shifts negatively as channel electrons escape from bulk traps to metal gates instead of injecting into bulk traps. Figure 4d shows the variation of SS with channel length (L_{SD}) of the TFTs on chips C375 and C500. The right-hand axis in the same graph shows the I_{ON} current as a function of L_{SD}, and the value of the I_{ON} current decreases with increasing channel length of devices due to a reduced channel resistance.

Interestingly, as shown in the data, the value of the I_{ON} current decreased for chip C500 due to an increase in the contact resistance and sheet resistance. The contact resistance (R_C) and sheet resistance (R_S) measured by the transmission line method (TLM) for chip C500 are 13.5 and 5.3 kΩ, respectively (given in the Figure S3, Supporting Information), whereas for chip C375, the values are R_C = 6.4 kΩ and R_S = 2.7 kΩ.

The performance of a TFT depends on the quality of the channel as it can give rise to high carrier mobilities. The field-effect mobility (μ_{FE}) of the carriers in the channel and the threshold voltage V_{TH} of the TFT were calculated using the following conventional equation[15]

$$\mu_{FE} = \frac{L}{WC_{OX}V_{DS}} g_m \quad (2)$$

where L and W are the length and width of the device, respectively, C_{OX} is the specific gate capacitance obtained by $C-V$ measurement, and $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$ is the transconductance. For chip C375 with a short channel, the extracted value of μ_{FE} is 2.95 cm^2/V-s, whereas for chip C500, it is 1.5 cm^2/V-s. In addition, the outstanding electrical performance of TiO_2 TFTs stands out among the state-of-the-art TFTs based on the TiO_2 channel and compares favorably with the previous literature reports on TiO_2 (Table 1).[14,18,19] We also tested multiple devices with the same L_{SD} = 3 μm for both chips. The data are shown in Figure S4 (given in the Supporting Information), and deviations in the subthreshold slope (SS) and threshold voltage (V_{TH}) are less than ±4%, which is important for large-area applications and circuit integration. We tested the aging effect of our TiO_2 TFT with time and measured the electrical characteristics. As shown in the data (given in the Figure S5, Supporting Information), performance parameters such as subthreshold swing (SS) and threshold voltage (V_{TH}) of TiO_2 TFTs for both chips degraded barely even after a 4-month time period. We also determined the environmental stability of our TiO_2 TFTs and measured their electrical characteristics with a relative humidity of up to 80%. The transfer curves of TFTs shifted to negative values for chip C375 because of electron trapping and detrapping at the channel/dielectric interface, whereas no obvious shift was observed for chip C500 (given in the Figure S6, Supporting Information), suggesting the feasibility of our TiO_2 TFTs for practical applications.

In addition, we also performed a gate bias stability test on TiO_2 TFTs on the same short-channel device with L_{SD} = 3 μm for chips C375 and C500. Figure 5a,b shows the measurement setup (the details are given in the Figure S7, Supporting Information) for TiO_2 TFTs under negative bias stress (NBS) and positive bias stress (PBS) tests in the dark, while the negative bias illumination stress (NBIS) and positive bias illumination stress (PBIS) tests are performed using laser light with illumination wavelength λ = 600 and 400 nm and intensity I = 150 mW/cm^2 for a better understanding of the device mechanism in the presence of oxygen vacancies. Figure 5c,d shows the transfer curves of the TiO_2 TFT under V_{DS} = 1 V after different accumulated bias times up to 1800 s during negative bias stress in the dark for chips C375 and C500,

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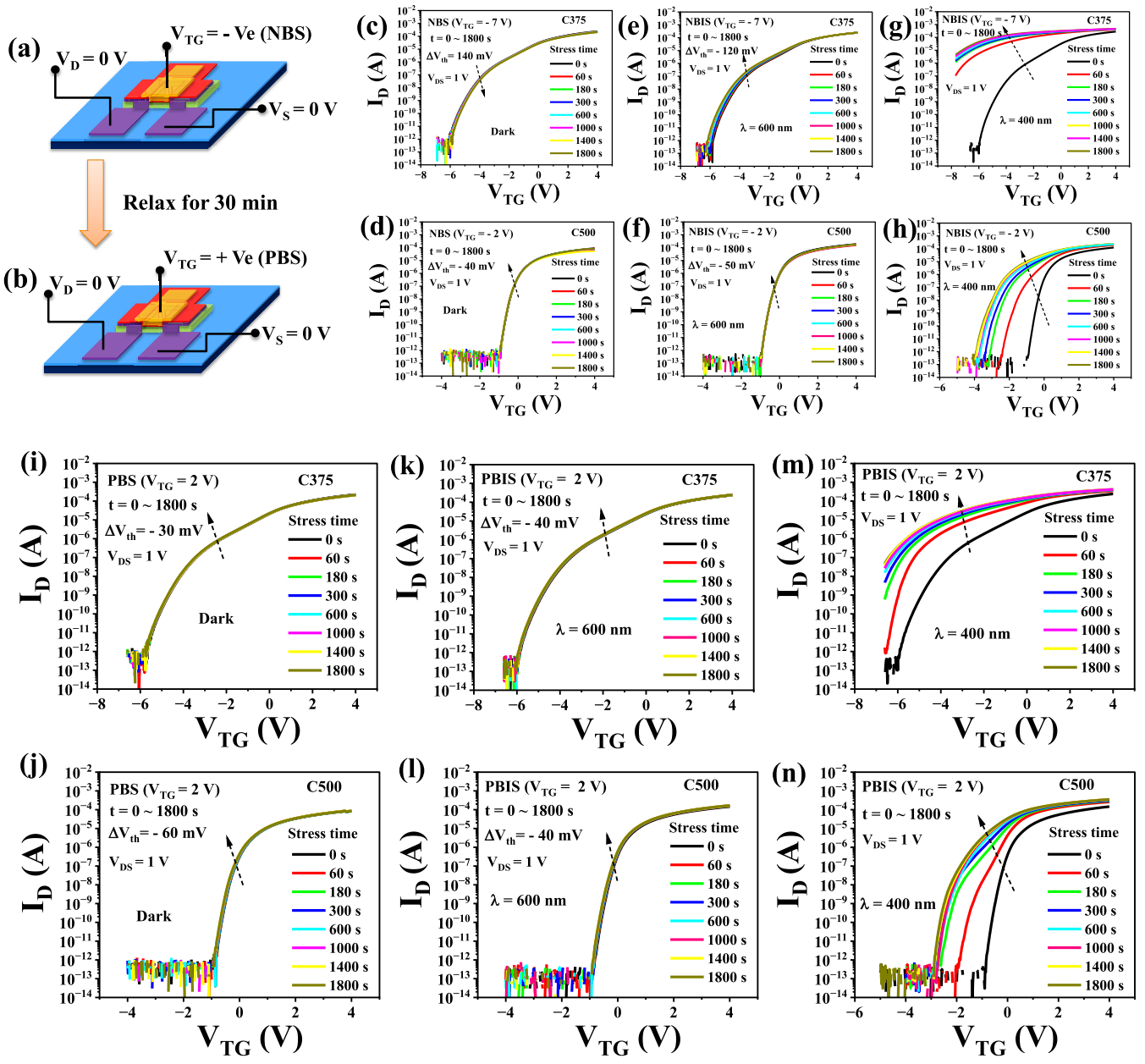

Figure 5. Measurement setup for TiO_2 TFTs under (a) negative bias stress (NBS) and (b) positive bias stress (PBS) tests. Transfer curves (I_D–V_{TG}) of the TiO_2 TFT for chips (c) C375 and (d) C500 during the NBS test in the dark. Transfer curves of the TiO_2 TFT for chips (e) C375 and (f) C500 during the NBIS test with the illumination of light with λ = 600 nm. Transfer curves of the TiO_2 TFT for chips (g) C375 and (h) C500 during the NBIS test with the illumination of light with λ = 400 nm. Transfer curves (I_D–V_{TG}) of the TiO_2 TFT for chips (i) C375 and (j) C500 during the PBS test in the dark. Transfer curves of the TiO_2 TFT for chips (k) C375 and (l) C500 during the PBIS test with the illumination of light with λ = 600 nm. Transfer curves of the TiO_2 TFT for chips (m) C375 and (n) C500 during the PBIS test with illumination of light with λ = 400 nm.

respectively, while Figure 5e,f shows the transfer curves of the TiO_2 TFT after different accumulated bias times up to 1800 s during the NBIS test with illumination of light with λ = 600 nm for chip C375 and C500, respectively. Interestingly, when the illumination wavelength λ = 600 nm, the transfer curves of TFTs in Figure 5e,f are slightly shifted toward negative values for both the chips in comparison to those in Figure 5g,h with an illuminated wavelength λ = 400 nm. This enormous shift of the transfer curve occurs because of a synergetic effect of the electron trapping and detrapping at the channel/dielectric interface with the excitation of oxygen vacancies under gate bias with the illumination wavelength λ = 400 nm.[15]

Similarly, Figure 5i,j shows the transfer curves of the TiO_2 TFT under V_{DS} = 1 V after different accumulated bias times up to 1800 s during positive bias stress in the dark for chips C375 and C500, respectively. Figure 5k,l depicts the transfer curves of the TiO_2 TFT after different accumulated bias times up to 1800 s during the PBIS test with the illumination of light with λ = 600 nm for chips C375 and C500, respectively. Similarly, when the illumination wavelength λ = 400 nm, the transfer curves of TFTs in Figure 5m,n for chips C375 and C500, respectively, shifted toward negative values for both the chips in comparison to those in Figure 5k,l with λ = 600 nm. Our TFTs show excellent stability with minimum electrical

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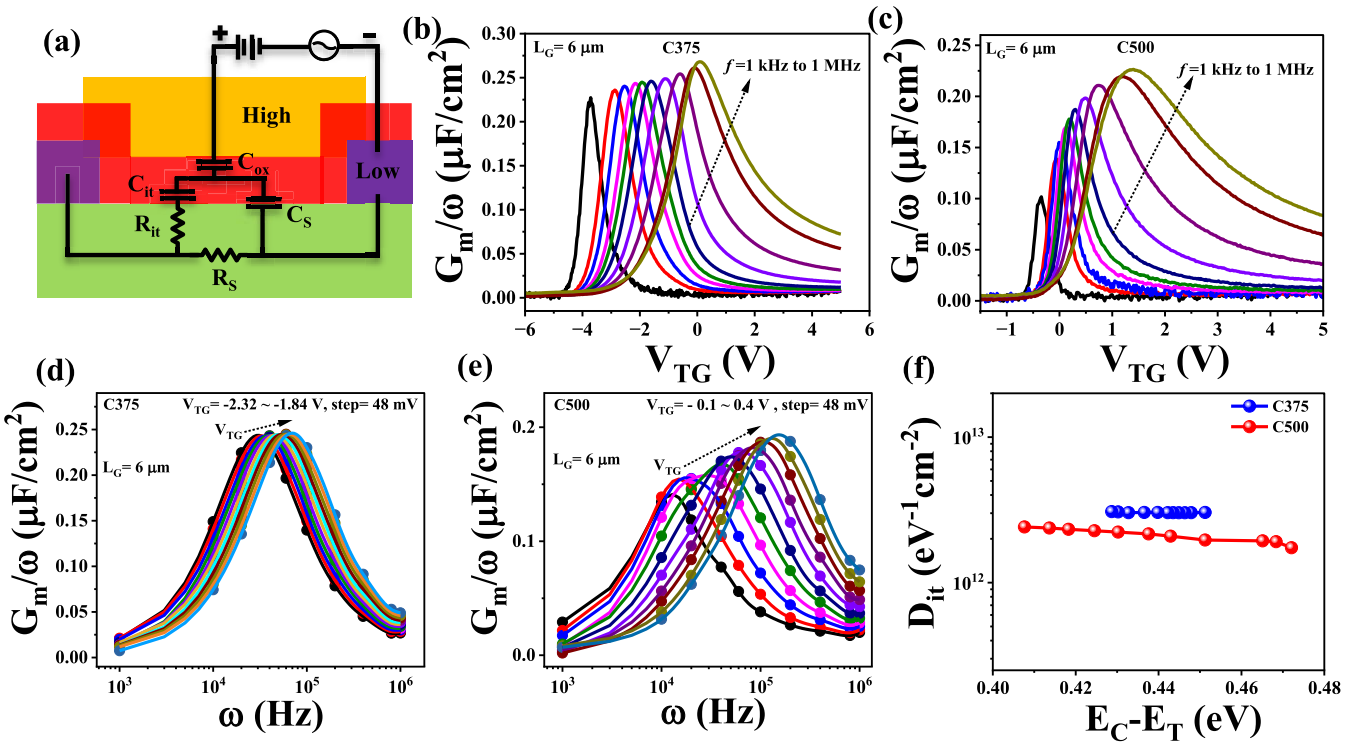

Figure 6. (a) Schematic illustration of the $C/G-V/f$ measurement setup of the TiO_2 TFT. Measured equivalent parallel conductance (G/ω) as a function of the applied voltage for chips (b) C375 and (c) C500. Conductance (G/ω) as a function of ω for interface trap density (D_{it}) extraction for chips (d) C375 and (e) C500 using the AC conductance method. Note that the symbols denote measured data and lines denote fitting results. (f) Comparison of the extracted D_{it} as a function of the energy level for the device with the channel length (L_{SD} = 3 μm) for both chips.

performance changes upon both NBS and PBS in the dark as well as with illumination gate stress up to 1800 s, suggesting the feasibility of our TiO_2 TFTs for practical applications.

We further investigated the interface quality of ZrO_2/TiO_2 by systematic capacitance–voltage ($C-V$) and AC conductance–voltage ($G-V$) measurements at different frequencies (1 kHz to 1 MHz) to extract the D_{it}. In order to measure the $C-V$ and $G-V$ responses of TFTs, the gate terminal was biased high, the source terminal was biased low, and the drain terminal was left open with an AC signal being superimposed, as shown in Figure 6a. The value of dielectric capacitance (C_{OX}) ~1 μF/cm^2 was calculated from the accumulation region of the $C-V$ curves. According to Figure S8a in the Supporting Information, $C-V$ curves are stretched over the frequency range of 1 kHz to 1 MHz for chip C375 because of the trapping of charge carriers in the interface trap states.[20−22] On the other hand, for chip C500 in Figure S8b, however, the low interface trap density and small frequency dispersion of capacitance indicate a good interface. The interface trap state density D_{it} was extracted from the measured equivalent parallel conductance G_m as a function of the bias voltage and frequency.

Figure 6b,c shows the measured equivalent parallel conductance (G_m/ω) as a function of the applied voltage under different frequencies for chips C375 and C500, respectively. The $G_m/\omega-V$ curves show that there is a peak at a certain frequency, and as the application frequency increases, the peak intensity increases, and its position shifts toward a higher applied voltage. For the interface states, the conductance represents the loss mechanism resulting from the trapping and detrapping processes of the charge carriers. It is described by the equation below[7,23]

$$\frac{G_m}{\omega} = \frac{e_0 D_{it}}{2\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2] \quad (3)$$

where D_{it} is the interface trap density, τ_{it} is the corresponding trap lifetime constant, ω is the angular frequency ($\omega = 2\pi f$), and e_0 is the elementary electron charge. Thus, the value of D_{it} and its related time constant τ_{it} can be obtained quantitatively with $D_{it} = \frac{2.5}{e_0}\left(\frac{G_m}{\omega}\right)_{peak}$ and $\tau_{it} = \frac{1.98}{\omega_0}$ by fitting the experimental $G_m/\omega-\omega$ data. Figure 6d,e shows the conductance as a function of the angular frequency under different top gate voltage (V_{TG}) values for chips C375 and C500, respectively. It must be noted that the symbols indicate experimental data, which are well matched with the modeled results that are indicated by lines.

The extracted D_{it} with its related time constant τ_{it} can be mapped to the energy level ($E_C - E_T$) according to the Shockley–Read–Hall statistics[24,25]

$$\tau_{it} = \frac{1}{\upsilon_{th}\sigma_n N_C} \exp\left(\frac{E_C - E_T}{\kappa T}\right) \quad (4)$$

where ν_{th} is the thermal velocity, σ_n is the electron capture cross section, and N_C is the effective density of states in the TiO_2 conduction band. By assuming T = 300 K, $\nu_{th} = 10^7$ cm/s, $\sigma_n = 10^{-14}$ cm^2, and $N_C = 10^{19}$ cm^{-3}, the extracted D_{it} values are shown comparatively in Figure 6f as a function of the energy level for both chips C375 and C500. It is observed that the D_{it} of ~3 × 10^{12} 1/eV cm^2 for chip C375 reduced to ~1.8 × 10^{12} 1/eV cm^2 with the high annealing temperature for chip C500. The reduced D_{it} value can be explained by the fact that surface contamination is substantially reduced with increasing O_2 annealing temperature (we will discuss this in detail in a

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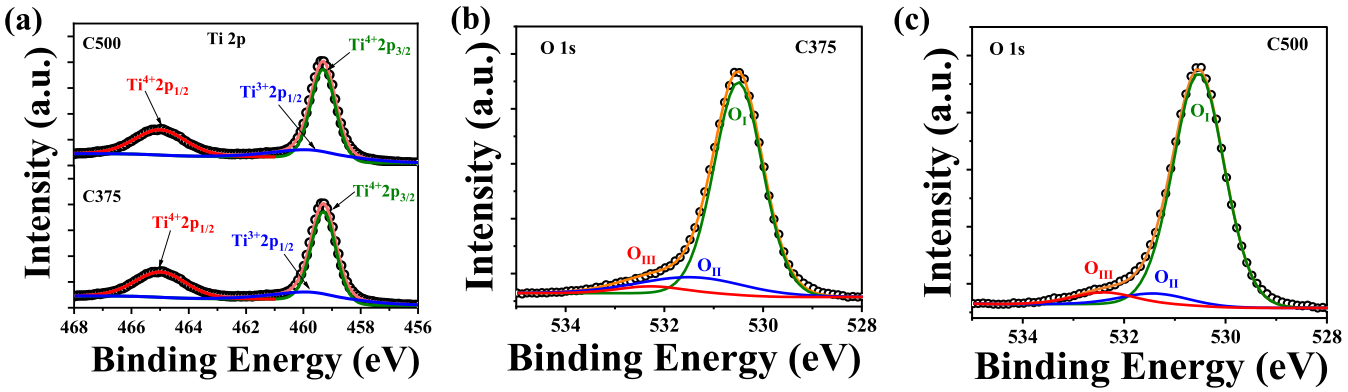

Figure 7. Chemical analysis of TiO_2 films with different annealing temperatures. (a) Ti 2p peak for chips C375 and C500. Deconvoluted XPS spectra of the O 1s peak in lattice oxygen (O_I), carbonate species (O_{II}), and surface adsorbate (−OH)/nonlattice oxygen (O_{III}) for chips (b) C375 and (c) C500.

later section), which leads to a high-quality channel/dielectric interface with low interface state traps (D_{it}) as result of a steep SS for chip C500.

To understand the effect of the annealing temperature on the chemical composition as well as the surface state of TiO_2 films, the films were investigated by XPS. A surface-sensitive technique such as XPS can provide information regarding changes in the chemical state of the species that constitute the film.

Figure 7a shows the high-resolution XPS spectra of Ti 2p peak with deconvoluted spectra. The decomposition of Ti 2p leads to Ti $2p_{3/2}$ and Ti $2p_{1/2}$ peaks located at 459.2 and 464.9 eV, respectively, with a spin−orbit splitting of 5.7 eV.[26] This corresponds to the typical signature for Ti^{4+} in stoichiometric TiO_2. However, there is also a shoulder peak at a binding energy of 460.4 eV corresponding to the Ti^{3+} in Ti_2O_3.[27,28] This indicates that both TiO_2 and Ti_2O_3 are formed in the film. Figure 7b,c shows the O 1s core-level spectra for chips C375 and C500, respectively. In all cases, the decomposition occurs through three major contributions denoted as O_I (530.5 eV), O_{II} (531.4 eV), and O_{III} (532.2 eV for C375 and 532.4 eV for chip C500). The low-energy peak O_I with a BE of 530.5 eV is assigned to the lattice oxygen (Ti−O) bond, while O_{II} and O_{III}, at higher binding energies, correspond to carbonate species (−CO) or the remaining precursor ligands stuck in the film related to surface contamination and nonlattice oxygen related to the −OH/surface-adsorbed state, respectively.[27] A quantitative analysis of the O 1s peaks is shown in Table 2.

It has been seen that for the high-annealing-temperature chip C500, the overall surface contamination (O_{II}) related to carbonaceous compounds/precursor ligands is substantially reduced by 61% in comparison with the low-annealing chip C375, which leads to a high-quality channel/dielectric interface with low interface state traps (D_{it}), as shown in Figure 6f, whereas the area of the nonlattice oxygen (O_{III}) increases by 54% for chip C500 with increasing annealing temperature. Therefore, the overall oxygen vacancies (V_os) were reduced by 37% for chip C500 with increasing O_2 annealing temperature. Photoluminescence (PL) spectroscopy was also performed to quantify the defect states of the TiO_2 film with different annealing temperatures (given in the Figure S9, Supporting Information), which is well corroborated with the XPS results.

Table 2. Area Percentage of the Deconvoluted O 1s Peak for ALD-Deposited TiO_2 Films Annealed at Different Temperatures

	chips			
	C375		C500	
deconvoluted O 1s peak	BE (eV)	area percentage (%)	BE (eV)	area percentage (%)
O_I	530.5	82.5	530.5	89
O_{II}	531.4	14	531.4	5.6
O_{III}	532.2	3.5	532.4	5.4
V_Os	17.5		11	

In order to conceptually depict the working mechanism of the device, a schematic representation of electron transport is shown in Figure 8. There are a large number of interface traps and oxygen vacancies in the TiO_2 channel for the low-annealing-temperature chip C375, as depicted in Figure 8a. However, these interface traps and oxygen vacancies were substantially reduced with an increasing O_2 annealing temperature for chip C500, as shown in Figure 8b. It is interesting to note that the presence of more donor-like oxygen vacancies in chip C375 may enhance the mobility of carriers with increasing carrier concentration,[29] whereas there is a degradation of the SS value due to the large number of interface states because of surface contamination. On the other hand, for chip C500, a high-quality channel/dielectric interface with low interface state traps (D_{it}) induces steep SS. However, there is an increase in the series electrical resistance (given in the Supporting Information) for chip C500, which degrades the ON state current of devices as compared with the low-annealing chip C375. In conclusion, the conductance of a TiO_2 thin film can be influenced by both the surface and the bulk, and oxygen vacancies can either be beneficial or disadvantageous depending on whether they are located in the bulk or at the interface.[29,30] Therefore, XPS measurement confirms that a high annealing temperature reduces the surface contamination related to carbonaceous compounds, which is crucial for the formation of a high-quality channel/dielectric interface. However, it needs to be emphasized that surface contamination and oxygen vacancies in the channel can be optimized by tuning the O_2 annealing temperature for the fabrication of high-performance electronic devices.

3. CONCLUSIONS

In summary, high-performance TiO_2-based TFTs were demonstrated by using multistack metal contacts along with

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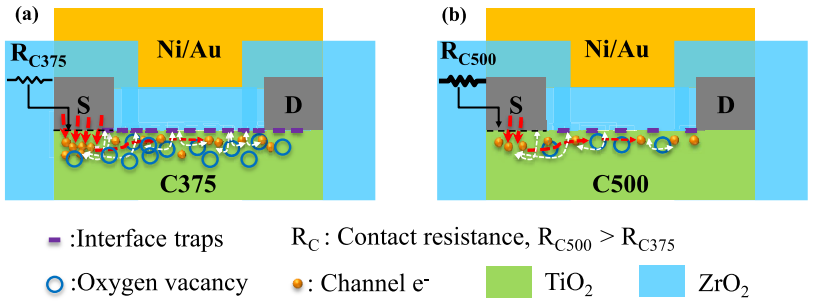

Figure 8. Schematic representation of the electron transport for chips (a) C375 and (b) C500 in a TiO_2 semiconductor channel in the presence of interface traps and oxygen vacancies.

a high-quality channel/dielectric interface. It is found that the carrier transport and electrical performance of TFTs can be tuned by O_2 annealing with the control of oxygen vacancies and contamination of the channel. TFTs with a higher O_2 annealing temperature (C500) exhibit an enhanced electrical performance, including a stepper SS of 88 mV/dec, a higher I_{ON}/I_{OFF} of ~10^9, and a mobility μ_{FE} of 1.5 cm^2/V-s under a battery-powered voltage of 1 V. In contrast, the transistors in chip C375 exhibit a degradation of SS value to ~123 mV/dec due to the large number of interface states. This high performance, along with low gate leakage and low I_{OFF} current, are highly promising to be employed in IoT applications with low power consumption requirements, offering a potential solution for applications with cost-effective demands. Furthermore, this study discloses the possible carrier transport mechanism in the stoichiometry with carbonaceous TiO_2 thin films, providing a better understanding of TiO_2 material properties, which facilitates the further development of TiO_2-based electronic and optoelectronic devices in the future.

4. EXPERIMENTAL SECTION

4.1. Fabrication Process. The devices were fabricated around a base of 260 nm thermally grown SiO_2/Si substrate, where SiO_2 was employed for isolation purposes. First, a thin TiO_2 film of 30 nm was deposited on the SiO_2/Si substrate by thermal atomic layer deposition (ALD) at 150 °C with tetrakisdimethylamino-titanium (TDMAT) and H_2O as the Ti and O sources, respectively. The sample was split into two chips, followed by rapid thermal annealing (RTA) at 375 and 500 °C for 30 min under an O_2 atmosphere. The chips were then subjected to the same device fabrication process. The devices using TiO_2 films annealed at 375 and 500 °C were named C375 and C500 chips, respectively. In the second step, the TiO_2 layer mesas were created by standard lithography and inductively coupled plasma (ICP) etching in a CF_4/Ar environment to isolate individual devices. After that, Al/Ti/Au (170 nm/10 nm/70 nm) was deposited as source/drain metal contacts followed by RTA annealing under a N_2 atmosphere at 300 °C. The chips were then brought into a plasma-enhanced chemical vapor deposition (PECVD) chamber to carry out N_2O treatment at 300 °C for 1 min. Next, a 20 nm-thick ZrO_2 gate dielectric was deposited by O_2 plasma-enhanced ALD. Finally, the Ni (180 nm)/Au (70 nm) metal stack was evaporated as the gate contact.

4.2. Characterization Methods. The crystal structures of the TiO_2 thin films with different annealing temperatures were characterized by grazing incidence X-ray diffraction (GI-XRD). The physical thicknesses of channel TiO_2 and dielectric ZrO_2 were measured by an ellipsometer (J.A. Woolam M-2000VI) using the Cauchy model based on the accompanying Si wafer during deposition. The surface morphology and roughness of TiO_2 mesas with different ZrO_2 thicknesses were examined by atomic force microscopy (AFM) in the tapping mode (Dimension-3100 V SPM). In order to understand the physical structure (film thickness) and interface quality of TiO_2 TFTs, samples are characterized by cross-sectional transmission electron microscopy (TEM). The focused ion beam (FIB) technique (Tescan S8000X Plasma FIB) was employed for cross-sectional sample preparation for the above investigation. Photoluminescence (PL) spectroscopy with 320 nm pulsed excitation by a Ti:sapphire laser source was used in a time-correlated single photon counting (TCSPC) system to quantify the defect states of the TiO_2 film with different annealing temperatures. The chemical compositions of the TiO_2 thin films were analyzed by X-ray photoelectron spectroscopy (XPS) (Thermo Scientific) with an Al Kα X-ray source at an energy of 1486.6 eV at a base pressure below 5 × 10^{-8} Torr. The data analysis was performed with Advantage software. All peak positions and relative sensitivity factors were calibrated to the C 1s peak at 284.8 eV, and the error in the binding energies is within 0.1 eV. For accurate detection, 5 nm-thick film surfaces were etched with Ar ions before XPS characterization. Current−voltage (I−V) measurements of the two chips were carried out at room temperature using an Agilent B1500A semiconductor parameter analyzer. Capacitance−voltage (C−V) measurements were also performed at room temperature using the Agilent B1520A from 1 kHz to 10 MHz.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.4c00524.

AFM images; I_D−V_{DS} curves of the TiO_2 back gate device with different N_2O treatment times and flow rates; I_D−V_{DS} data for the TLM structure; reproducibility of TiO_2 TFTs; stability (aging effect); environmental stability of TiO_2 TFTs; measurement setup for NBS and PBS tests; capacitance−voltage (C−V) at different frequencies; room temperature PL spectra with deconvoluted peaks of the TiO_2 film (PDF)

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Author Contributions

C.S.: conceptualization, data curation, formal analysis, and writing—original draft and methodology; S.Y.: writing—review and editing; T.Z.: data curation and AFM analysis; H.Z.: data analysis (TEM); L.G.: data curation (PL); Y.Z.: supervision, conceptualization, and project administration. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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