Real-time Model Predictive Control of a DC-DC Buck Converter

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Abstract—We propose a digitally assisted analog computing circuit for real-time model predictive control (MPC) of a DC-DC buck converter. The computing circuit comprises analog elements for speed and digital components for programmability. It implements gradient-flow dynamics for a penalty-based reformulation of the quadratic optimization problem corresponding to the original MPC formulation. The MPC problem is set up to regulate output voltage while explicitly enforcing constraints on the buck converter's inductor current and duty cycle. Simulation results in a closed-loop configuration demonstrate superior dynamic response with lower settling time and overshoot compared to the Type-III controller and linear quadratic regulator (LQR). The proposed approach achieves accuracy similar to the numerically computed optimal solution from the interior-pointconvex algorithm of MATLAB's quadprog solver while offering real-time implementation capability.

Index Terms—Analog circuits, DC-DC power converters, digital circuits, gradient methods, optimization, predictive control.

I. Introduction

The drive to reduce the size of passive components has increased switching frequencies for power converters across applications. This reduces the passive components' ability to store energy, leading to faster dynamics. These rapid dynamics necessitate that companion control and optimization routines be executed faster. However, bottlenecks due to delays in digital circuits (frequently leveraged for control and optimization) are unavoidable. As a result, it is common to resort to offline routines, such as look-up tables, rather than real-time optimization [1]–[4]. This compromise often results in suboptimal converter performance and robustness.

This paper presents a digitally assisted analog computing circuit (DAACC) that implements real-time model predictive control (MPC) of a DC-DC buck converter. The optimization problem is formulated to regulate output voltage while enforcing bounds on inductor current and the duty cycle. The DAACC is built with operational amplifiers (op-amps), diodes, and passive circuit elements judiciously assisted by a digital circuit. The proposed solution preserves desirable attributes of digital computing (programmability customized to the application) and analog circuits (speed of response). From

This work was supported in part by the National Science Foundation (NSF) through awards 2305431 and 2305432.

a mathematical and control-theoretic point of view, the states of the DAACC realize gradient-flow dynamics for a penalty-based reformulation of the original MPC problem. Equilibria of the DAACC are engineered to coincide with the first-order Karush-Kuhn-Tucker (KKT) conditions for optimality [5].

Several works have proposed synthesizing analog circuits to simulate and optimize a wide range of physical systems, including power converters [3], [6]–[16]. Similarly, there has been significant interest in MPC for power electronics [17]–[27]. A comprehensive review of MPC formulations in power electronics, including computational complexity and stability, can be found in [2]. Most solutions for power electronics applications have been implemented in the digital domain, with the exception being [11]. Our implementation involving penalty-based gradient-flow dynamics offers a different solution strategy compared to [11]. While not directly pursued in this work, it can also encompass nonlinear objective (cost) functions [3], [6], [28]. We demonstrate via switching-level simulations that the proposed DAACC facilitates real-time implementation of MPC.

The remainder of this paper is structured as follows. Section II introduces the formulation of the MPC problem. The reformulation of the MPC problem using the penalty method and the circuit-based realization are described in Section III. Section IV presents simulation results for the MPC problem and a comparative analysis with conventional control methods. Finally, Section V concludes the paper.

II. MODEL PREDICTIVE CONTROL (MPC) PROBLEM FORMULATION

This section presents the Model Predictive Control (MPC) problem formulation for a DC-DC buck converter. We begin by introducing the state-space model of the buck converter, followed by the MPC problem formulation.

A. Buck Converter State-space Model

We develop an MPC solution for a buck converter to step down input voltage, $V_{\rm in}$, to output voltage, $v_{\rm C}$, across a (variable) load modeled by resistance $R_{\rm load}$. (See Fig. 1.) The DAACC regulates $v_{\rm C}$ to a desired reference voltage, $v_{\rm ref}$,

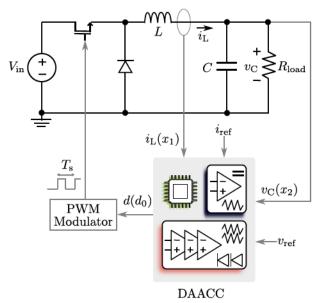


Fig. 1: A DC-DC buck converter with a DAACC implementing MPC. The goal is to enforce constraints $i_{\rm L} \leq I_{\rm max}$ (to avoid inductor saturation and limit switch current) and $d_{\rm min} \leq d \leq d_{\rm max}$ while regulating $v_{\rm C}$ to $v_{\rm ref}$.

by computing a control input duty cycle, d. The continuous-time dynamics of the buck converter are governed by state-space equations given in (1) [29]. The state variables, inductor current and capacitor voltage, are represented as $x = \begin{bmatrix} x_1 & x_2 \end{bmatrix}^\top = \begin{bmatrix} i_L & v_C \end{bmatrix}^\top$. The control input u = d is used to regulate the converter output voltage. System dynamics can be expressed in state-space form

$$\dot{x} = A_{c}x + B_{c}u, \quad y = C_{c}x, \tag{1}$$

where:

$$A_{\rm c} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{R_{\rm load}C} \end{bmatrix}, \ B_{\rm c} = \begin{bmatrix} \frac{V_{\rm in}}{L} \\ 0 \end{bmatrix}, \ C_{\rm c} = \begin{bmatrix} 0 & 1 \end{bmatrix}.$$

B. MPC Problem Formulation

We consider an MPC formulation that minimizes a quadratic objective function f over a finite prediction horizon, N, with constraints on states and control inputs: [30], [31]

$$\min_{\substack{d_{0}, d_{1}, \dots, d_{N-1} \\ x_{1}, x_{2}, \dots, x_{N-1}}} f = \sum_{k=1}^{N-1} (x_{\text{ref}} - x_{k})^{\top} Q (x_{\text{ref}} - x_{k}) + \sum_{k=0}^{N-1} d_{k}^{\top} R d_{k},$$
 (2a)

s.t.
$$x_{k+1} = A_{\mathrm{d}}x_k + B_{\mathrm{d}}d_k$$
, $\forall k = 0, \dots, N-1$, (2b) $x_{\min} \le x_k \le x_{\max}$, $\forall k = 1, \dots, N-1$, (2c) $d_{\min} < d_k < d_{\max}$, $\forall k = 0, \dots, N-1$, (2d)

where $x_{\text{ref}} = \begin{bmatrix} i_{\text{ref}} & v_{\text{ref}} \end{bmatrix}^{\top}$ is the reference state, and the duty cycles over the horizon, d_k 's are the optimization variables. The state of the system at the k+1-st instant, x_{k+1} , is predicted using the current state x_k , and the control input

 d_k by discretizing the dynamics (1) using a zeroth-order hold. Symmetric weighting matrices $Q \succeq 0$ and $R \succ 0$ are tuned for desired closed-loop performance. The limits on state variable values are given by x_{\min} and x_{\max} , while the bounds on control input d_k are given by d_{\min} and d_{\max} . The problem is solved in each sampling period (which is equal to the switching period in our case), T_s , with initial state measurement, x_0 , and the duty cycle, d_s , is set to be the optimizer d_0^* . Matrices A_d , B_d are obtained through the discretization of the continuous system dynamics (1) over T_s :

$$A_{\mathrm{d}} = \mathrm{e}^{A_{\mathrm{c}}T_{\mathrm{s}}}, \quad B_{\mathrm{d}} = \left(\int_{ au=0}^{T_{\mathrm{s}}} \mathrm{e}^{A_{\mathrm{c}} au} \mathrm{d} au\right) B_{\mathrm{c}}.$$

C. MPC with Terminal Cost for Stability

Unlike the stability properties of infinite-horizon linear quadratic regulator (LQR), in finite-horizon MPC, ensuring stability—convergence of the solution to the optimization problem—requires careful design of the objective function, prediction horizon, and constraints [30], [31]. To promote the stability of the MPC formulation, a terminal cost term, $(x_{\text{ref}} - x_N)^{\top} P(x_{\text{ref}} - x_N)$, can be added to the objective function (2a) of the optimization problem in (2) to approximate the infinite-horizon LQR behavior. The modified objective function becomes: [30], [31]

$$\min_{\substack{d_0, d_1, \dots, d_{N-1} \\ x_1, x_2, \dots, x_N}} f = \sum_{k=1}^{N-1} (x_{\text{ref}} - x_k)^\top Q (x_{\text{ref}} - x_k) + \sum_{k=0}^{N-1} d_k^\top R d_k + (x_{\text{ref}} - x_N)^\top P (x_{\text{ref}} - x_N).$$
(3)

The constraints remain the same as in (2b), (2c), and (2d). The matrix P is determined from the discrete algebraic Riccati equation: [31]

$$P = Q + A_{\mathbf{d}}^{\top} P A_{\mathbf{d}}$$

$$- \left(A_{\mathbf{d}}^{\top} P B_{\mathbf{d}} \right) \left(R + B_{\mathbf{d}}^{\top} P B_{\mathbf{d}} \right)^{-1} \left(B_{\mathbf{d}}^{\top} P A_{\mathbf{d}} \right).$$

$$(4)$$

While we focus on a quadratic objective function, it is worth noting that simpler objective functions (e.g., $\|\cdot\|_1$ norm) are used to reduce the computational burden in fast-dynamic power electronic systems [2]. These alternatives often trade off closed-loop performance for faster computation.

III. SYNTHESIS OF THE DIGITALLY ASSISTED ANALOG COMPUTING CIRCUIT (DAACC) FOR MPC

This section presents the design of a Digitally Assisted Analog Computing Circuit (DAACC) implementing the MPC problem from Section II. We transform the MPC problem in terms of control variables, reformulate it using the penalty method to handle constraints, and describe the DAACC implementation using gradient-flow dynamics for a real-time solution.

A. Transformation of MPC Problem

To implement the MPC problem using a DAACC, the problem is first transformed so that the objective function only features the control variables, d_k [30]. This transformation eliminates the need for explicit state prediction in the circuit implementation. It is achieved by using the discrete-time statespace solution to the equality constraint (2b), which expresses the current state, x_k , in terms of the initial measured state, x_0 , and the sequence of control inputs, d_k , $\forall k = 1, \ldots, N$:

$$x_k = A_{\rm d}^k x_0 + \sum_{j=0}^{k-1} A_{\rm d}^{k-j-1} B_{\rm d} d_j.$$
 (5)

Substituting (5) into the objective function f from (2a) and constraints from (2c), we obtain a transformed MPC problem that depends only on the control variables d_k :

$$\min_{d_0, d_1, \dots, d_{N-1}} \widetilde{f} = \sum_{k=1}^{N-1} (x_{\text{ref}} - (A_{\mathbf{d}}^k x_0 + \sum_{j=0}^{k-1} A_{\mathbf{d}}^{k-j-1} B_{\mathbf{d}} d_j))^{\top} Q$$

$$(x_{\text{ref}} - (A_{\mathbf{d}}^k x_0 + \sum_{j=0}^{k-1} A_{\mathbf{d}}^{k-j-1} B_{\mathbf{d}} d_j)) + \sum_{k=0}^{N-1} d_k^{\top} R d_k, \qquad (6a)$$
s.t.
$$x_{\min} \le A_{\mathbf{d}}^k x_0 + \sum_{j=0}^{k-1} A_{\mathbf{d}}^{k-j-1} B_{\mathbf{d}} d_j \le x_{\max}, \qquad \forall k = 1, \dots, N, \qquad (6b)$$

$$d_{\min} \le d_k \le d_{\max}, \quad \forall k = 0, \dots, N-1. \qquad (6c)$$

Notice that the equality constraint (2b) is eliminated from the original MPC problem (2), as the system dynamics are now directly represented in the objective function and inequality constraints on the state.

B. Penalty-based Reformulation of the MPC Problem

To solve the constrained optimization problem in (6) using a DAACC, we further reformulate it into an unconstrained problem using the penalty method [5]. This is accomplished by penalizing inequality constraint violations via a penalty function $\phi: \mathbb{R} \to \mathbb{R}$. The problem then boils down to:

$$\min_{d \in \mathbb{R}^N} \widetilde{f} + \frac{\rho}{2} \phi, \tag{7}$$

where

$$\begin{split} \phi &= \sum_{k=1}^{N-1} \left(\left(\min(0, A_{\mathrm{d}}^k x_0 + \sum_{j=0}^{k-1} A_{\mathrm{d}}^{k-j-1} B_{\mathrm{d}} d_j - x_{\min}) \right)^2 \\ &+ \left(\min(0, x_{\max} - (A_{\mathrm{d}}^k x_0 + \sum_{j=0}^{k-1} A_{\mathrm{d}}^{k-j-1} B_{\mathrm{d}} d_j)) \right)^2 \right) \\ &+ \sum_{k=0}^{N-1} \left(\left(\min(0, d_k - d_{\min}) \right)^2 + \left(\min(0, d_{\max} - d_k) \right)^2 \right). \end{split}$$

The inequality constraints are implicitly handled through the penalty function, ϕ , which, in our implementation, is a sum of quadratic forms $(\min(\cdot,\cdot))^2$. The quadratic form ensures that the penalty is zero when the constraint is satisfied and

increases quadratically with the magnitude of the violation. A penalty parameter $\rho \in \mathbb{R}_{>0}$ determines the extent of the constraint violation applied and is selected such that $\frac{\rho}{2}\phi\gg 0$. Sufficiently large values ensure that the solution to (7) closely approximates the solution to the original constrained problem in (2). This penalty-based reformulation allows us to solve the MPC problem using gradient-based methods, which can be implemented using DAACC. The following subsection will detail the DAACC implementation based on gradient-flow dynamics to solve this reformulated problem in real-time.

C. DAACC Based on Gradient-flow Dynamics

The reformulated unconstrained problem is solved by applying the following continuous-time gradient-flow dynamics for all d_k , k = 0, ..., N - 1:

$$\frac{\mathrm{d}d_k}{\mathrm{d}t} = -\gamma \left(\frac{\partial \widetilde{f}}{\partial d_k} + \frac{\rho}{2} \frac{\partial \phi}{\partial d_k} \right),\tag{8}$$

where $\gamma \in \mathbb{R}_{>0}$ is a constant, $\frac{\partial \widetilde{f}}{\partial d_k}$ is the gradient of the function $\widetilde{f}(\cdot)$, and $\frac{\partial \phi}{\partial d_k}$ is the gradient of the penalty function $\phi(\cdot)$ given by:

$$\frac{\partial \tilde{f}}{\partial d_{k}} = 2Rd_{k} - 2\sum_{\ell=k+1}^{N-1} (x_{\text{ref}} - x_{\ell})^{\top} Q A_{\text{d}}^{\ell-k-1} B_{\text{d}}
- 2(x_{\text{ref}} - x_{N})^{\top} P A_{\text{d}}^{N-k-1} B_{\text{d}}, \tag{9}$$

$$\frac{\partial \phi}{\partial d_{k}} = 2B_{\text{d}} (\min(0, x_{k+1} - x_{\min}) - \min(0, x_{\max} - x_{k+1}))
+ 2(\min(0, d_{k} - d_{\min}) - \min(0, d_{\max} - d_{k})). \tag{10}$$

The circuits in Fig. 2 show the proposed DAACC implementing dynamics (8) for prediction horizons N=1 with terminal cost term $(P \neq 0)$, N=2, and N=3 without terminal cost term (P=0) respectively. To keep the circuit size low, we enforce the inductor current constraint only at the first prediction step. The circuit realization relates to the dynamics (8) via the parametric relationship:

$$\gamma = \frac{1}{R_{\gamma}C_{\gamma}}, \quad \rho = \frac{R_{\rho}}{R_{\circ}}.$$

Analog Subsystem: The terms in $\frac{\rho}{2} \frac{\partial \phi}{\partial d_k}$ are implemented via an analog circuit consisting of op-amps, diodes, and resistors. Inputs to the analog circuit stage are either constants (such as I_{\max} , d_{\max} , d_{\min}) or derived from inverting op-amp stages (not shown in the Fig. 2) that linearly manipulate voltages such as $A_{d_{11}}i_L$, $A_{d_{12}}v_C$, $B_{d_{11}}d_0$, where the subscripts denote the respective elements of matrices A_d and B_d (e.g., $A_{d_{11}}$ is the (1,1) element of matrix A_d). High-gain inverting amplifiers with a gain (R_{ρ}/R_{\circ}) , then, impose significant penalties (ρ) to constrain d and i_L within bounds. The $\min(\cdot,\cdot)$ function is realized using an op-amp paired with a diode, where R_{\lim} restricts current flowing through the op-amp output terminal and associated diode. Unity-gain buffer follows the $\min(\cdot,\cdot)$ function stage to provide sufficient buffering. Finally, we incorporate an inverting amplifier, which provides a gain $(R_{\ell,k}/R_{\circ})$ equivalent to scalar term in $\frac{\partial \phi}{\partial d_k}$ (such as B_d),

where ℓ denotes the specific constraint and k the prediction step.

Digital Subsystem: Terms in $\frac{\partial \tilde{f}}{\partial d_k}$ can be generated by a digital circuit, such as a Field-Programmable Gate Array (FPGA) or digital microcontroller.

The analog integrators, each composed of a capacitor C_{γ} and resistor R_{γ} , sum the output from the digital circuit generating $\frac{\partial \tilde{f}}{\partial d_k}$ and the analog circuit implementing $\frac{R_{\rho}}{R_0}\frac{\partial \phi}{\partial d_k}$ to produce the sequence of optimal duty cycles d_k^{\star} of which, d_0^{\star} is applied as the duty cycle for the subsequent sampling (switching) period.

IV. PERFORMANCE VALIDATION

This section presents simulation results for the proposed DAACC implementing MPC for a buck converter, followed by a comparative analysis with conventional control methods and numerical optimization techniques.

A. DAACC Simulation Results

The proposed DAACC circuit implementing MPC for a buck converter, shown in Fig. 2, is simulated using the LTspice circuit simulator. The buck converter parameters used in our simulations are listed in Table I. The digital circuit is implemented using behavioral sources with its outputs limited to ± 5 V. In these LTspice simulations, we have assumed instantaneous output from the digital circuit without delay. However, it is important to note that digital delays can introduce instability depending on time delay values [15], [28], [32]. The analog circuit implementing $\frac{R_\rho}{R_\odot} \frac{\partial \phi}{\partial d_k}$ terms and integrators, utilizes AD8039 op-amps chosen for their high speed (350 MHz bandwidth) and high slew rate (425 V/ μ s). The analog circuit uses a high gain $(R_\rho/R_\odot=100)$ to implement large penalties (ρ) for constraint handling, with its outputs limited to ± 12 V.

The MPC formulation uses weighting matrices $Q \succeq 0$ and $R \succ 0$ selected as follows:

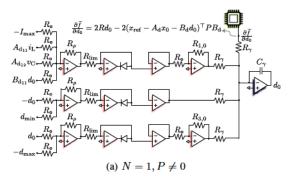
$$Q = \begin{bmatrix} 0 & 0 \\ 0 & 10^3 \end{bmatrix}, \quad R = 1. \tag{11}$$

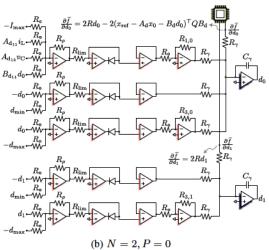
These values are chosen to prioritize output voltage regulation while moderating control efforts. Additionally, the zero elements in Q reduce computational complexity by simplifying the calculation of terms in $\frac{\partial \tilde{f}}{\partial d_a}$.

All results are reported in Figs. 3a, 3b, and 3c and described subsequently. The output (capacitor) voltage $v_{\rm C}$ aligns with the reference voltage $v_{\rm ref}$ of 5 V at start-up. Subsequently, $v_{\rm ref}$ is step changed to 10 V at time t=0.2 ms, and $v_{\rm C}$

TABLE I: Buck Converter Parameters

Parameter	Value
Input voltage, $V_{\rm in}$	48 V
Inductor, L	$30 \mu H$
Capacitor, C	$10 \mu F$
Load resistance, R_{load}	$10~\Omega$
Switching period, $T_{ m s}$	$1 \mu s$





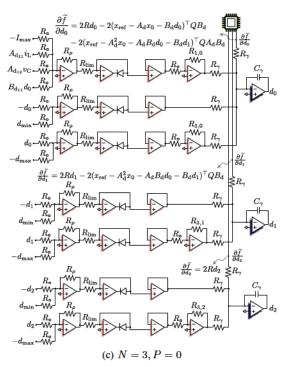


Fig. 2: Circuit implementation of the DAACC solving the MPC problem. The circuit enforces constraints $i_{\rm L} \leq I_{\rm max}$ and $d_{\rm min} \leq d \leq d_{\rm max}$. The circuit component values are $R_{\rm o} = R_{\rm lim} = R_{3,0} = R_{3,1} = R_{3,2} = R_{\gamma} = 10~{\rm k}\Omega$, $R_{1,0} = B_{\rm d_{11}}R_{\rm o}$, $R_{\rho} = 1~{\rm M}\Omega$, and $C_{\gamma} = 1~{\rm nF}$.

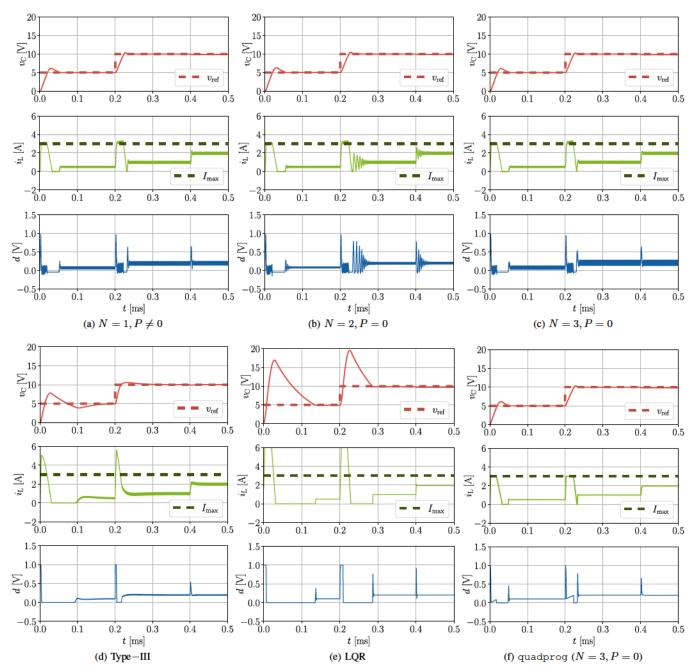


Fig. 3: Simulation results for the buck converter controlled by: (a),(b),(c) the proposed DAACC using MPC with different prediction horizons (switched-model simulation), compared with (d) Type-III controller (switched-model simulation), (e) LQR (averaged-model simulation), and (f) MATLAB's quadprog solver (averaged-model simulation).

settles within approximately 50 μ s. The DAACC maintains the state constraints to limit the inductor current $i_{\rm L} \leq 3$ A, which significantly reduces overshoot in $v_{\rm C}$. The $v_{\rm C}$ regulation for a step change in $R_{\rm load}$ from 10 Ω to 5 Ω carried out at t=0.4 ms is also depicted in Figs. 3a, 3b, and 3c.

The dynamic response of the buck converter improves with an increasing prediction horizon N=2 to N=3 without terminal cost term (P=0), as seen in Figs. 3b and 3c, although

with the trade-off of an increased circuit size. Furthermore, the effect of including a terminal cost is demonstrated in Fig. 3a, which shows the case where $N=1, P\neq 0$, corresponding to the objective function in (3), which includes the terminal cost term. Here, P is computed using the discrete algebraic Riccati equation (4). This achieves a better dynamic response compared to the higher prediction horizon case of N=2, P=0 shown in Fig. 3b, which corresponds to the

objective function in (2a) without the terminal cost term.

As N increases, although dynamic response improves, the number of analog components grows linearly. Assuming that the bounds on $i_{\rm L}$ are implemented at the start of the prediction horizon, there is an increase of approximately 8 op-amps per prediction horizon. Moreover, the computation in the digital circuit increases, resulting in a longer computational delay.

B. Comparative Analysis

We compare the DAACC-based MPC with a third-order Type-III controller (Fig. 3d) and discrete LQR (Fig. 3e). Type-III controller can be viewed as a proportional-integral-derivative (PID) controller with a second-order lag [33]. The transfer function G(s) of a Type-III controller is:

$$G(s) = G_0 \frac{(1+s/\omega_{\rm z_1})(1+s/\omega_{\rm z_2})}{s(1+s/\omega_{\rm p_1})(1+s/\omega_{\rm p_2})}, \label{eq:Gs}$$

where $G_0=1.2\times 10^4$ is the controller gain, $\omega_{z_1}=5.1\times 10^4$ rad/s and $\omega_{z_2}=5.7\times 10^4$ rad/s are the angular frequencies of the zeros, and $\omega_{p_1}=3.3\times 10^6$ rad/s and $\omega_{p_2}=3.6\times 10^6$ rad/s are the angular frequencies of the poles. These parameters are designed using MATLAB's sisotool to provide a gain margin of 20 dB and a phase margin of 60° at 102 kHz. This s-domain transfer function is simulated in a closed loop with the buck converter using Plexim's PLECS simulator. Note that simulating the Type-III controller with op-amp can introduce additional limitations that further degrade performance compared to the s-domain simulation.

The LQR control minimizes a quadratic objective function J over an infinite horizon, given as: [31]

$$J = \sum_{k=0}^{\infty} \left(\left(x_{\text{ref}} - x_k \right)^{\top} Q \left(x_{\text{ref}} - x_k \right) + d_k^{\top} R d_k \right),$$

where $d_k = K(x_{ref} - x_k)$ is the control input that minimizes J. The gain matrix K is computed in MATLAB as:

$$K = (R + B_{\mathrm{d}}^{\top} P B_{\mathrm{d}})^{-1} (B_{\mathrm{d}}^{\top} P A_{\mathrm{d}}) = \begin{bmatrix} 0.96 & 7.28 \end{bmatrix}$$

where P satisfies the algebraic Riccati equation given by (4). The matrices Q and R for discrete LQR control are the same as that for MPC, as given by (11). This discrete LQR controller is simulated using MATLAB in a closed loop with the buck converter.

As shown in Fig. 3, the DAACC-based MPC achieves faster settling time with a lower overshoot in the output voltage $v_{\rm C}$ while limiting $i_{\rm L}$. In contrast, both the Type-III controller and LQR lack inherent structure for constraining $i_{\rm L}$ (which leads to overshoots in $v_{\rm C}$). Furthermore, while DAACC-based MPC directly incorporates control input d constraints within its formulation, the conventional Type-III controller and LQR require external limiting for d. However, these traditional controllers have the advantage of lower computational complexity.

To validate the optimality of our proposed DAACC approach, we compare the DAACC case of N=3, P=0 in Fig. 3c with an equivalent MPC implementation using MATLAB's quadprog solver in Fig. 3f, which employs

an interior-point-convex algorithm. The quadprog solver returns the global optimal solution of the convex quadratic problem and serves as a benchmark for our DAACC implementation. The dynamic response obtained from MATLAB's quadprog solver closely aligns with that of the DAACC implementing penalty-based gradient-flow dynamics (Fig. 3c). This similarity in response indicates that both methods converge to comparable optimal solutions. However, while MATLAB's quadprog solver faces real-time implementation challenges, the DAACC-based MPC is designed for real-time application in fast dynamic power converters.

V. CONCLUSIONS

This paper presents a digitally assisted analog computing circuit (DAACC) for real-time MPC applied to a DC-DC buck converter. The proposed DAACC yields a fast dynamic response with minimal overshoots in the output voltage while maintaining limits on the inductor current and duty cycle. The DAACC outperforms conventional Type-III and LQR controllers in dynamic response and constraint handling. In addition, while achieving performance comparable to MAT-LAB's quadprog solver, the DAACC-based MPC enables real-time implementation for power converters with rapid dynamics.

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