

Monolayer hBN RRAM with High DC Endurance and Low Operation Voltages using an Oxidized Top Electrode

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The rapid evolution of artificial intelligence technologies has escalated the need for compact, high-density memory solutions [1]. Monolayer hexagonal boron nitride resistive random access memory (ML hBN RRAM) emerges as a particularly promising candidate due to its simple, ultra-thin metal-insulator-metal structure. However, these atomristor devices usually wear out quickly, with a maximum of 100 DC linear sweeps reported in existing studies [2]. Our research has led to a groundbreaking enhancement: by integrating a conductive oxidized metal top electrode into monolayer hBN RRAM, we have significantly extended its durability, achieving over 2000 cycles at low operational voltages below 0.5 V. These devices also have demonstrated the ability to endure up to continuous 400 cycles under μs pulse voltage, and even more pulse cycles by reactivating them by DC sweeps. This is the first time monolayer 2D material RRAM has exhibited such a high number of DC cycles and shows the potential for higher pulse-operated endurance and future energy-efficient computing applications.

Fig. 1. shows an optical microscope image of the crossbar RRAM, with layers Ag(50 nm)/Pt(5 nm)/monolayer hBN/oxidized metal (80 nm) composed of e-beam evaporated electrodes and wet-transferred CVD monolayer hBN. The scratch on the right pad reveals that the metal on top is thoroughly oxidized, both inside and outside. Fig. 2 shows the first four DC sweeps of the ML hBN RRAM, which was in slightly low resistance state in the first sweep, and then reset to high resistance state (HRS) by the second DC sweep. The 3rd and 4th DC sweeps were within $V_{\text{stop}} = 0.3 \text{ V}$ and -0.6 V . Fig. 3(a) shows the 1st to 100th set and reset cycles after obtaining Fig. 2, and Fig. 3(b) is the 1901st to 2000th cycles. The red dashed lines mark the range of V_{set} and the green dashed lines mark the range of V_{reset} . It is observed that the variance of V_{set} and V_{reset} becomes lower in later cycles, which implies that the device settles with subsequent less wear out. It is important to note that after 2000 DC cycles, the device still operates. V_{set} and V_{reset} are both smaller than 0.3 V, and V_{stop} is at maximum 0.5 V, which are very low operating voltages showing an energy-efficient memory device.

We also apply pulse voltages for setting and resetting the ML hBN RRAM. The real-time current and voltage curves are shown in Fig. 4. Here, slightly higher set and reset voltages ($V_{\text{set}} = 0.6 \text{ V}$, $V_{\text{reset}} = -1 \text{ V}$) are used due to the ultrasmall pulse period (total pulse period = 3 μs). The details of the pulse voltages are shown in Fig. 5, and the resistance values of 400 continuous pulse cycles are shown in Fig. 6. The range of low resistance state (LRS) and HRS are indicated by the red and green shading, respectively, and the HRS/LRS ratio for each cycle is at least 20. After these 400 continuous cycles, the device was kept in HRS in the following pulse sweeps. After applying a few DC sweeps in the same voltage condition of Fig. 3(a) and Fig. 3(b), the device was reactivated again and was able to be set and reset by pulse operations.

In summary, we use an oxidized top electrode to demonstrate, for the first time, over 2000 DC cycles of ML hBN RRAM and 400 continuous pulsed cycles, with the devices continuing to be operational after testing. The ML hBN RRAM shows low operation voltages below 0.5 V. These results show atomristors have a path to overcome endurance challenges to create ultra-scaled RRAM for memory and neuromorphic computing.

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References:

- [1] Piergiulio Mannocci, *et al.*, "In-memory computing with emerging memory devices: Status and outlook," Virtual Community of Pathological Anatomy (University of Castilla La Mancha), vol. 1, no. 1, Feb. 2023, doi: <https://doi.org/10.1063/5.0136403>
- [2] J. Xie, S. Afshari, and I. Sanchez Esqueda, "Hexagonal boron nitride (h-BN) memristor arrays for analog-based machine learning hardware," npj 2D Materials and Applications, vol. 6, no. 1, Jul. 2022, doi: <https://doi.org/10.1038/s41699-022-00328-2>

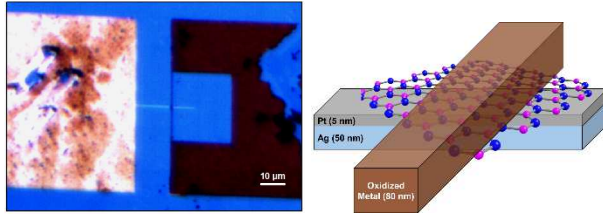


Fig. 1. Optical microscopic image and the illustration of the Ag/Pt/monolayer hBN/oxidized metal crossbar RRAM. The overlapped area is smaller than $1 \times 1 \mu\text{m}^2$.

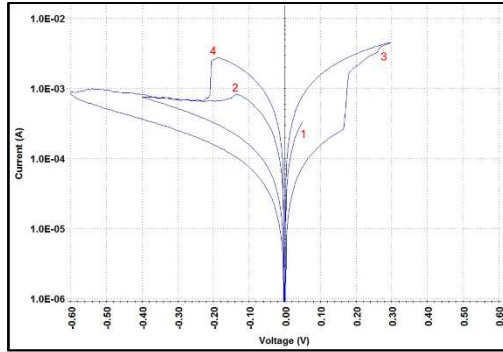
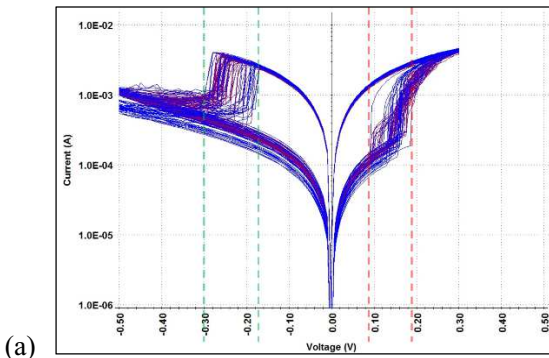
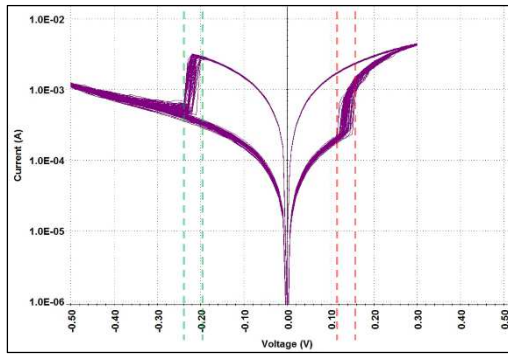


Fig. 2. The first four DC sweeps of the ML hBN RRAM. $V_{\text{stop}} = 0.05 \text{ V}, -0.4 \text{ V}, 0.3 \text{ V}$ and -0.6 V .



(a)



(b)

Fig. 3 (a) The first 100th and (b) the 1901st-2000th set and reset DC sweeps within $V_{\text{stop}} = 0.3 \text{ V}$ and -0.5 V . The dash lines show the range of V_{set} and V_{reset} .

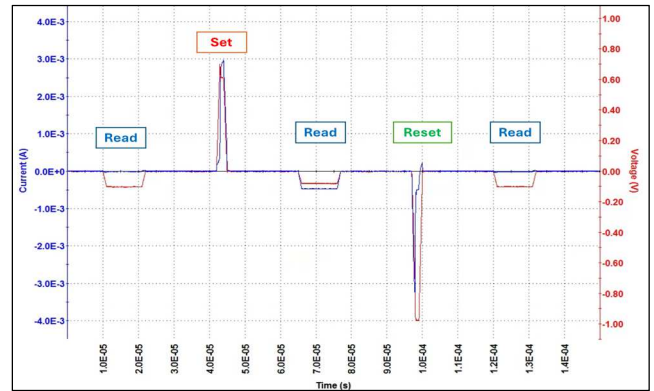


Fig. 4. (a) Real-time current-voltage curves of the pulse cycles.

Read pulse rise/fall time	1 μs
Read pulse voltage	-0.1 V
Read pulse width	10 μs
Set pulse rise/fall time	1 μs
Set pulse voltage	0.6 V
Set pulse width	1 μs
Reset pulse rise/fall time	1 μs
Reset pulse voltage	-1 V
Reset pulse width	1 μs

Fig. 5. The parameters of the pulse operation in Fig.4.

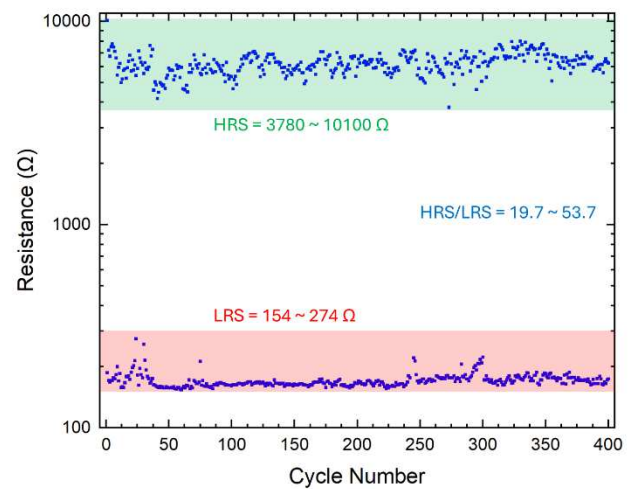


Fig.6 $\text{HRS}_{\text{pulse}}$ and $\text{LRS}_{\text{pulse}}$ for continuous 400 pulse cycles showing HRS range, LRS range, and HRS/LRS.