A Fractional Spur Cancellation Technique for Fractional-N Frequency Synthesizers Enabled by Dual Loop Phase Clamping

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***Abstract*—A fractional spur cancellation technique for fractional-N frequency synthesizers is presented in this paper. A time domain quantitative analysis is performed to obtain an intuitive understanding of the origin of fractional spurs. By utilizing a dual loop architecture that generates two feedback phases leading and lagging to the reference phase, respectively, the proposed technique can clamp the reference phase in the middle of the two feedback phases, and realize the spur cancellation after combining the complementary outputs of the two charge pumps. Simulation results demonstrate that the proposed technique can improve the worst-case fractional spur level by more than 50dB.**

Keywords—fractional-N frequency synthesizer, fractional spur cancellation, dual loop, phase clamping

I. Introduction

Emerging wireless communication services make the wireless frequency band a scarce resource. The overcrowded frequency bands have motivated people to make a more efficient use of the available spectrum resource, which usually means higher data rate and higher order modulation schemes [1-3]. This has set extremely challenging requirements on the linearity and signal-to-noise performance of the wireless communication systems. The frequency synthesizer, also named as the phase-locked loop (PLL), is one of, if not the most critical building blocks since it is dictating the performance boundary of every clocked building block, and its effect is very difficult to remove after the clock generation. Recent trend has shown a growing interest in architectures based on digital-to-time-converter (DTC) [4-7]. Adoption of DTC can enable more signal processing, thus ideally better performance of the PLL, however, not only it will increase the system complexity, but also the DTC' nonidealities should be addressed properly, otherwise it will be translated into PLL's output nonidealities, making the DTC based techniques less effective. This paper will explore a pure analog methodology that can effectively suppress the fractional spurs in a fractional-N frequency synthesizer with minimum system complexity overhead and no extra processing stages in the signal path.

II. System Architecture

A. Spurs in Fractional-N Frequency Synthesizers

Fig. 1(a) shows the system diagram of a conventional charge-pump fractional-N frequency synthesizer. To analyze the fractional spurs in time domain, we can look at the timing diagram of the reference signal and feedback signal, which is shown in Fig. 1(b). The timing of the n-th rising edge of the reference and feedback signal can be given by

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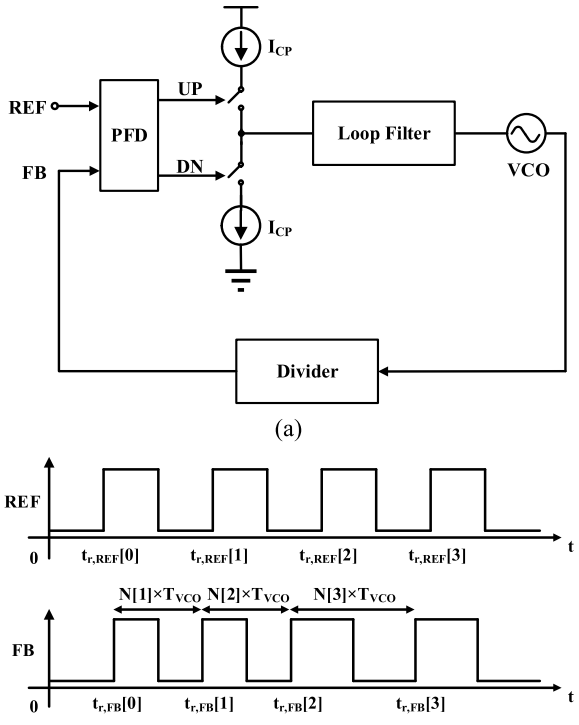


Fig. 1. (a) System diagram, and (b) timing diagram of a conventional charge-pump fractional-N frequency synthesizer.

$$\begin{cases} t_{r,REF}[n] = t_{r,REF}[0] + nT_{REF} \\ t_{r,FB}[n] = t_{r,FB}[0] + \sum_{i=1}^{n} N[i]\,T_{VCO} \end{cases} \quad (1)$$

, where T_{REF} and T_{VCO} are the periods of the reference signal and the voltage-controlled oscillator's (VCO) output, respectively, and $N[i]$ is the division ratio of the i-th reference clock cycle.

The phase detector will find the time difference between the adjacent rising edges of the two signals, which can be expressed as

$$\begin{aligned} \Delta t[n] &= t_{r,REF}[n] - t_{r,FB}[n] \\ &= \Delta t[0] + n\left(T_{REF} - N_{eq}T_{VCO}\right) \\ &\quad - \sum_{i=1}^{n}\left(N[i] - N_{eq}\right)T_{VCO} \end{aligned} \quad (2)$$

, where N_{eq} is the equivalent division ratio of the fractional divider. So, the output of the phase detector consists of two parts: 1) the first two terms in (2) represent the ideal feedback signal; 2) the third term in (2) is the error due to mimicking the fractional division with integer divisions, which is the main culprit of the fractional spurs in the PLL.

In the steady-state, the VCO's oscillation frequency is locked with the reference signal, i.e., $T_{REF} = N_{eq}T_{VCO}$, then (2) will become

$$\Delta t[n] = \Delta t[0] - \sum_{i=1}^{n} \big(N[i] - N_{eq}\big)\, T_{VCO}. \qquad (3)$$

This time difference Δt will then be converted to charge by the charge pump, and injected into the loop filter, which has the expression of

$$Q_{CP}[n] = I_{CP} \times \Delta t[n]. \qquad (4)$$

Ideally, to get a clean spectrum for the VCO output, we would like $Q_{CP}[n]$ to remain zero so that there will be no fluctuation in the control voltage of the VCO. However, in the case that N_{eq} is a fractional number, since $N[i]$ can only be integer numbers, then unavoidably $Q_{CP}[n]$ will mostly be non-zero values, unless we can somehow inject another charge with the value of $-Q_{CP}[n]$ to cancel it, which is the main idea of the proposed architecture.

B. Proposed Dual Loop Fractional-N PLL

According to the previous discussion, we would like to develop a new PLL architecture that can achieve two targets:

1) The effect of non-zero charge $Q_{CP}[n]$ will be cancelled out by injecting another charge $-Q_{CP}[n]$.
2) Such cancellation should only be applied to the components causing fractional spurs, but not affecting the feedback signal from VCO's output.

Assuming $\Delta t[0] = 0$, this may not be true in a conventional PLL, but we will prove later in this section that this is valid for the proposed PLL. Then (4) can be updated with

$$Q_{CP}[n] = I_{CP} \times \sum_{i=1}^{n} \big(N[i] - N_{eq}\big)\, T_{VCO}. \qquad (5)$$

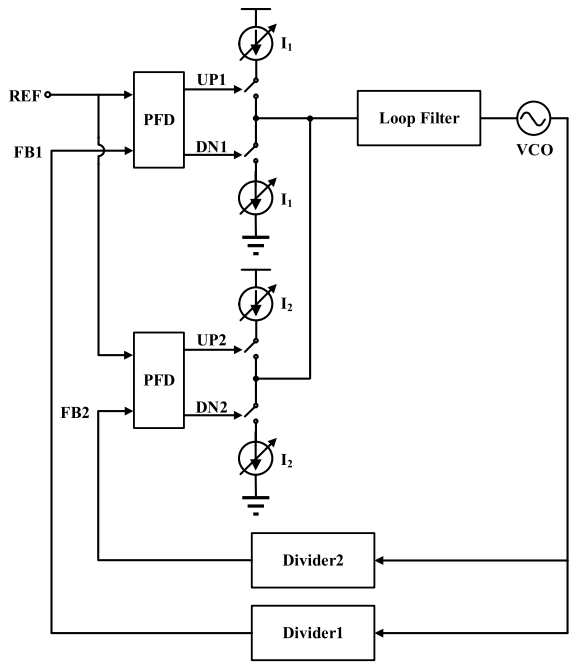
So, the value of $Q_{CP}[n]$ is somehow controllable by manipulating the array of $N[i]$. If we have two frequency dividers with different division ratios $N_1[i]$ and $N_2[i]$, which satisfy

$$\sum_{i=1}^{n} \big(N_1[i] - N_{eq}\big) \le 0 \le \sum_{i=1}^{n} \big(N_2[i] - N_{eq}\big) \qquad (6)$$

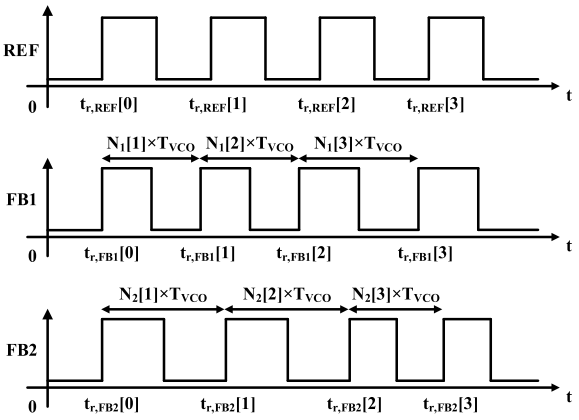
, then we can generate two charges with different polarities to cancel out each other.

To accommodate the two frequency dividers, two phase detectors and two charge pumps are also needed. Then the proposed dual loop Fractional-N PLL is shown in Fig. 2. The feedback loop will first be split into two separate paths by two frequency dividers, and then recombined by two charge pumps injecting charges into a shared loop filter.

Fig. 2(b) shows the timing diagram of the reference signal and the two feedback signals, which will all have the same frequency in the steady state. To quantitatively analyze the two loops, similar as (1), we can define



(a)



(b)

Fig. 2. (a) System diagram, and (b) timing diagram of the

$$\begin{cases} t_{r,REF}[n] = t_{r,REF}[0] + nT_{REF} \\ t_{r,FB1}[n] = t_{r,FB1}[0] + \sum_{i=1}^{n} N_1[i] \times T_{VCO} \\ t_{r,FB2}[n] = t_{r,FB2}[0] + \sum_{i=1}^{n} N_2[i] \times T_{VCO} \end{cases} \qquad (7)$$

, where $t_{r,FB1}[n]$ and $t_{r,FB2}[n]$ are the timing of the n-th rising edges of the two feedback signals.

The time differences between the rising edges of the reference signal and the two feedback signals, in the steady state, can be given by

$$\begin{cases} \Delta t_1[n] = \Delta t_1[0] - \sum_{i=1}^{n} \big(N_1[i] - N_{eq}\big) \times T_{VCO} \\ \Delta t_2[n] = \Delta t_2[0] - \sum_{i=1}^{n} \big(N_2[i] - N_{eq}\big) \times T_{VCO}. \end{cases} \qquad (8)$$

And the charge pumps will then convert the time differences to charges:

$$\begin{cases} Q_{CP1}[n] = I_1[n] \times \Delta t_1[n] \\ Q_{CP2}[n] = I_2[n] \times \Delta t_2[n] \end{cases} \quad (9)$$

, where $I_1[n]$ and $I_2[n]$ are the currents of the charge pumps. And the total charge injected into the loop filter is the summation of $Q_{CP1}[n]$ and $Q_{CP2}[n]$.

In order to have a zero net charge in each reference clock cycle, we would like $Q_{CP1}[n]$ and $Q_{CP2}[n]$ to be opposite numbers. Note that $I_1[n]$ and $I_2[n]$ must be non-negative values, so the only option is making $\Delta t_1[n]$ and $\Delta t_2[n]$ have the opposite polarities, which means one of the feedback signals will have a phase leading to the reference signal, while the other one lagging to the reference, or in other words, the two feedback signals will clamp the reference signal in the middle.

In addition to having opposite polarities, $Q_{CP1}[n]$ and $Q_{CP2}[n]$ should also have the same absolute value to completely cancel out each other. However, despite the special case that N_{eq} equals an integer number divided by 2, the ratio of $\Delta t_1[n]$ to $\Delta t_2[n]$ cannot be a constant value, then $I_1[n]$ and $I_2[n]$ must be programmable to make the summation of $Q_{CP1}[n]$ and $Q_{CP2}[n]$ always zero.

To simplify the control logic, we can let $\Delta t_1[0] = \Delta t_2[0] = 0$, which means that at the beginning of the first clock cycle, the two feedback signals are aligned (this is easy to achieve since the dividers are fully programmable), and the reference signal is also aligned with the feedback signals (the loop will automatically adjust the phases to make this happen, we will prove in the next paragraph that any case other than this is impossible in the steady state). Then, substitute (8) into (9), and make $Q_{CP}[n] = Q_{CP1}[n] + Q_{CP2}[n]$ be zero, we will obtain the conditions to cancel the fractional spurs:

$$\frac{I_1[n]}{I_2[n]} = -\frac{\sum_{i=1}^{n}\left(N_2[i] - N_{eq}\right)}{\sum_{i=1}^{n}\left(N_1[i] - N_{eq}\right)}. \quad (10)$$

And we will also keep $I_1[n] + I_2[n]$ constant at the same time, so that the loop dynamics will not be affected by manipulating the ratio between the two currents. In other words, when recombining the two loops, the signal components will have constructive combination, while the spurious components will have destructive combination.

Now let's think about what if $\Delta t_1[0] = \Delta t_2[0] = \Delta t[0]$ not equal to zero. Assume that I_1, I_2, N_1 and N_2 are assigned proper patterns to satisfy (10), then the total net charge injected into the loop filter will become

$$Q_{CP}[n] = (I_1[n] + I_2[n]) \times \Delta t[0]. \quad (11)$$

So, in the steady state, $\Delta t[0]$ must be zero since the average value of $Q_{CP}[n]$ should be zero.

III. Building Blocks

A. Phase Frequency Detectors

In the previous analysis, there is actually an implicit assumption on the phase detector that the phase detector will find the time difference between the most adjacent rising edges of the two input waveforms. However, this is not always true for a conventional flip-flop-based phase frequency detector (PFD). Fig. 3 shows the transfer curve and the potential bimodal issue of a conventional PFD. In this example timing diagram, the PFD has two potential

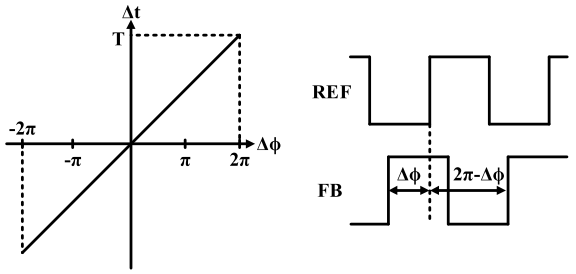
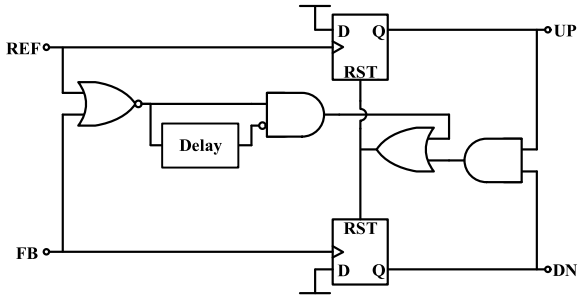


Fig. 3. Transfer curve and the potential bimodal issue of a conventional PFD.



working modes: 1) Define the feedback signal as the leading signal, and the resultant phase difference output will be $\Delta\phi$; 2) Define the reference signal as the leading signal, and the resultant phase difference output will be $2\pi - \Delta\phi$. Which mode the PFD will work in depends on the initial conditions.

This bimodal behavior of the PFD is not problematic in a conventional single loop PLL, since the transfer curve of the PFD, as shown in Fig. 3, is monotonic, so that the phase difference will finally converge to zero (or near zero) anyway. However, it may affect the functionality of the dual loop PLL. For example, the core of the dual loop is having one feedback signal leading to the reference signal, while the other one lagging, so that when recombining the two loops, the signal components will have constructive combination, while the spurious components will have destructive combination. But with the bimodal issue, it's possible that both PFDs define the feedback signal as the leading signal, then the spurious components will have constructive combination, and the signal components will have destructive combination.

To overcome this bimodal problem, an auxiliary circuitry is added to a conventional flip-flop-based PFD, as shown in Fig. 4. The working principle is that, when the both inputs of the phase detector are low, a positive pulse will be generated, and this pulse will be used to reset the flip-flops. This circuitry will be triggered whenever there is an input phase difference with an absolute value larger than π. The proposed PFD will then have a reduced input range of $[-\pi, \pi]$, instead of $[-2\pi, 2\pi]$, which is the origin of the bimodal issue.

B. Sampled Loop Filter

In the steady state, the charges injected by the two charge pumps will cancel each other in every cycle, however, due to the fact that one feedback signal is leading to the reference signal, and the other one is lagging, charge pumps are injecting charges at different timing, causing

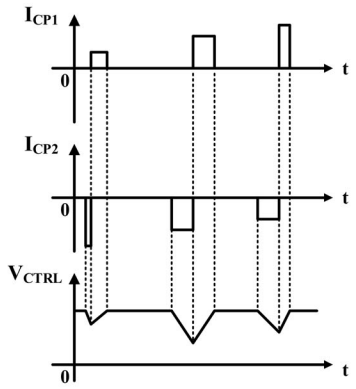


Fig. 5. Voltage fluctuations at the VCO's input due to charge pumps injecting charge at different timing.

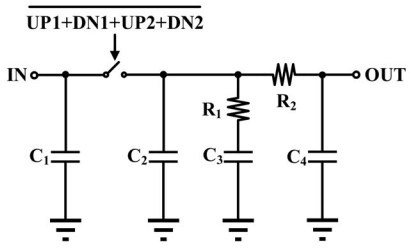


Fig. 6. Sampled loop filter.

TABLE I. SYSTEM PARAMETERS

f_{ref}	$31.25MHz$
$I_1 + I_2$	$100\mu A$
I_{LSB}	$\frac{I_1 + I_2}{2^8}$
C_1	$0.8pF$
C_2	$0.4pF$
C_3	$35pF$
C_4	$2pF$
R_1	$90K\Omega$
R_2	$4K\Omega$
K_{VCO}	$100\ MHz/V$
N_{eq}	$96 + \alpha, 0 < \alpha < 1$

voltage fluctuation at the VCO's input. See Fig. 5, I_{CP1} and I_{CP2} are the output currents of the two charge pumps, and V_{CTRL} is the VCO's input voltage. Since $\Delta t_1[n]$ and $\Delta t_2[n]$ are varying from cycle to cycle, then the shape of this voltage fluctuation will also vary, thus introducing fractional spurs to the VCO's output spectrum.

To protect the VCO's input from this voltage fluctuation, we can use a sampled loop filter as shown in Fig. 6, which was originally developed to remove the reference spurs [8]. The sampling capacitor C_1 will be disconnected from the rest of the loop filter when either of the two charge pumps is being activated, and will be reconnected when both charge pumps are deactivated. So C_1 will act like a charge buffer, first storing all the charges injected by charge pumps on C_1, then transferring the net charge to the rest of the loop filter. In the steady state, the net charge in every cycle will be zero, then the voltage across C_1 and also the VCO's input voltage will be a constant value.

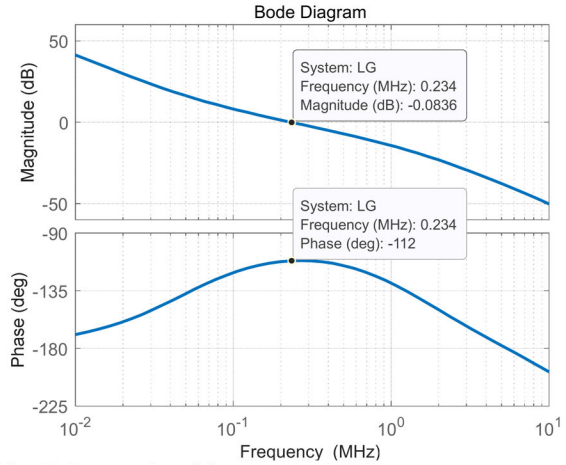


Fig. 7. Loop gain of the proposed PLL.

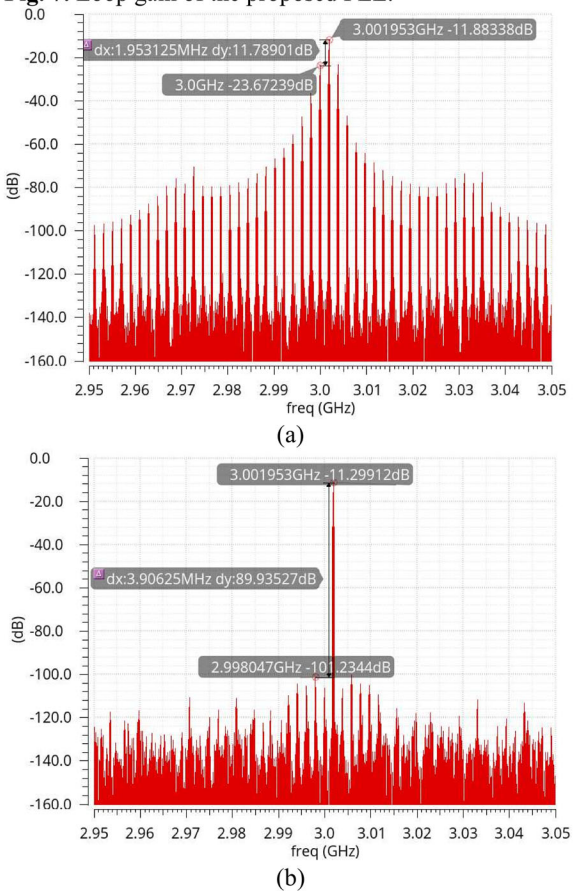


Fig. 8. VCO's output spectrum of (a) a conventional PLL, and (b) the proposed PLL.

IV. SIMULATION RESULTS

The proposed dual loop frequency synthesizer is designed in TSMC 40nm CMOS technology, with the system parameters shown in Table I, where f_{ref} is the reference clock frequency, I_{LSB} is the tunning resolution of the charge pumps, C_1, C_2, C_3, C_4, R_1 and R_2 are the components of the loop filter, K_{VCO} is the VCO's gain, and N_{eq} is the equivalent division ratio. The frequency response of the proposed PLL is shown in Fig. 7. The loop

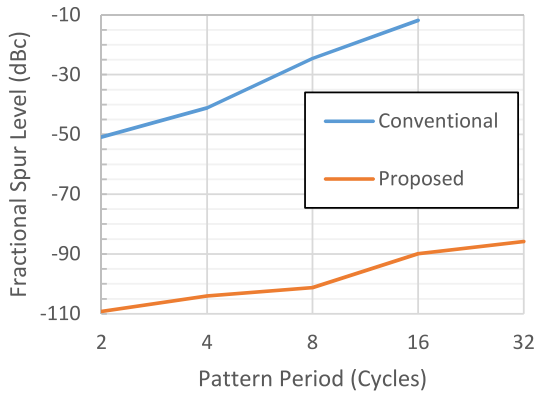


Fig. 9. Worst-case fractional spur level of the conventional and proposed PLLs with different division ratio pattern period.

bandwidth is around 230KHz, and the phase margin is around 68 degree.

To demonstrate the effectiveness of the proposed technology, the proposed PLL is compared with a conventional fractional-N PLL with the same system parameters. In this simulation, both PLLs have the same division ratio pattern with an average value of $N_{eq} = 96\frac{1}{16}$. The pattern period is 16 cycles, so that the fractional spurs will appear at the frequency of $\left(N_{eq} + \frac{k}{16}\right) \times f_{ref}, k \in \mathbb{Z}$. The VCO's output spectrum in both cases are shown in Fig. 8.

For the conventional PLL case, the worst-case fractional spur level is -11.8dBc. This spur level is excessive since the frequency offset from the carrier frequency is close to the loop bandwidth. For the proposed PLL case, the worst-case fractional spur level is -89.9dBc. The spur is significantly reduced by over 78dB.

Similar comparisons are done with different division ratio pattern periods. The results are summarized in Fig. 9. We are missing the case with a pattern period of 32 cycles for the conventional PLL, because in this case, the fractional spur is too close to the loop bandwidth, making the VCO's output of the conventional PLL a chirp signal instead of a fixed tone. As a comparison, the proposed PLL can work properly in this case, and have a worst-case fractional spur level of -85.8dBc. For all the other cases, the proposed technique can also significantly improve the fractional spur performance of a fractional-N PLL. The worst-case fractional spur level of the proposed PLL is always below -85dBc.

V. Conclusions

In this paper, we have presented a fractional spur cancellation technique for fractional-N frequency synthesizers. Enabled by complementary feedback loops and phase clamping, the proposed technique can elegantly cancel the effect of periodic division ratio patterns at the output of the loop filter without affecting the loop dynamics. The proposed technique also requires minimum system complexity overhead and no extra processing stages in the signal path, making it easy to design. Simulation results show that the proposed technique can effectively reduce the fractional spurs in VCO's output spectrum. The improvement of the worst-case fractional spur level can achieve more than 50dB for different division ratio patterns.

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