Gate Switching Lifetime of P-Gate GaN HEMT: Circuit Characterization and Generalized Model

Bixuan Wang
Center for Power Electronics Systems(CPES)
Virginia Tech
Blacksburg, USA
Email: bixuanwang@vt.edu

Qihao Song
CPES
Virginia Tech
Blacksburg, USA
Email: qihao95@vt.edu

Yuhao Zhang
CPES
Virginia Tech
Blacksburg, USA
Email: yhzhang@vt.edu

Abstract—**The gate reliability of p-gate GaN HEMTs is crucial for converter applications due to the narrow gate overvoltage margin. Despite many studies using DC bias and pulse I-V tests, the gate reliability under practical switching conditions remains inadequately addressed. Moreover, the unique electrostatics of the p-GaN gate challenge the applicability of the DC lifetime model to switching applications. This work develops a new circuit method to generate application-like gate voltage (V_G) stress, which comprises a resonant ringing added onto an operational DC bias. Using this circuit method, we characterize the gate lifetime of a commercial p-gate GaN HEMT under various V_G peak values ($V_{G(PK)}$), switching frequencies (f_{SW}), and temperatures (T). Subsequently, we derive $V_{G(PK)}$-, f_{SW}-, and T-related acceleration functions for gate degradation and further construct a gate switching lifetime model for p-gate GaN HEMTs for the first time. This model can directly derive the gate lifetime based on the V_G waveforms in application operations, as well as quantify the impacts of many parameters such as $V_{G(PK)}$, DC bias, f_{SW}, T, and duty cycle. This new circuit and lifetime model provide key references for the qualifications and applications of GaN power HEMTs.**

***Keywords*—GaN, HEMT, gate, spike, overvoltage, switching, reliability, lifetime, model**

I. INTRODUCTION

The GaN Schottky-type p-gate GaN HEMTs (SP-HEMTs) have gained popularity in power electronics applications, owing to their outstanding switching and conduction performance [1]. However, a critical concern in their applications is the narrow gate voltage (V_G) margin (1~2 V) between the typical driving voltage (5~6 V) and the suggested maximum allowable voltage (~7 V) [2], [3]. In power converters, the gate-loop parasitic inductance is very likely to induce V_G overshoots during the device turn-on transient due to its resonance with the device gate capacitance, resulting in a typical V_G profile consisting of a transient resonant ringing with an average slew rate (dV_G/dt) of 1~2 V/ns added onto an operational DC bias [Fig. 1(a)]. This gate overshoot typically become increasingly serious in high switching-frequencies (f_{SW}) operations, calling for an gate reliability evaluation of GaN SP-HEMTs for practical operations.

Unfortunately, current gate reliability tests of GaN HEMTs is primarily based on the DC bias [4], [5], [6], [7], [8], [9], [10] [Fig. 1(b)], which differs significantly from practical application conditions and cannot capture the device switching behaviors. Recently, the square-wave AC tests [Fig. 1(c)] performed using pulse current-voltage (I-V) system have been used to evaluate the gate lifetime, revealing the lifetime's strong dependencies on switching conditions [11], [12], [13]. However, the V_G slew rate of this method is still distinct from the practical V_G profile. To better simulate the V_G profile in practical applications, we have developed a circuit method to produce resonant V_G overshoots [Fig. 1(d)] and used it to characterize gate breakdown and lifetime [14], [15]. However, these V_G overshoots still differ from practical stress profiles as they lack the DC bias.

In addition to the gate reliability characterization, another key knowledge gap for the p-GaN gate lies in the switching lifetime model. Existing models primarily fit the relationship between gate lifetime and the DC-bias or pulse I-V V_G, using various mathematical functions (e.g., power law, E-mode, 1/E-model) [5], [6], [7], [8], [10], [11]. However, these models are not able to consider the impact of the V_G trajectory in practical waveforms. The pulse I-V lifetime model cannot take into account the impacts of the ringing slew rate, and the DC lifetime model cannot even capture the possible dependences on f_{SW} and duty cycle (D).

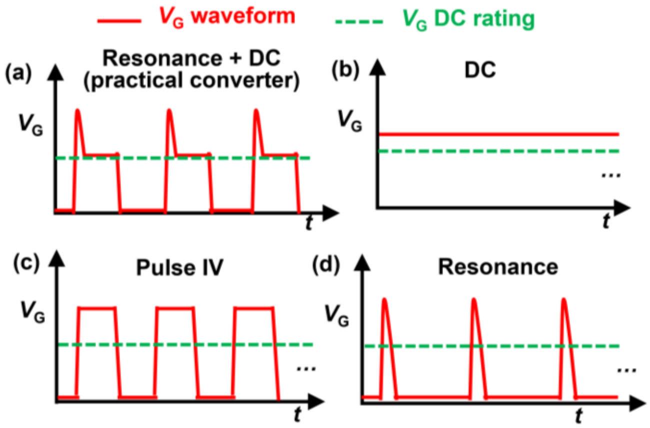


Fig. 1. Gate voltage profiles in (a) practical converters and various reliability tests based on (b) DC bias, (c) pulse I-V tests, and (c) resonance circuit test.

This work is supported in part by the National Science Foundation under the contracts ECCS-2202620 and ECCS-2045001 and by the Power Management Consortium of the Center for Power Electronics Systems, Virginia Tech.

This work addresses these barriers by developing a new circuit method to produce an application-like V_G stress profile and, for the first time, deriving a switching lifetime model for p-gate GaN HEMTs based on the circuit test results. The produced V_G profile consists of a resonant ringing added to a DC bias of 5 V, where the resonance has a controllable peak V_G ($V_{G(PK)}$) and a pulse width of less than 20 ns, producing dV_G/dt comparable to practical applications. The derived switching lifetime model captures the stress generated along the entire V_G waveform and the acceleration effects of f_{SW} and temperature (T). Moreover, this model can capture the gate stress under both resonant ringing and DC-bias ($V_{G(DC)}$) and quantify the impacts of multiple parameters including $V_{G(PK)}$, pulse width (PW) of the ringing, $V_{G(DC)}$, f_{SW}, and D. Thus, this switching lifetime model offer straightforward references for the qualifications and applications of GaN power HEMTs.

II. NEW CIRCUIT TEST SETUP

The device under test (DUT) is a 650V/30A GaN SP-HEMT from a mainstream vendor. Over 300 devices from different batches were tested to validate statistical significance.

Fig. 2(a) shows the schematics of our prior circuit reported in [14], [15], and Fig. 2(b) illustrates the modified circuit used in this work. Both circuits produce fast, resonant V_G pulses from an unclamped discharging of energy in the inductor L_G, mimicking the parasitic inductance of the practical driver loop. The working principle of the prior circuit is elaborated in our earlier work [14], using an input DC voltage (V_{DD}) to mimic the source of surge energy, and a fast switch S_1 to modulate the amount of surge energy. The V_G DC platform after the overshoot is set by V_{DD}, satisfying $V_{G(DC)} = V_{DD}$. In Fig. 2(a), the V_{DD} is fixed at 0.5 V to ensure an OFF-state after the overshoot. The circuit in Fig. 2(b), while remaining the same overvoltage-generation loop, uses a high V_{DD} of 5 V to produce an ON-state of the DUT with an operational DC bias after the V_G overshoot. An additional loop is included in Fig. 2(b) loop to generate an OFF state by pulling down the V_G with a negative DC platform. This second loop comprises a fast switch S_2, a resistor R_1, and an isolated DC voltage source V_1 (1 V). Fig. 2(c) shows the photo of the prototyped board, and Fig. 2(d) details the component specifications. Fig. 2(e) presents the experimental waveforms of the DUT's V_G, and the driving signals of the two switches (S_1 and S_2) in a cycle. The circuit operation can be divided into four stages:

Stage 1 [$t_0 \sim t_1$]: S_1 and S_2 are ON. L_G is charged by V_{DD}. The peak L_G current (I_{LG}) is modulated by the ON time of S_1 ($t_{ON,S1}$). The DUT's V_G (~ −0.9 V) equals $-V_1$ added to the forward voltage drop of S_2 (~0.1 V), keeping the DUT OFF.

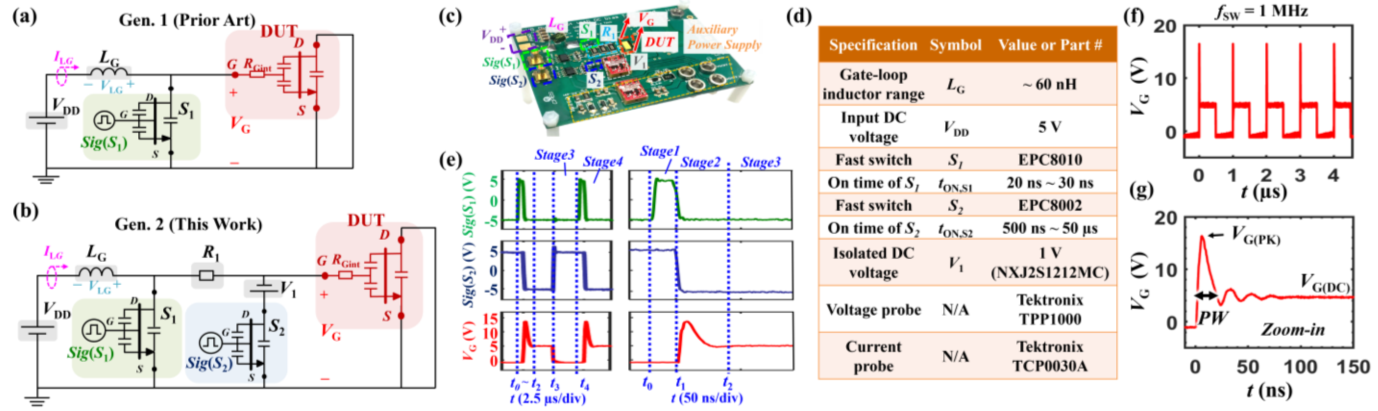
Stage 2 [$t_1 \sim t_2$]: S_1 and S_2 turn OFF simultaneously. The energy stored in L_G creates a V_G overshoot on the DUT via an RLC resonance (R is R_1, L is L_G, and C is the S_1's output capacitance and DUT's input capacitance). This overshoot is quickly damped by R_1, and the DUT's V_G settles to V_{DD}.

Stage 3 [$t_2 \sim t_3$]: S_1 and S_2 are both OFF, V_G remains V_{DD}.

Stage 4 [$t_3 \sim t_4$]: S_2 turns ON while S_1 remains OFF. The DUT's V_G remains ~ −0.9 V.

The PW of V_G overshoot, defined as the duration when V_G exceeds V_{DD}, is adjusted 20 ns by tuning L_G value. The $V_{G(PK)}$ is adjusted ranging from 13.5 to 17.5 V in various tests by tuning $t_{ON,S1}$. The dV_G/dt in this work ranges from 0.7 to 2 V/ns. The lifetime in this work is tested by repetitive switching, with f_{SW} ranging from 10 kHz up to 2 MHz and the duty cycle (D) kept at 0.5. A program is developed to detect waveform deformation (i.e., DUT failure, validated by post-stress characterization) and count the number of switching cycles. Fig. 2(f) shows an exemplary V_G waveform under $V_{G(PK)} = 16.5$ V, $V_{G(DC)} = V_{DD} = 5$ V, $f_{SW} = 1$ MHz, and $PW = 20$ ns. The DUT case temperature (T_C) is adjusted by a power resistor attached to the case and calibrated by a thermocouple and thermal camera.

Similar to previous work [14], the circuit in Fig. 2(b) can also be integrated with an inductive load in the power loop to test gate reliability under hard switching. In this work, all tests are performed under the drain-source grounded (DSG) condition, as it has been shown to pose more severe gate stress compared to hard switching [13], [14]. In this DSG condition, minimal heating is produced, with the DUT junction temperature (T) nearly identical to T_C.



Specification	Symbol	Value or Part #
Gate-loop inductor range	L_G	~ 60 nH
Input DC voltage	V_{DD}	5 V
Fast switch	S_1	EPC8010
On time of S_1	$t_{ON,S1}$	20 ns ~ 30 ns
Fast switch	S_2	EPC8002
On time of S_2	$t_{ON,S2}$	500 ns ~ 50 µs
Isolated DC voltage	V_1	1 V (NXJ2S1212MC)
Voltage probe	N/A	Tektronix TPP1000
Current probe	N/A	Tektronix TCP0030A

Fig. 2. The schematics of the circuits in (a) our prior work and (b) this work. (c) Photo of the prototyped system. (d) Table listing the component specifications. (e) working stages and waveforms (left) including a switching cycle and (right) zoom-in view of the period including charging of L_G and generation of V_G overshoot. (f) Exemplary test waveform at $V_{G(PK)} = 16.5$ V and $f_{SW} = 1$ MHz and (g) Zoom-in view over the overshoot period.

III. SWITCHING LIFETIME MODEL

Based on tests of over 300 DUTs under different conditions, the gate lifetime is found to depend on $V_{G(PK)}$, f_{SW}, and T. The $V_{G(DC)}$ in the range of 0.5 V to 5.5 V induces minimal impact on gate lifetime, suggesting V_G stress is dominant by the resonant overshoot rather than the operational DC platform.

Upon reaching the wear-out gate failure under various test conditions, we assume the cumulative stress to failure ($\Sigma stress$) is a constant for a certain device technology [16]

$$\Sigma stress = \Sigma stress^V \times AF^{fsw} \times AF^T = Const \qquad (1)$$

where $\Sigma stress^V$ represents the total stress from gate voltage acceleration; AF^{fsw} and AF^T are the acceleration functions of f_{SW} and T, respectively.

To probe models for V_G acceleration, we assume that the gate lifetimes tested under various $V_{G(PK)}$ should produce a similar $\Sigma stress^V$. Fig. 3(a) shows the switching cycle to failure (#SCTF) data of DUTs measured at various $V_{G(PK)}$ at T of 25, 50 and 125 ºC. For each condition, the #SCTF of 10 DUTs are fitted by Weibull distribution, followed by the extraction of the #SCTF with 63% failure probability (#SCTF63%). Based on a commonly adopted power-law model [17], we suspect $\Sigma stress^V$ to be in the form

$$\sum stress^V = \int_0^T [V_G(t) - V_{G,Th}]^b dt \times \#SCTF \qquad (2)$$

where T is the period of a switching cycle, $V_{G,Th}$ is a V_G threshold above which the gate stress turns significant, and b is a power law coefficient. To fit $V_{G,Th}$ and b, the mean absolute percentage error (MAPE) of three $\sum stress^V$ at various $V_{G(PK)}$ are plotted in Fig. 3(b) for a b range of 10~40 and $V_{G,Th}$ of 3~5 V. Each $\sum stress^V$ is calculated using $\#SCTF_{63\%}$ and the $V_G(t)$ integral based on the V_G waveform. The MAPE shows a similar valley for all three T, verifying the model in (2). Moreover, a wide window of b and $V_{G,Th}$ selection is found to satisfy MAPE < 20% in all conditions. Here we select a b of 26 and $V_{G,Th}$ of 4 V in our model. Note that this 4-V $V_{G,Th}$ is also physically meaningful, as it is roughly the V_G above which the p-GaN Schottky contact becomes reversely-biased [11], [14].

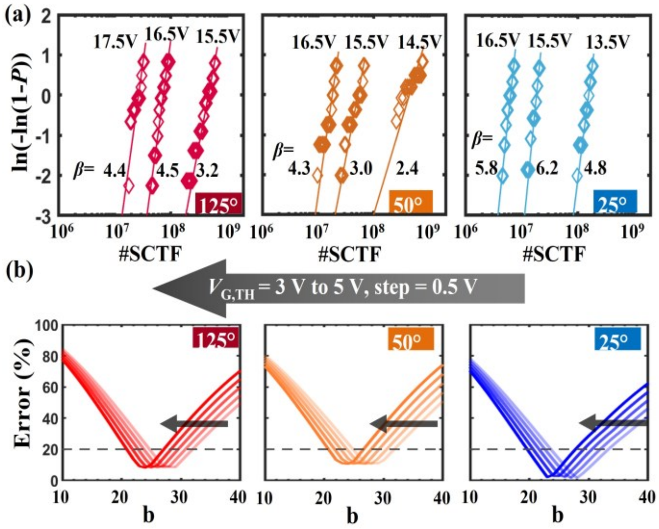


Fig. 3. (a) The #SCTF data of DUTs measured at various $V_{G(PK)}$ at T of 25, 50 and 125 ºC, as well as the Weibull distribution. (b) the mean absolute percentage error (MAPE) of three $\sum stress^V$ versus b and $V_{G,Th}$ for three T.

The f_{SW} acceleration is found to occur only at high f_{SW} > 100 kHz. Below this threshold f_{SW} (f_{Th}), the #SCTF shows nearly no dependence on f_{SW}. In contrast, as shown in Fig. 4(a), the #SCTF decreases fast with f_{SW} above f_{Th}. This general trend is consistent with several other reports [11], [12], [14] using different test methods. As shown in Fig. 4(b), the #SCTF-f_{SW} relation can be fitted by a power-law model, giving AF^{fsw} in the form

$$AF^{fsw} = \begin{cases} 1 & (f_{SW} \le f_{Th}) \\ d \cdot f_{SW}{}^{e} & (f_{SW} > f_{Th}) \end{cases} \qquad (3)$$

where e is a power-law coefficient fitted to be 0.023, and d is a normalization parameter to ensure the continuity of AF^{fsw}.

The T acceleration of #SCTF occurs at the decreasing T, as shown in Fig. 5(a). The #SCTF data at three T can be fitted by

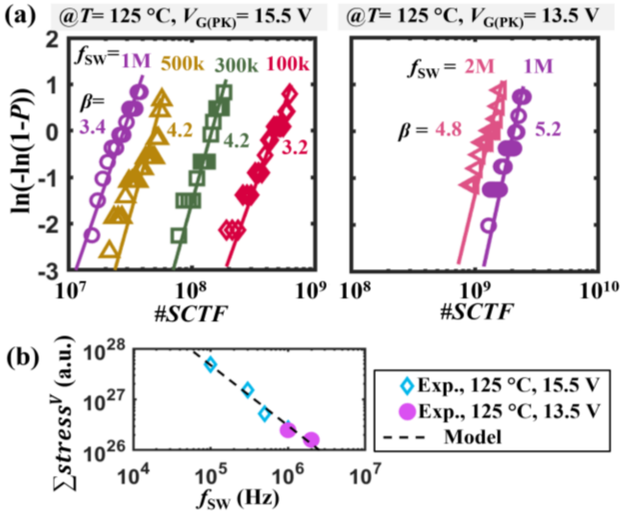


Fig. 4. (a) The #SCTF data of DUTs measured at various f_{SW}, as well as the Weibull distributions. (b) the power-law fitting of $\sum stress^V$ versus f_{SW}.

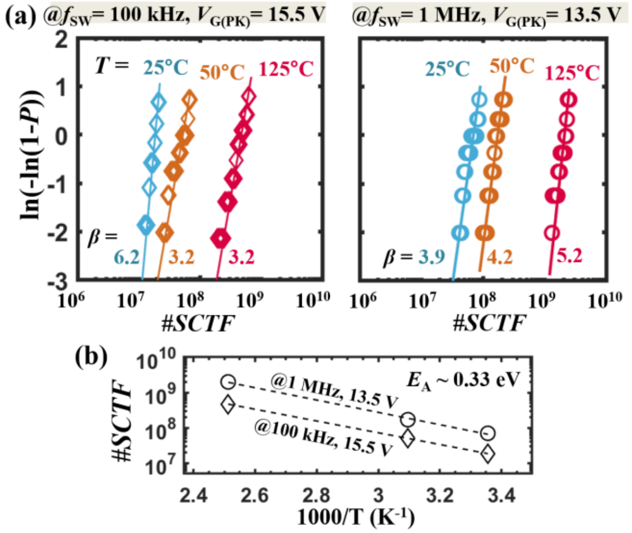


Fig. 5. (a) The #SCTF data of DUTs measured at three different T for two f_{SW}, as well as the Weibull distributions. (b) Arrhenius fitting of #SCTF *vs*. T.

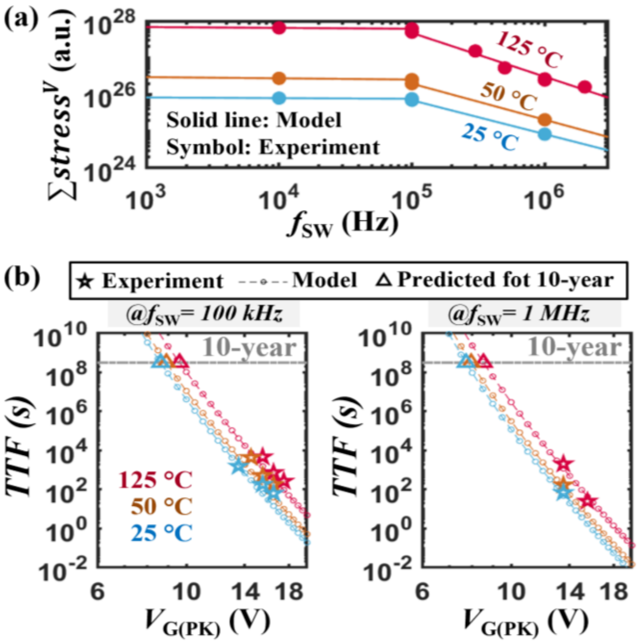


Fig. 6. (a) The $\sum stress^V$ as a function of f_{SW} at different T, illustrating a lower failure boundary (and lower lifetime) at high f_{SW} and lower T due to their acceleration effects. (b) The gate lifetime as a function of $V_{G(PK)}$ at different temperatures and two f_{SW} (100 kHz and 1 MHz). The data from experiments and lifetime model are marked in star and circle symbols, respectively.

the Arrhenius plot for two f_{SW}, as shown in Fig. 5(b), proving the AF^{fsw} and AF^T can be de-coupled. AF^T can be given by

$$AF^T = \exp\left(-E_A/kT\right) \tag{4}$$

where the activation energy (E_A) is fitted to be −0.33 eV.

To illustrate the f_{SW} and T acceleration, $\Sigma stress^V$ is plotted versus f_{SW} at three T in Fig. 6(a). Lower $\Sigma stress^V$ suggests a shorter #SCTF. Finally, by combining (1)-(4), the gate lifetime, i.e., time-to-failure (TTF), can be written as

$$TTF = \frac{\#SCTF}{f_{sw}} = \frac{\Sigma stress}{\int_0^T [V_G(t) - 4V]^{26} dt \times f_{sw} \times AF^{fsw} \times \exp\left(0.33eV/kT\right)} \tag{5}$$

Using this model, the TTF versus $V_{G(PK)}$ can be calculated for various f_{SW} and T, allowing for the extraction of the maximum $V_{G(PK)}$ for 10-year lifetime under various application conditions, assuming the V_G ringing approximately a sinusoidal function. As shown in Fig. 6(b), such maximum $V_{G(PK)}$ is projected to be 7.8 V for f_{SW} of 1 MHz, respectively, at 25 ºC with 63% failure probability, and it increases by ~1 V under either a higher T of 125 ºC or a lower f_{SW} of 100 kHz. As compared to conventional extraction methods, this lifetime model obviates the need for selecting the fitting functions (e.g., power-law, E-model, 1/E model), avoiding the errors associated with the model selection, and thereby providing a more accurate projection for a wider variety of use conditions.

IV. GATE STRESS UNDER RINGING AND DC PLATFORM

In practical converter operations, the gate overvoltage stress primarily originates from two main components: the resonant ringing and the DC platform (i.e., the $V_{G(DC)}$), as illustrated in Fig. 7(a). Understanding the stresses induced by the overvoltage components is crucial for driver design and optimizing the performance and reliability of power electronic systems. Prior DC-based and pulse I-V-based gate lifetime models cannot distinguish the stress from these two V_G profiles.

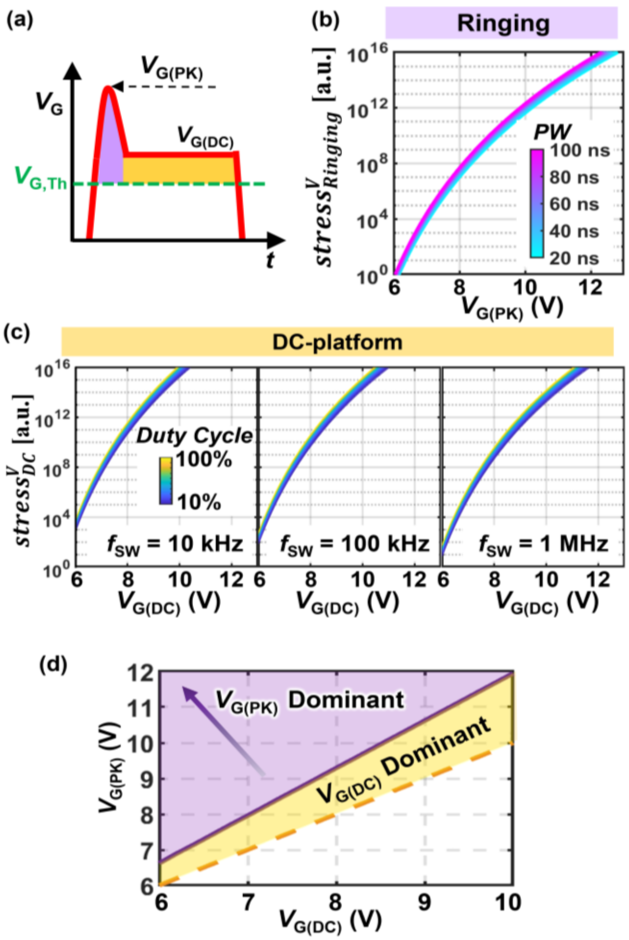


Fig. 7. Schematics of two primary sources of gate overvoltage stress in practical converter operations: resonant ringing (filled in purple) and the DC platform (filled in yellow). The calculated cumulative gate overvoltage stress in one cycle induced by (b) resonant ringing ($stress^V_{Ringing}$) as a function of $V_{G(PK)}$ and PW and (c) induced by the DC platform ($stress^V_{DC}$) as a function of $V_{G(DC)}$, f_{SW} and Duty cycle (D). (d) Projected critical $V_{G(PK)}$ ($V_{G(PK),\,Cri}$), above which the ringing-induced stress becomes dominant, as a function of $V_{G(DC)}$. Here, the $V_{G(PK),\,Cri}$ is estimated at 100 kHz, with D = 50% and PW of ringing assumed as 20 ns. In the regime between the $V_{G(PK),\,Cri}$ line and the $V_{G(DC)}$=$V_{G(PK)}$ line, the stress induced by the DC platform dominates the gate stress.

The switching lifetime model developed in this work can calculate the gate stress along the V_G waveform and quantify the stress from the ringing and DC platform. Here we calculate the cumulative gate overvoltage stress produced by the resonant ring and DC platform individually in a switching cycle (i.e., $stress^V_{Ringing}$ and $stress^V_{DC}$, respectively) using the voltage acceleration function developed in Chapter III. The resonant ringing profile is approximated as a sinusoidal waveform, consistent with prior switching lifetime projections.

The $stress^V_{Ringing}$ shows significant increase at higher $V_{G(PK)}$ and longer PW of the ringing profile [see Fig. 7(b)]. A 1-

V increase of $V_{G(PK)}$ from 8 to 9 V results in a ~350-times increase in the $stress_{Ringing}^{V}$. This indicates the critical role of considering the V_G profile in evaluating gate stress. On the other hand, the $stress_{DC}^{V}$ depends on the $V_{G(DC)}$ and its duration in a switching cycle. Thus, under a specific $V_{G(DC)}$, $stress_{DC}^{V} \propto D/f_{SW}$ [see Fig. 7(c)]. In a 100-kHz switching, increasing the $V_{G(DC)}$ from 7 to 7.5 V generates a ~54 times increase in the $stress_{DC}^{V}$.

The distinct impact factors and dependencies of the two overvoltage components suggest the need for a full consideration of multiple operation conditions when evaluating gate stress. Fig. 7(d) demonstrates an example presenting the projected critical $V_{G(PK)}$ ($V_{G(PK),Cri}$), above which resonant ringing becomes the dominant stressor, as a function of $V_{G(DC)}$ under a 100 kHz switching with D = 50%. Here the PW is considered to be 20 ns to simulate typical practical V_G profile. Below this $V_{G(PK),Cri}$ versus $V_{G(DC)}$ line and above the $V_{G(DC)}$= $V_{G(PK)}$ line is the region where the stress from $V_{G(DC)}$ dominates over the one from $V_{G(PK)}$.

V. PHYSICAL MECHANISM

The Schottky p-gate can be represented by an anti-series connection of the p-GaN Schottky junction and the GaN PIN junction (Fig. 8). Its failure under V_G overshoot can be explained by the time-dependent Schottky breakdown; this mechanism and its T acceleration in circuit tests have been elaborated in [14]. In this work, we newly find the f_{SW} acceleration at f_{SW} > 100 kHz in the circuit test. Note that, in prior circuit test , the f_{SW} is only tested up to 100 kHz.

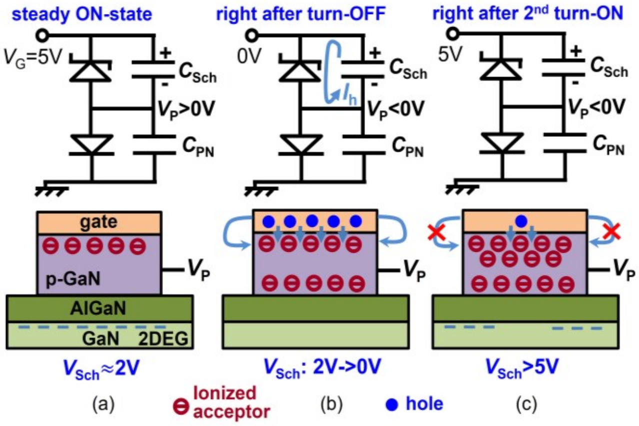


Fig. 8. (Top) equivalent circuit model and (bottom) schematic of charges in the Schottky-type p-GaN gate structure under three working conditions: (a) steady ON-state, (b) right after the turn-OFF, and (c) right after the 2nd turn-ON when V_P has not recovered to zero in the stage (b) (i.e., high-f_{SW} scenario). The arrows in (b) show the hole injection to facilitate the V_p recovery, and such hole injection is blocked at positive V_G in (c) due to the reverse-biased Schottky junction. The voltage across the Schottky junction (V_{Sch}), which is directly proportional to the electric field stress at the Schottky contact, is also marked for three conditions, highlighting the high V_{Sch} and electric field stress in (c).

This newly found f_{SW} acceleration can be explained by a theory similar to [18]. In the steady ON-state, the potential of the non-depleted p-GaN (V_P) is positive (Fig. 8(a)). Right after turn-OFF, due to the depletion charge stored in the Schottky junction, V_P drops to negative. It then gradually returns to zero via hole injection (Fig. 8(b)). When f_{SW} is high, V_P is still negative when the next turn-ON occurs, leading to a high bias across the Schottky junction (V_{Sch}=V_G-V_P), which further induces a high electric field at the Schottky junction (Fig. 8(c)). In addition, the Schottky junction is reverse-biased at V_G > 0 V, which suppresses hole injection and V_P rise. This effect prolongs the high field stress on the Schottky contact. Such higher and prolonged field stress explains the degraded switching lifetime at high f_{SW}. In contrast, when f_{SW} is below a certain threshold (e.g., f_{Th}), there is sufficient time for V_P to rise to 0 V in the OFF-state, which eliminates the extra field stress on the Schottky contact during the next turn-ON originated from the negative V_P.

In summary, this work demonstrates a new circuit method for characterizing the gate reliability of p-gate GaN HEMTs in application-use conditions. The produced V_G stress consists of a resonant ringing added to an operational DC bias. A switching lifetime model is established that can capture the overvoltage stress from an entire practical V_G waveform instead of merely a certain V_G magnitude. The model also quantifies the acceleration effects of f_{SW} and T. The results suggest the DC test is not sufficient to project the gate lifetime of the p-gate GaN HEMT, as the DC lifetime model cannot capture the stress associated with the practical V_G waveform as well as the f_{SW} acceleration. These results provide key reference for the gate qualification, converter application, and driver design of p-gate GaN HEMTs.

VI. CONCLUSIONS

In summary, this work demonstrates a new circuit method for characterizing the gate reliability of p-gate GaN HEMTs in application-use conditions. The produced V_G stress consists of a resonant ringing added to an operational DC bias. A switching lifetime model is established that can capture the overvoltage stress from an entire practical V_G waveform instead of merely a certain V_G magnitude. The model also quantifies the acceleration effects of f_{SW} and T. The results suggest the DC test is not sufficient to project the gate lifetime of the p-gate GaN HEMT, as the DC lifetime model cannot capture the stress associated with the practical V_G waveform as well as the f_{SW} acceleration. We showcase the capabilities of the developed switching lifetime model in two applications: 1) project the maximum $V_{G(PK)}$ for 10-year lifetime without the need for selecting a fitting function; 2) quantitatively comparing the gate stresses induced by the ringing and the DC bias. These results provide key reference for the gate qualification, converter application, and driver design of p-gate GaN HEMTs.

ACKNOWLEDGEMENT

The authors thank Sandeep R. Bahl at Texas Instrument for his valuable suggestions on this work and the manuscript.

REFERENCES

[1] Y. Zhang, F. Udrea, and H. Wang, “Multidimensional device architectures for efficient power electronics,” *Nat Electron*, vol. 5, no. 11, Art. no. 11, Nov. 2022, doi: 10.1038/s41928-022-00860-5.

[2] J. P. Kozak *et al.*, “Stability, Reliability, and Robustness of GaN Power Devices: A Review,” *IEEE Transactions on Power Electronics*, vol. 38, no. 7, pp. 8442–8471, Jul. 2023, doi: 10.1109/TPEL.2023.3266365.

[3] S. K. Murray *et al.*, “Transient Overvoltage Detection Technique for GaN HEMTs Integrated in a 200-V GaN-on-SOI Process,” in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2022, pp. 1400–1405. doi: 10.1109/APEC43599.2022.9773399.

[4] T.-L. Wu *et al.*, “Forward Bias Gate Breakdown Mechanism in Enhancement-Mode p-GaN Gate AlGaN/GaN High-Electron Mobility Transistors,” *IEEE Electron Device Letters*, vol. 36, no. 10, pp. 1001–1003, 2015, doi: 10.1109/LED.2015.2465137.

[5] M. Ťapajna, O. Hilt, E. Bahat-Treidel, J. Würfl, and J. Kuzmík, “Gate Reliability Investigation in Normally-Off p-Type-GaN Cap/AlGaN/GaN HEMTs Under Forward Bias Stress,” *IEEE Electron Device Letters*, vol. 37, no. 4, pp. 385–388, Apr. 2016, doi: 10.1109/LED.2016.2535133.

[6] I. Rossetto *et al.*, “Time-Dependent Failure of GaN-on-Si Power HEMTs With p-GaN Gate,” *IEEE Transactions on Electron Devices*, vol. 63, no. 6, pp. 2334–2339, Jun. 2016, doi: 10.1109/TED.2016.2553721.

[7] S. Stoffels *et al.*, “Failure mode for p-GaN gates under forward gate stress with varying Mg concentration,” in *2017 IEEE International Reliability Physics Symposium (IRPS)*, Apr. 2017, pp. 4B-4.1-4B-4.9. doi: 10.1109/IRPS.2017.7936310.

[8] A. Stockman *et al.*, “Gate Conduction Mechanisms and Lifetime Modeling of p-Gate AlGaN/GaN High-Electron-Mobility Transistors,” *IEEE Transactions on Electron Devices*, vol. 65, no. 12, pp. 5365–5372, Dec. 2018, doi: 10.1109/TED.2018.2877262.

[9] Y. Zhong *et al.*, “Gate Reliability and its Degradation Mechanism in the Normally OFF High-Electron-Mobility Transistors With Regrown p-GaN Gate,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 3, pp. 3715–3724, Jun. 2021, doi: 10.1109/JESTPE.2020.3014372.

[10] A. N. Tallarico, N. E. Posthuma, B. Bakeroot, S. Decoutere, E. Sangiorgi, and C. Fiegna, “Role of the AlGaN barrier on the long-term gate reliability of power HEMTs with p-GaN gate,” *Microelectronics Reliability*, vol. 114, p. 113872, Nov. 2020, doi: 10.1016/j.microrel.2020.113872.

[11] J. He, J. Wei, S. Yang, Y. Wang, K. Zhong, and K. J. Chen, “Frequency- and Temperature-Dependent Gate Reliability of Schottky-Type p -GaN Gate HEMTs,” *IEEE Transactions on Electron Devices*, vol. 66, no. 8, pp. 3453–3458, 2019, doi: 10.1109/TED.2019.2924675.

[12] M. Millesimo *et al.*, “The Role of Frequency and Duty Cycle on the Gate Reliability of p-GaN HEMTs,” *IEEE Electron Device Letters*, vol. 43, no. 11, pp. 1846–1849, Nov. 2022, doi: 10.1109/LED.2022.3206610.

[13] Y. Cheng *et al.*, “Gate Reliability of Schottky-Type p-GaN Gate HEMTs Under AC Positive Gate Bias Stress With a Switching Drain Bias,” *IEEE Electron Device Letters*, vol. 43, no. 9, pp. 1404–1407, Sep. 2022, doi: 10.1109/LED.2022.3188555.

[14] B. Wang *et al.*, “Gate Robustness and Reliability of P-Gate GaN HEMT Evaluated by a Circuit Method,” *IEEE Transactions on Power Electronics*, vol. 39, no. 5, pp. 5576–5589, May 2024, doi: 10.1109/TPEL.2024.3355042.

[15] B. Wang *et al.*, “Dynamic Gate Breakdown of p-Gate GaN HEMTs in Inductive Power Switching,” *IEEE Electron Device Letters*, vol. 44, no. 2, pp. 217–220, Feb. 2023, doi: 10.1109/LED.2022.3227091.

[16] S. R. Bahl, F. Baltazar, and Y. Xie, “A Generalized Approach to Determine the Switching Lifetime of a GaN FET,” in *2020 IEEE International Reliability Physics Symposium (IRPS)*, Apr. 2020, pp. 1–6. doi: 10.1109/IRPS45951.2020.9129631.

[17] K. Ohgata *et al.*, “Universality of power-law voltage dependence for TDDB lifetime in thin gate oxide PMOSFETs,” in *2005 IEEE International Reliability Physics Symposium, 2005. Proceedings. 43rd Annual.*, Apr. 2005, pp. 372–376. doi: 10.1109/RELPHY.2005.1493115.

[18] M. Millesimo *et al.*, “Gate Reliability of p-GaN Power HEMTs Under Pulsed Stress Condition,” in *2022 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2022, p. 10B.2-1-10B.2–6. doi: 10.1109/IRPS48227.2022.9764592.