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Paving the Way for Pass Disturb-Free Vertical NAND Storage via a Dedicated and String-Compatible Pass Gate

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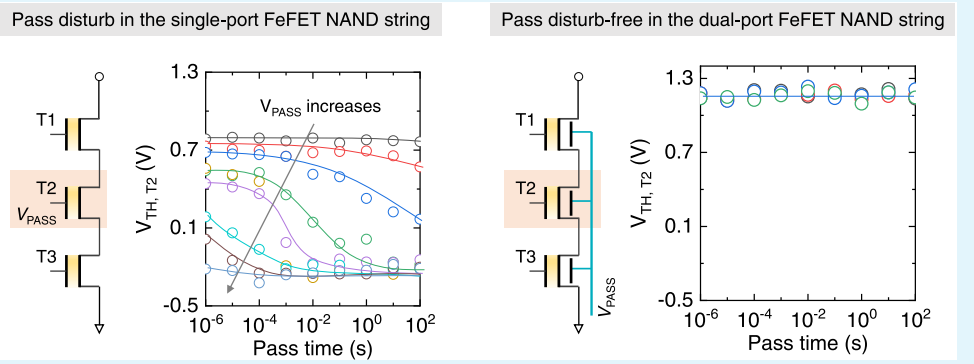

ABSTRACT: In this work, we propose a dual-port cell design to address the pass disturbance in vertical NAND storage, which can pass signals through a dedicated and string-compatible pass gate. We demonstrate that (i) the pass disturb-free feature originates from weakening of the depolarization field by the pass bias at the high-V_{TH} (HVT) state and the screening of the applied field by the channel at the low-V_{TH} (LVT) state; (ii) combined simulations and experimental demonstrations of dual-port design verify the disturb-free operation in a NAND string, overcoming a key challenge in single-port designs; (iii) the proposed design can be incorporated into a highly scaled vertical NAND FeFET string, and the pass gate can be incorporated into the existing three-dimensional (3D) NAND with the negligible overhead of the pass gate interconnection through a global bottom pass gate contact in the substrate.

KEYWORDS: *dual-port FeFET, disturb free, vertical NAND, FEOL, BEOL*

INTRODUCTION

Vertical NAND flash storage, as shown in Figure 1a, has been the backbone of the current digital storage system due to its high density and low cost.[1−4] It attains an impressive memory density by vertically stacking memory layers, as shown in the cross-sectional schematic in Figure 1b, with the state-of-the-art design surpassing 200−300 layers[5,6] and marching toward an unprecedented 1000 layers.[7] Concurrently, there is a growing interest in exploring cell technologies beyond conventional flash transistors to lower operation voltage and enhance operational speed. One noteworthy contender is the ferroelectric field-effect transistor (FeFET), gaining attention following the discovery of ferroelectricity in thin doped HfO_2 films.[8−10] Possessing a similar transistor structure, vertical FeFET demonstrates the potential for multibit storage through partial polarization switching and an exceptionally efficient polarization switching process,[11−13] making it a promising candidate for mass storage. However, whether employing commercialized flash or potential FeFET storage, a common challenge faced by the vertical NAND structure is the escalating disturbance to memory states during array operation under aggressive scaling.[14] Such disturbance could increase the bit error rate and under extreme cases, cause information loss.[15] In this study, we thoroughly investigate disturbance issues in NAND storage using the FeFET as an illustrative platform. To address these challenges, we introduce a novel dual-port FeFET structure, as shown in Figure 1c, designed to enable disturbance-free operation.

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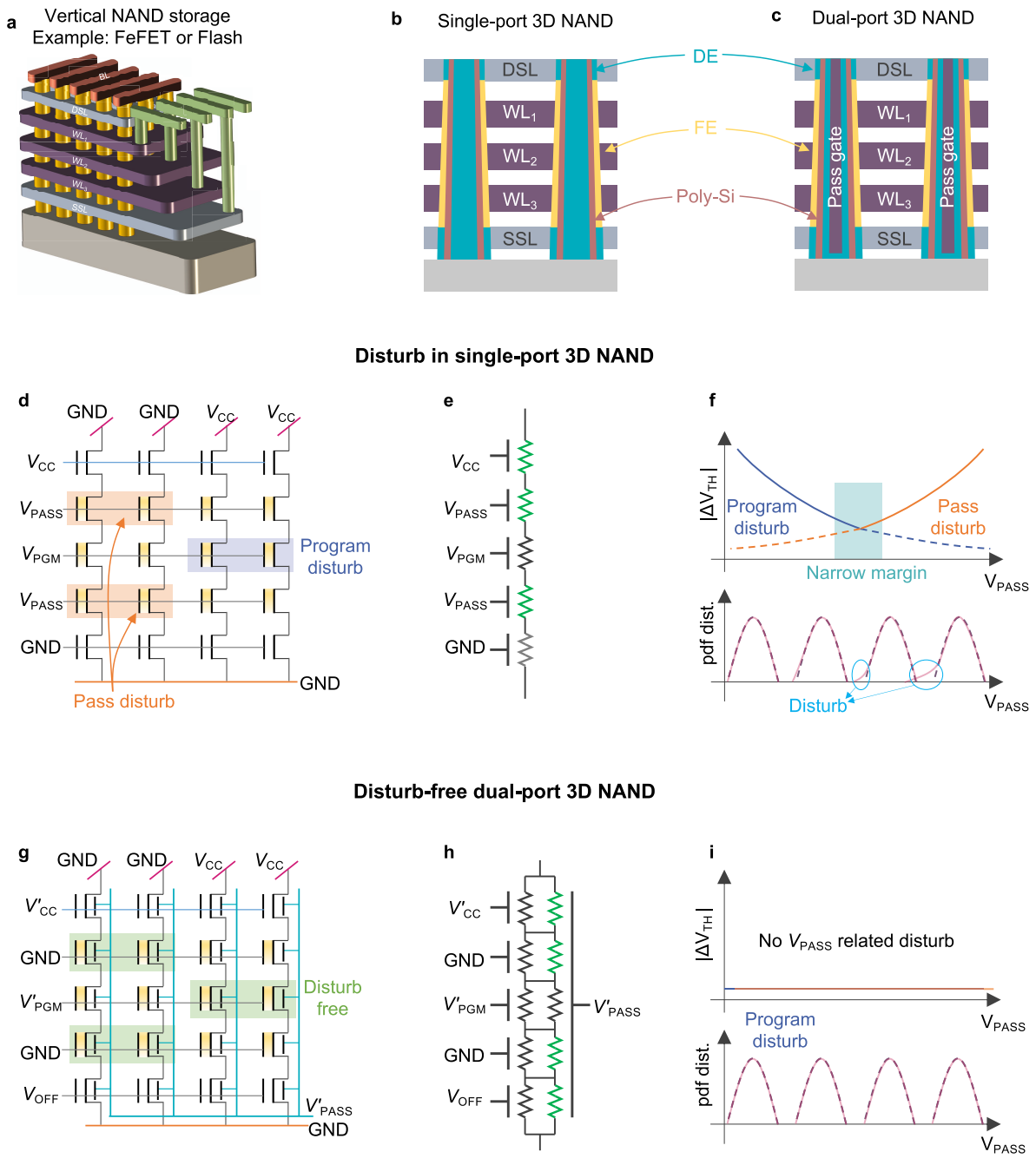

Figure 1. Dual-port vertical NAND FeFET for pass disturb-free operation. (a) The conventional vertical NAND flash storage has been widely used as a high-density low-cost storage. FeFET can utilize a similar structure to achieve lower operation voltage and faster operation speed. (b) The conventional vertical storage stacks hundreds of layers for a higher density but suffers from escalating disturbance due to the aggressive scaling. (c) Adding a second port specifically for the read and pass operations can address these challenges. (d) A typical global self-boosting program inhibition scheme for the program and inhibition operations. The program disturb occurs on the selected page, while the pass disturb is seen on the unselected pages. (e) The equivalent circuit model for the selected string. The green resistors represent ON cells. (f) A high V_{PASS} causes the pass disturb, while a low V_{PASS} increases the program disturb. The disturb-free margin is narrow. (g) The proposed design features an independent nonferroelectric pass gate for the read and pass operation. The V_{PASS} will no longer be applied to the ferroelectric gate, resulting in a pass disturb-free operation. (h) The equivalent circuit model for the selected string. The pass transistors are turned ON from the pass gate. Panel (i) illustrates the negligible V_{TH} shifts and the related distribution.

Due to its unique serial structure, the vertical NAND array is more susceptible to disturb than other structures of a memory array during memory read and write operations.[16] For example, to read the target cell in a conventional single-port vertical NAND string, where the program and pass biases are applied on the same gate (i.e., word line, (WL)), other unselected cells in the same string need a large pass voltage, V_{PASS}, on the gate to pass string end voltages to the target cell.[17] For this purpose, V_{PASS} needs to be greater than the highest threshold voltage (V_{TH}) to ensure turning ON unselected cells regardless of their V_{TH} states. As a result, a high V_{PASS} could disturb the memory states. In addition, the choice of V_{PASS} is even more delicate during memory write operation in order to balance between various disturbs.[18] Figure 1d shows a typical global self-

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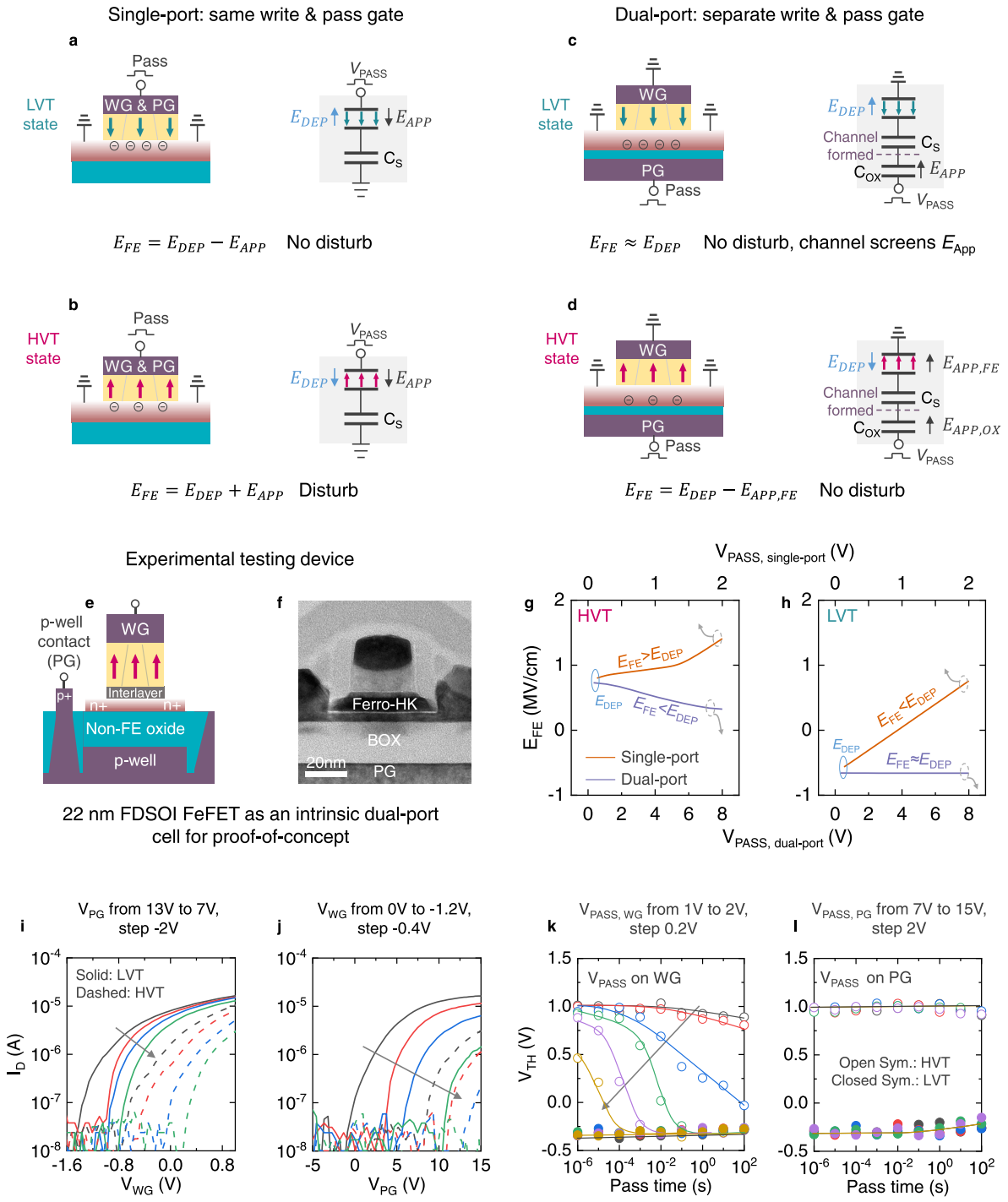

Figure 2. Origin of pass disturbance in the single-port FeFET and the pass disturbance free in the dual-port FeFET. (a) For the single-port FeFET in the LVT state, the V_{PASS} applied to the gate with the ferroelectric film generates E_{APP}, which counteracts the E_{DEP}. (b) In contrast, the E_{APP} applied in the HVT state enhances E_{DEP}, causing pass disturb. (c) Dual-port FeFET offers two independent paths for write and read/pass operations, respectively. For the FeFET in the LVT state, although the E_{APP} aligns with the E_{DEP}, the applied pass bias is screened by the formed channel electrons, resulting in no enhancement in E_{DEP}. (d) For the FeFET in the HVT state, E_{APP} is aligned with the polarization, thus enhancing retention. (e, f) The schematic and the TEM of the FDSOI FeFET used for experimental verification.[23] (g, h) The simulated results of the E_{FE}-V_{PASS} curves confirm the analysis of the read disturb issue. (i, j) $I_D - V_G$ curves for WG read and PG read measured after ±4 V, 1 μs write pulses. (k, l) V_{TH} shifts were measured after different pass time lengths under different pass voltages applied on the WG and PG, respectively. No V_{TH} shift is found when measuring with PG. TEM image reprinted with permission from Reference 23. Copyright 2017 IEEE.

boosting program inhibition scheme adopted in vertical NAND.[19,20] After a block erase, the target cells on the selected page will be programmed, while other cells on the same page will be inhibited. This is achieved by applying a ground and V_{CC} on the selected cells and unselected cells, respectively. In this way, the selected cells have enough voltage applied to program the state while unselected strings are floating, and the channel potential will be raised by the applied voltages to inhibit programming. Figure 1e shows the equivalent circuit model for the selected string, where the green resistors

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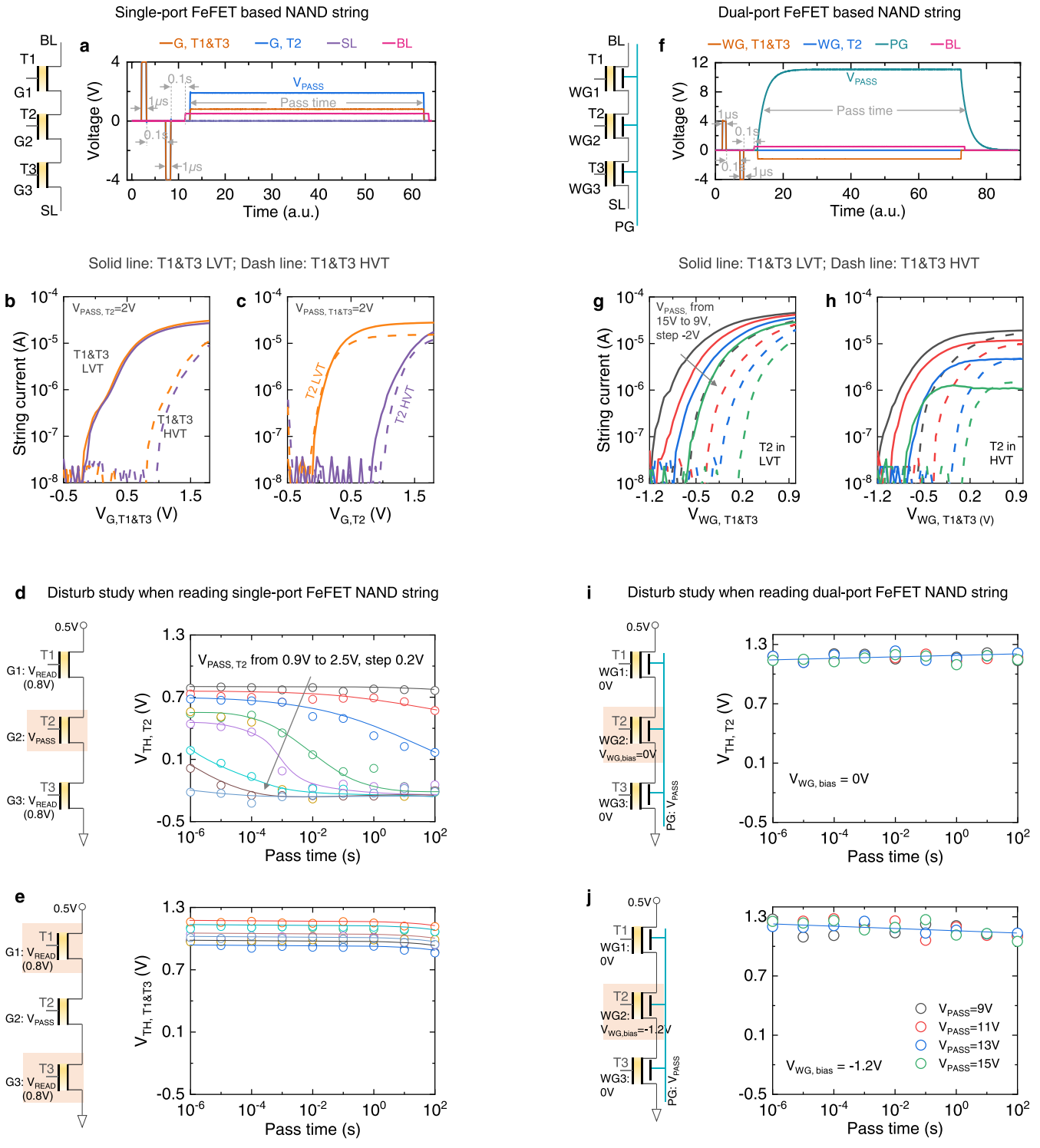

Figure 3. Experimental Validation of the pass disturb-free operation in the NAND FeFET string. (a) Experimental setup and waveforms for the single-port FeFET-based NAND string. The gates of T1 and T3 are wired together for ease of characterization. (b, c) String current when respectively sweeping $V_{G,\ T1\ \&\ T3}$ and $V_{G,\ T2}$ with V_{PASS} = 2 V. (d) Characterization of the pass disturb under different V_{PASS} conditions. A higher V_{PASS} value causes a shorter pass time for the V_{TH} state to be disturbed. (e) Read disturb is unnoticeable in T1 and T3 as V_{READ} is much lower than V_{PASS}. (f) Experimental setup and waveforms for the dual-port FeFET-based NAND string. (g, h) String current sweep when applying the pass voltage on the PG of T2 for the LVT and HVT state, respectively. A higher V_{PASS} value is necessary to achieve a high string current when T2 is in the HVT state. (i) No V_{TH} shift is found when reading the NAND string from the PG. (j) The condition of $V_{WG,\ bias}$ = −1.2 V is also measured to confirm the pass disturb-free operation.

represent ON cells. Under this scenario, a high/low V_{PASS} will introduce severe pass/program disturb, respectively, as shown in Figure 1f. When V_{PASS} is very high, the pass disturb to the cells on the same selected strings, as shown in Figure 1d, will be significantly disturbed. However, when V_{PASS} is very low, the unselected string channel potential may not be elevated

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enough to inhibit program disturb to unselected cells on the same page, as shown in Figure 1d. Therefore, only a narrow V_{PASS} margin is available, and sometimes a trade-off has to be made.

To address this challenge, a dual-port vertical NAND, shown in Figure 1c, is proposed in this work, which features an independent pass gate (PG) in the core of a NAND string and normal nonferroelectric gate dielectric, which can turn ON the string channel for the passing operation. In this way, such a structure is compatible with the vertical NAND array without incurring significant overhead when introducing the additional gate. Figure 1g shows the programming bias scheme for the proposed dual-port vertical NAND array, where the pass operation is conducted by using a dedicated pass gate. In this case, unselected cells on the same target strings will no longer need a high V_{PASS} on the ferroelectric gate, thus completely eliminating the pass disturb. Figure 1h shows the equivalent circuit model for this case, where the channel is turned ON from the back such that the string end voltages can be passed to the target cells. As a result, we argue that there will be negligible disturbance to the memory states with the dual-port transistor design, and the array distribution will be highly robust against the pass disturb, as illustrated in Figure 1i. In the following, we will clarify the origin of disturb-free operation in the dual-port FeFETs and validate experimentally in both the front-end-of-line (FEOL) and back-end-of-line (BEOL) HfO_2-based FeFETs, demonstrating disturb-free operation in NAND FeFET string and performing technology computer-aided design (TCAD) studies on scaled vertical FeFET.

DUAL-PORT FEFET ENABLING DISTURB-FREE OPERATION

Analysis on the Origin of Pass Disturb. The origin of pass disturb in the single-port FeFET and the disturb-free operation in the dual-port FeFET are illustrated in Figure 2. For a single-port FeFET, where the write/read/pass biases are all applied on the gate with the ferroelectric film, disturb can result. If the single-port FeFET is in the low-V_{TH} (LVT) state, as shown in Figure 2a, then a V_{PASS} applied on the gate generates an applied electric field, E_{APP}, which is aligned with the polarization, thus weakening the depolarization field (E_{DEP}) and improving the state stability. In contrast, when FeFET is in the high-V_{TH} (HVT) state, as shown in Figure 2b, the applied E_{APP} exerted by the V_{PASS} will be against polarization, thus enhancing the E_{DEP} and causing retention loss. Pass disturb to other intermediate states will also be between that for the LVT and HVT extreme states. Such pass disturb can be eliminated through structural modification by adopting a dual-port FeFET, where a second electrical gate with nonferroelectric dielectric is incorporated.[21] Due to the thin film channel, the polarization set through the ferroelectric gate controls the channel carrier concentration, which can also be sensed through the nonferroelectric gate. This innate structural property ensures pass disturb-free operation. For example, when the FeFET is set to the LVT state, as shown in Figure 2c, the pass bias applied on the nonferroelectric pass gate could cause an E_{APP} against the polarization. However, in this case, the channel is fully turned ON such that all of the applied bias is screened by the channel electrons, and almost no electric field can penetrate through the channel and reach the ferroelectric layer. As a result, the ferroelectric state is retained. For the HVT state, the E_{APP} exerted by the pass bias is aligned with the polarization, thus helping HVT state retention, as shown in Figure 2d.[22]

Experimental Verification. To validate the disturb-free pass operation in dual-port FeFET, two types of FeFETs are integrated and characterized: one FEOL version and one BEOL version. The FEOL dual-port FeFET is simply realized with fully depleted silicon-on-insulator (FDSOI) FeFET, as shown in Figure 2e, where the ferroelectric sits on the top of the Si channel, and the buried oxide (BOX) is the nonferroelectric dielectric while the p-well contact can serve as the pass gate. Figure 2f shows the transmission electron microscopy (TEM) image of the testing device integrated on the 22 nm FDSOI platform.[23] First, a theoretical understanding of the disturb-free pass operation is gained by checking the ferroelectric electric field at different pass biases for both single-port and dual-port FEOL FeFET using well-calibrated TCAD models of the FDSOI transistor. Figure 2g and **h** shows the ferroelectric electric field for the HVT state and LVT state, respectively. It shows that the depolarization field was enhanced in the single-port device while reduced in the dual-port device at the HVT state, thus supporting the physical picture discussed above. For the LVT state, the depolarization field is reduced for the single-port device while remaining constant for the dual-port device due to the channel screening. Experimental validation on the FDSOI FeFET is also conducted. Figure 2i and j shows measured $I_D - V_G$ curves swept on the ferroelectric gate and the nonferroelectric gate, respectively. For each gate sweep, it shows the classical behavior that V_{TH} can be tuned linearly with the other gate bias. It also shows a much larger memory window for the nonferroelectric gate sweep due to the much larger equivalent oxide thickness (EOT).[21] Figure 2k shows the disturb to the HVT and LVT state on a single-port FeFET when V_{PASS} is applied on the write gate (WG). It shows a severe disturbance to the HVT state by V_{PASS} in a single-port FeFET and no disturbance to the LVT state. However, for the dual-port FeFET, as shown in Figure 2l, both the HVT and LVT states are stable under V_{PASS} bias, therefore verifying the disturb-free pass operation. The pass disturb-free operation is also experimentally verified on the BEOL dual-port FeFET. The FeFET is realized with the ferroelectric placed below the amorphous metal oxide thin film channel (e.g., tungsten doped indium oxide (IWO) in this work) and the nonferroelectric layer placed above the channel, as shown in Supplementary Figure S2.

PASS DISTURB-FREE OPERATION IN NAND FEFET STRING

Next, the pass disturb-free operation in a NAND FeFET string will be tested. Without loss of generality, a string composed of three FDSOI FeFETs is tested, which contains all of the key features of the NAND array and is enough to demonstrate the working principles. First, pass disturb in a single-port FeFET NAND string is demonstrated. Figure 3a shows the experimental setup and waveforms for a single-port FeFET-based NAND string. For ease of characterization, during the experiment, gates of the top transistor (i.e., T_1) and bottom transistor (i.e., T_3) are wired together, which makes T_1 and T_3 have the same state and operations at all times. The waveform shows a case where V_{READ}/V_{PASS} is applied to selected (T_1 & T_3)/unselected (T_2) transistors. With this setup, the $I_D - V_G$ characteristics of T_1 & T_3 can be obtained, as shown in Figure 3b, demonstrating the successful operation of the string. Similarly, when the selected cell is T_2, a V_{PASS} will be applied on T_1 & T_3, and $I_D - V_G$ characteristics of T_2 can be measured, as shown in Figure 3c. In this case, irrespective of the states of unselected cells, the correct memory information on selected cells can be successfully sensed. Following this demonstration, the pass disturb is characterized, as shown in Figure 3d, where V_{PASS} is applied on T_2 for T_1& T_3 sensing. Different V_{PASS} from 0.9 to 2.5 V are applied, and then T_2 V_{TH} is measured. Similar

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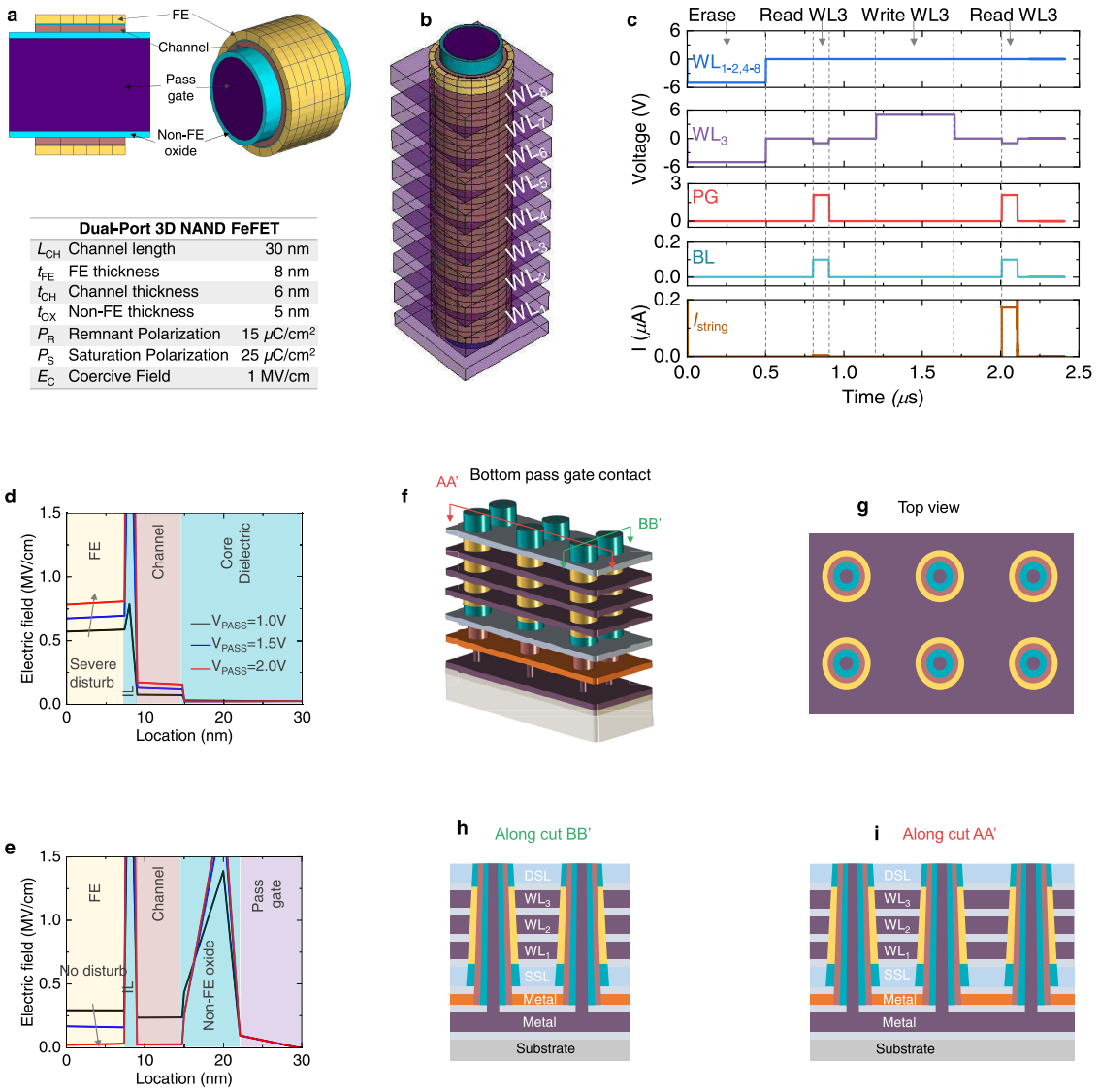

Dual-Port 3D NAND FeFET

L_{CH}	Channel length	30 nm
t_{FE}	FE thickness	8 nm
t_{CH}	Channel thickness	6 nm
t_{OX}	Non-FE thickness	5 nm
P_R	Remnant Polarization	15 μC/cm^2
P_S	Saturation Polarization	25 μC/cm^2
E_C	Coercive Field	1 MV/cm

Figure 4. Scaled dual-port vertical NAND FeFET operation and integration. (a) Cross-section of the dual-port memory cell and its parameters in TCAD simulation. (b) A 3D model of the dual-port NAND string with 8 WLs. (c) Operation waveforms show erase, write, and read operations. WL_3 is the select cell. (d, e) Electric field distribution in the single- and dual-port gate stacks of the pass cell in the HVT state. The electric field induced by V_{PASS} enhances the depolarization field in the single-port string while it degrades it in the dual-port string. (f) Proposed 3D design for the vertical NAND-compatible structure. It features a core pass gate in the center of the string with a pass gate contact at the bottom. (g–i) Top view and cutline views of the proposed design showing the details of the global pass gate.

to the single cell demonstration on single-port FeFET shown in Figure 2k, severe disturb can happen for a large V_{PASS}. For example, if V_{PASS} = 2.3 V, then 100 μs of pass time can completely flip the memory state, thus posing a serious concern over the state stability. This disturb is of course highly stress bias dependence, as also seen in the read disturb characterization to T_1 & T_3 shown in Figure 3e, where the state is not disturbed.

Dual-port FeFET can eliminate pass disturb by incorporating separate ports for write/read and pass operations. Figure 3f shows the three-transistor NAND string and the corresponding testing waveforms. The p-well body contact shared among the three transistors is used for pass operation. The waveform shows write and read pulses of T_1 & T_3, and T_2 write gate is grounded while the pass bias is applied on the pass gate. Figure 3g and **h** shows the $I_D - V_G$ characteristics of T_1 & T_3 when the unselected cell T_2 is at the LVT state and the HVT state, respectively. It shows that sensing of the target cell memory state can be successfully realized. Note that the results also show that a high enough V_{PASS} is required; otherwise, the HVT state device is not fully turned ON, which could limit the string current, as shown in Figure 3h. Figure 3i and j shows study pass disturb in the dual-port NAND FeFET string. The V_{TH} of cell T_2 is measured after pass bias is applied to the pass gate. The results show that T_2 is not disturbed at all, even when V_{PASS} = 15 V is applied. These results therefore confirm the pass disturb-free nature of the dual-port NAND string.

SCALED DUAL-PORT VERTICAL NAND FEFET OPERATION AND INTEGRATION

Previous verifications on a planar dual-port FeFET device and NAND string have demonstrated that the pass disturb-free operation originates from its unique structural property. Such a principle should also be applicable to a vertical NAND array.

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To verify the dual-port operation in a practical vertical NAND string, we performed TCAD simulations. The cross-section of a dual-port memory cell and its parameters are shown in Figure 4a. A 3D model of a dual-port NAND string with 8 WLs is shown in Figure 4b. In the simulation, operations to write and read the WL_3 cell is shown in Figure 4c. First, all of the cells are erased, after which the WL_3 cell is read out. To do that, the center pass gate is applied a pass bias, and a WL_3 read bias is applied. In this case, a low string current is read out due to the erase operation. Then, the WL_3 cell is programmed into the LVT state. After the read operation, a high string current is sensed. Therefore, it demonstrates the feasibility of the proposed technique in vertical NAND FeFET string. In addition, Figure 4d and **e** shows the electric field in the gate stack for both single- and dual-port strings for the pass cell in the HVT state. When V_{PASS} is applied also on the write gate, the depolarization field in the ferroelectric is enhanced while it is reduced when the pass voltage is applied on the central pass gate in a dual-port FeFET string. The extracted electric field distribution of a NAND string with different V_{PASS} is shown in Supporting Figure S2. These results demonstrate that pass disturb-free operation is applicable for the vertical NAND array.

It is also worth noting that the proposed design is compatible with existing vertical NAND process integration with minimum overhead.[16,17] Supporting Figure S3 shows a tentative process integration flow to integrate a center core pass gate. The center core metal can be filled after memory hole etching and subsequent deposition of the ferroelectric, polysilicon channel, and pass gate nonferroelectric dielectric. A few other steps, such as selective deposition of the gate metal for the string select transistor, can be included for complete processing. The resulting 3D structure is shown in Figure 4f. It suggests a similar structure to a conventional vertical NAND array.[24] However, for each string, the central filler is no longer a dielectric but a metallic pass gate, which is connected to a bottom pass gate contact patterned in the bottom substrate in a block. The top view and cutline views in Figure 4g–i show more details. Leveraging the global pass gate, the pass operation can be performed at a low cost.

CONCLUSIONS

We have performed a comprehensive evaluation of the challenges of the single-port NAND FeFET in handling pass disturb and the effectiveness of the proposed dual-port design through a combined experimental verification and mechanism analysis. We studied the origin of the pass disturbance by analyzing the depolarization field and the applied field. We have shown that the dual-port design is immune to the pass disturbance due to the unique dual-port structure. We also proposed a global bottom pass gate contact and explored the design in highly scaled vertical NAND memory through TCAD simulation. The key significance of this work is to address the obstacles to FeFET in NAND applications caused by the pass disturb, and moreover, this design can be extended to vertical NAND flash storage.

ASSOCIATED CONTENT

Data Availability Statement

The data that support the plots within this paper and other findings of this study are available from the corresponding author on reasonable request.

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.4c08190.

Additional data concerning device fabrication; electrical characterization; characterization of the dual-Port BEOL IWO FeFET; extracted electric field of the NAND string; and tentative process flow for the dual-port vertical FeFET-based NAND storage (PDF)

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Author Contributions

K.N., V.N., and S.D. proposed and supervised the project. Z.Z., Z.J., S.D., and Y.X. performed FEOL FeFET experimental verification. K.A.A. and S.G.K. performed BEOL FeFET experimental verification. S.W. and S.Y. conducted 3D TCAD simulations. H.M., S.D., D.K., S.S., and S.B. fabricated the FEOL FeFET devices. R.J. helped with the device validation. S.M., and M.M. helped with the FDSOI FeFET operations as a dual-port FeFET. S.L., K.K., K.K., W.K., and D.H. helped discussion of the project. All authors contributed to write-up of the manuscript.

Notes

The authors declare the following competing financial interest(s): An invention disclosure has been submitted through the Pennsylvania State University.

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