A Large Window Nonvolatile Transistor Memory for High-Density and Low-Power Vertical NAND Storage Enabled by Ferroelectric Charge Pumping

Zijian Zhao, *Graduate Student Member, IEEE*, Yixin Qin, *Graduate Student Member, IEEE*, Jiahui Duan, *Member, IEEE*, YuShan Lee, *Student Member, IEEE*, Suhwan Lim, Kijoon Kim, Kwangsoo Kim, Wanki Kim, Daewon Ha, Vijaykrishnan Narayanan, *Fellow, IEEE*, and Kai Ni, *Member, IEEE*

***Abstract*— In this work, we have developed a large memory window (MW) ferroelectric field effect transistor (FeFET) memory for vertical NAND storage. We demonstrate that: 1) by inserting a top functional layer above the ferroelectric, gate side injection pumped by ferroelectric switching event can be enhanced, thus increasing the MW; 2) inspired by the charge trap flash, SiN_X is chosen as the charge trapping layer and the proposed structures have been experimentally demonstrated to effectively increase MW; 3) the MIFIS structure demonstrates a 6V-8V MW for 11V 1μs write pulse and 8V-12V window for 15V 1μs with a SiO_X composite functional layer; 4) interestingly, the MIFIS device shows immediate read-after-write capability, which is not observed in the baseline FeFET, suggesting minor channel side injection and relaxation.**

***Index Terms*— Charge pumping, ferroelectric FET, NAND storage, nonvolatile memory, quad-level-cell (QLC), SiN_X, zirconium doped hafnium oxide (HZO).**

I. Introduction

NOWADAYS, data is being generated at an unprecedented rate, calling for tremendous amount of data storage. Vertical NAND flash, due to its high capacity, has become the backbone for data storage. However, one of the serious challenges of NAND flash is the poor write performance (Fig. 1(a)) [1], [2], [3]. Due to the inefficient write mechanism, i.e., tunneling, the required write pulse voltage and pulse width for flash memory are significant, posing reliability and power concerns. FeFET, on the other hand, has a much more efficient write mechanism based on polarization switching, which can be initiated via an applied electric field [4], [5]. However, one major roadblock for FeFET as storage technology is that its memory window (MW) is proportional to its thickness (t_{FE}) (Fig. 1(b)) [6], [7], [8]. Since the gate stack thickness is directly related with the memory density and the gate dielectric thickness should be kept below 20 nm to be competitive with the state-of-the-art flash [9]. To break the fundamental trade-off between the MW and density in FeFETs, a long proposed technique is receiving renewed interests, where the ferroelectric switching and charge injection from the gate side are working synergistically to enhance the MW [10]. In conventional FeFET design, channel side injection is induced by write pulses, offsetting the polarization induced MW (Fig. 2(a)) [11]. In contrast, if a functional layer is inserted above the ferroelectric to facilitate gate side injection, which adds to the polarization effect such that the MW can be enhanced (Fig. 2(b)). In this work, we further hypothesize that the ferroelectric switching acts a charge pump and each switching event pumps charge from the gate into the top functional layer and we call this type of devices as FePFET. Based on this theory, we propose and experimentally demonstrate a FePFET design.

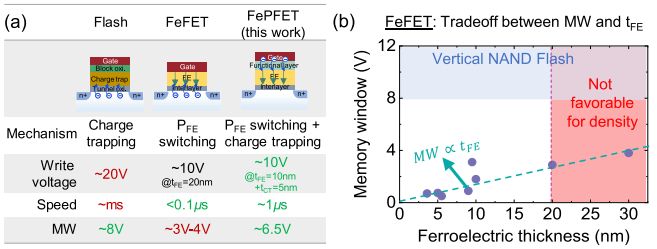


Fig. 1. (a) Comparison of different types of transistor memories. The proposed design features large MW and fast speed, and low write voltage. (b) Pure FeFET suffers from MW and ferroelectric thickness trade-off.

II. Device Design and Fabrication

To illustrate the operation principles, TCAD simulations on the write operation are performed on both the control MFIS and the proposed MIFIS. Fig. 3(a) shows the control

Received 19 May 2024; revised 5 September 2024; accepted 7 October 2024. Date of publication 10 October 2024; date of current version 26 November 2024. This work was supported in part by the Superior Energy-Efficient materials and Devices (SUPREME) and Center for Processing with Intelligent Storage and Memory (PRSIM), two of the Semiconductor Research Corporation (SRC)/Defense Advanced Research Projects Agency (DARPA) Joint University Microelectronics Program (JUMP) 2.0 Centers; and in part by NSF under Grant 2344819. The review of this letter was arranged by Editor M. Kobayashi. *(Corresponding author: Zijian Zhao.)*

Zijian Zhao, Yixin Qin, Jiahui Duan, YuShan Lee, and Kai Ni are with the Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556 USA (e-mail: zzhao24@nd.edu).

Suhwan Lim, Kijoon Kim, Kwangsoo Kim, Wanki Kim, and Daewon Ha are with Samsung Electronics Company Ltd., Hwaseong-si, Gyeonggi-do 18448, Republic of Korea.

Vijaykrishnan Narayanan is with the Department of Computer Science and Engineering, The Pennsylvania State University, State College, PA 16801 USA.

Color versions of one or more figures in this letter are available at https://doi.org/10.1109/LED.2024.3477510.

Digital Object Identifier 10.1109/LED.2024.3477510

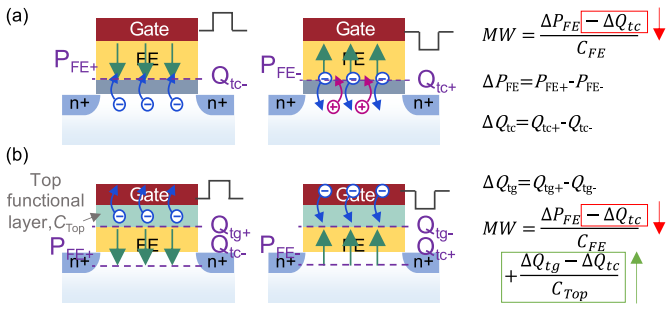


Fig. 2. (a) Channel-side injection of FeFETs degrades MW while (b) the gate-side injection pumped by the polarization switching realizes a large MW.

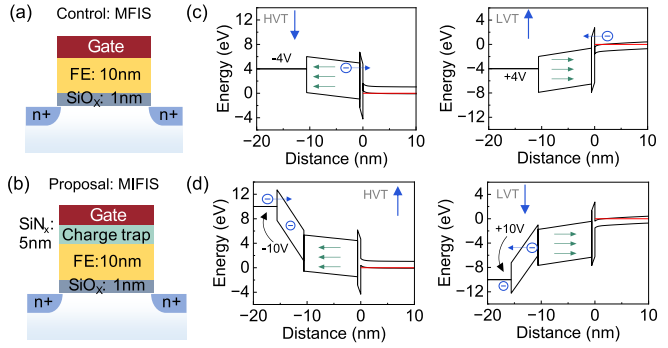


Fig. 3. Device schematics of (a) the control and (b) proposed designs. (c-d) TCAD simulated band diagrams during reset (HVT) and set (LVT) operations. The blue arrows represent the impact of charge trapping/detrapping on the V_{TH} state.

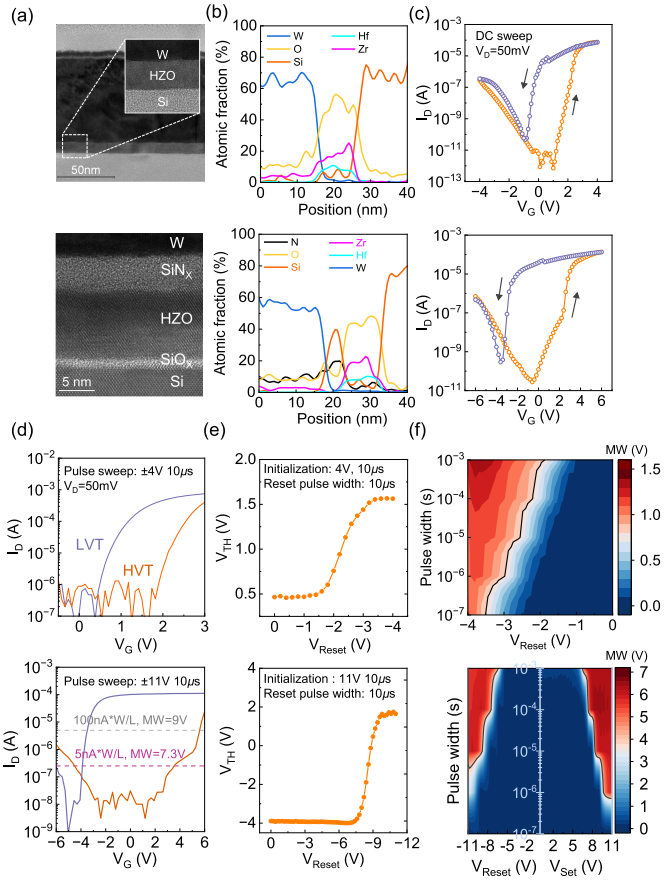


Fig. 4. Comparison between MFIS (upper) and MIFIS (lower). (a) TEM images for the gate stack. (b) Element fraction vertically along the gate stack. (c) DC I_D-V_G curves. Counterclockwise for both. (d) Pulsed I_D-V_G measured after reset/set pulses. (e) V_{TH} as a function of reset voltage amplitude. (f) Switching dynamics in terms of pulse width and amplitude. W/L = 50μm/1μm for all.

design MFIS, which is a conventional FeFET featuring 10 nm ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ layer. A 1 nm SiO_X layer is used as the interfacial layer (IL). Fig. 3(b) shows the proposed design MIFIS. A charge trapping layer, i.e., SiN_X, is inserted on the top of the ferroelectric layer. TCAD simulated band diagrams of the two designs for both reset and set operations are shown in Fig. 3(c) and (d) for the control and proposed design, respectively. For the control MFIS, the applied negative gate bias repels electrons from the HZO layer to the channel while the positive gate bias attracts electrons from the channel to the HZO layer, resulting in a reduced MW. In contrast, when a negative gate bias is applied to MIFIS, the electrons are injected from the gate side into SiN_x and get trapped. When a positive voltage is applied, the trapped electrons in the SiN_X layer will detrap to the gate. The trapped electrons will elevate the HVT and the de-trapped electrons will lower the LVT. Both of these operations will increase the MW. Moreover, the trapped electrons in SiN_X can compensate the polarization that points toward the channel, which therefore helps retain the trapped electrons even without a blocking layer, resulting in good retention [9]. Therefore, the channel side injection in the control design reduces MW while the top functional layer can enhance MW through charge trapping.

The device fabrication starts on a P-type silicon substrate. Screen oxide is deposited for ion implantation. After phosphorus ion implantation and activation, the isolation oxide in the gate area is removed and the gate area is cleaned for 10 nm $Hf_{0.5}Zr_{0.5}O_2$ and 5 nm SiN_X gate dielectric deposition through atomic layer deposition (ALD) at 250°C. Source/drain via is opened by reactive-ion etching (RIE) and buffered oxide etch (BOE). A 100 nm thick tungsten (W) layer is sputtered on the wafer for source, drain, and gate metal. The device is finally annealed in the forming gas (N_2+H_2, 350°C) and N_2 (500°C) for ferroelectric crystallization. The control sample does not have the SiN_X deposition.

III. Results and Discussion

Fig. 4(a) shows the transmission electron microscopy (TEM) cross sections of MFIS and MIFIS FeFET gate stack. It shows a crystalline ferroelectric film in both designs. Fig. 4(b) shows the atomic composition vertically along the gate stack. HZO and SiN_X distribution is confirmed in the MIFIS FeFET. Fig. 4(c) shows DC I_D-V_G sweeps in both devices. Counterclockwise hysteresis are observed, suggesting both devices are not observing significant channel side injection. The pulsed I_D-V_G curves are shown in Fig. 4(d). The MFIS sample shows a MW of 1.4 V with pulses of ±4 V 10 μs while the MIFIS sample shows a much larger MW. Depends on the extraction standard (i.e., different constant current), the MW can be between 7.3 V and 9.0 V. The noise floor is high because the current measurement range is set to be high in order to fully show the on state current. The V_{TH} as a function of voltage amplitude show a highly efficient write process, where even 10 V, 10 μs write pulse can fully saturate the switching (Fig. 4(e)). Fig. 4(f) shows the full switching dynamics, demonstrating different combinations

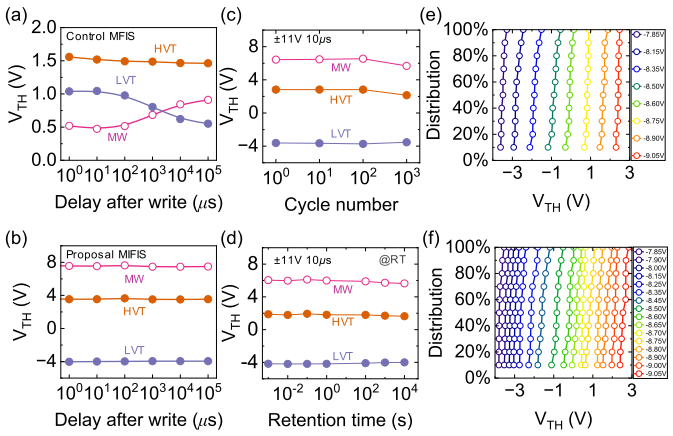
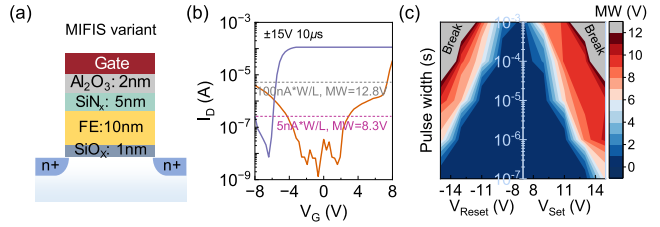


Fig. 5. V_{TH} vs. delay between read and write for (a) MFIS control sample and (b) Proposed MIFIS sample. The proposal shows immediate read-after-write feature. (c) Endurance>1000 cycles is shown. (d) 10^4s retention. It is also feasible to demonstrate (e) TLC and (f) QLC operation. W/L = 50μm/1μm for all.



(d)	[7]	[9]	[12]	[13]	This work
Stack height	19nm	N/A	20nm	N/A	15nm (17nm)
Write voltage	12V	~16V	~10V	~16V	11V (15V)
Speed	10μs	N/A	<0.1μs	N/A	1μs
MW	7V*	5.5V	~3V-4V	10.5V	6-8V (8-13V)

*Results based on C-V measurement

Fig. 6. (a) Another MIFIS variant with 2nm Al_2O_3 is also developed, which (b) shows an even large MW. (c) Switching dynamics of the device. (d) Our device shows great promise compared with other large MW FeFETs. W/L = 50μm/1μm for (b) and (c).

of write pulses and its corresponding MW. These results suggest that a significant gate-side injection is happening during polarization switching. Charges are stored and repelled by the applied gate voltage and held by the ferroelectric polarization. Therefore, the proposed MIFIS greatly surpasses the control FeFET MW, though they have the same ferroelectric thickness.

In contrast to the control MFIS, which typically requires a significant read delay after write (Fig. 5(a)), the proposed MIFIS FePFET shows immediate read-after-write (Fig. 5(b)), suggesting a negligible channel-side injection. Endurance cycling is shown in Fig. 5(c). The gate-side injection also improves retention, as shown in Fig. 5(d), where no degradation is observed at room temperature [9]. With a large MW, the proposed MIFIS FePFET can enable triple-level cell (TLC) (Fig. 5(e)) and quad-level-cell (QLC) (Fig. 5(f)). We have also designed a MIFIS variant, where a 2 nm Al_2O_3 is inserted above SiN_X (Fig. 6(a)), which shows an even larger MW (8.3 V-12.8 V) (Fig. 6(b)). The full switching dynamics (Fig. 6(c)) also show an efficient switching. Fig. 6(d) benchmarks most of the large MW FeFETs, highlighting the great promise of our design [7], [9], [12], [13].

IV. Conclusion

In this work, we have demonstrated two effective designs that can facilitate gate-side injection to enhance the FeFET MW. With the help of SiN_X in the MIFIS stack of the FePFET, we have successfully demonstrated a MW between 6 V-8 V with a write pulse of 11 V 1 μs. Therefore this stack, with further optimization, can be a promising candidate for next generation vertical NAND.

References

[1] R. Micheloni, L. Crippa, and A. Marelli, *Inside NAND Flash Memories*. Cham, Switzerland: Springer, 2010, doi: 10.1007/978-90-481-9431-5.

[2] B. Prince, *Vertical 3D Memory Technologies*. Hoboken, NJ, USA: Wiley, 2014, doi: 10.1002/9781118760475.

[3] C. Sandhya, U. Ganguly, N. Chattar, C. Olsen, S. M. Seutter, L. Date, R. Hung, J. M. Vasi, and S. Mahapatra, "Effect of SiN on performance and reliability of charge trap flash (CTF) under Fowler–Nordheim tunneling program/erase operation," *IEEE Electron Device Lett.*, vol. 30, no. 2, pp. 171–173, Feb. 2009, doi: 10.1109/LED.2008.2009552.

[4] K. Florent, M. Pesic, A. Subirats, K. Banerjee, S. Lavizzari, A. Arreghini, L. D. Piazza, G. Potoms, F. Sebaai, S. R. C. Mcmitchell, M. Popovici, G. Groeseneken, and J. Van Houdt, "Vertical ferroelectric HfO_2 FET based on 3-D NAND architecture: Towards dense low-power memory," in *IEDM Tech. Dig.*, Dec. 2018, pp. 2–5, doi: 10.1109/IEDM.2018.8614710.

[5] Z. Zhao, Y. Xu, J. Read, P.-K. Hsu, Y. Qin, T.-J. Huang, S. Lim, K. Kim, K. Kim, W. Kim, D. Ha, T. Kämpfe, S. George, X. Gong, S. Datta, S. Yu, V. Narayanan, and K. Ni, "In-situ encrypted NAND FeFET array for secure storage and compute-in-memory," in *IEDM Tech. Dig.*, Dec. 2023, pp. 1–4, doi: 10.1109/IEDM45741.2023.10413774.

[6] C.-Y. Liao, K.-Y. Hsiang, F.-C. Hsieh, S.-H. Chiang, S.-H. Chang, J.-H. Liu, C.-F. Lou, C.-Y. Lin, T.-C. Chen, C.-S. Chang, and M. H. Lee, "Multibit ferroelectric FET based on nonidentical double $HfZrO_2$ for high-density nonvolatile memory," *IEEE Electron Device Lett.*, vol. 42, no. 4, pp. 617–620, Apr. 2021, doi: 10.1109/LED.2021.3060589.

[7] D. Das, H. Park, Z. Wang, C. Zhang, P. V. Ravindran, C. Park, N. Afroze, P.-K. Hsu, M. Tian, H. Chen, W. Chern, S. Lim, K. Kim, K. Kim, W. Kim, D. Ha, S. Yu, S. Datta, and A. Khan, "Experimental demonstration and modeling of a ferroelectric gate stack with a tunnel dielectric insert for NAND applications," in *IEDM Tech. Dig.*, vol. 105, Dec. 2023, pp. 1–4, doi: 10.1109/IEDM45741.2023.10413697.

[8] H. J. Kim, M. H. Park, Y. J. Kim, Y. H. Lee, W. Jeon, T. Gwon, T. Moon, K. D. Kim, and C. S. Hwang, "Grain size engineering for ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ films by an insertion of Al_2O_3 interlayer," *Appl. Phys. Lett.*, vol. 105, no. 19, Nov. 2014, Art. no. 192903, doi: 10.1063/1.4902072.

[9] S. Lim, T. Kim, I. Myeong, S. Park, S. Noh, S. M. Lee, J. Woo, H. Ko, Y. Noh, M. Choi, K. Lee, S. Han, J. Baek, K. Kim, J. Kim, D. Jung, K. Kim, S. Yoo, H. J. Lee, S.-G. Nam, J.-S. Kim, J. Park, C. Kim, S. Kim, H. Kim, J. Heo, K. Park, S. Jeon, W. Kim, D. Ha, Y. G. Shin, and J. Song, "Comprehensive design guidelines of gate stack for QLC and highly reliable ferroelectric VNAND," in *IEDM Tech. Dig.*, Dec. 2023, pp. 1–4, doi: 10.1109/IEDM45741.2023.10413820.

[10] S. R. Rajwade, T. A. Naoi, K. Auluck, K. Jayant, R. B. Van Dover, and E. C. Kan, "Ferroelectric-assisted dual-switching speed DRAM–Flash hybrid memory," *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 1944–1950, Jun. 2013, doi: 10.1109/TED.2013.2257787.

[11] K. Ni, P. Sharma, J. Zhang, M. Jerry, J. A. Smith, K. Tapily, R. Clark, S. Mahapatra, and S. Datta, "Critical role of interlayer in $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric FET nonvolatile memory performance," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2461–2469, Jun. 2018, doi: 10.1109/TED.2018.2829122.

[12] T. Ali, P. Polakowski, K. Kühnel, M. Czernohorsky, T. Kämpfe, M. Rudolph, B. Pätzold, D. Lehninger, F. Müller, R. Olivo, M. Lederer, R. Hoffmann, P. Steinke, K. Zimmermann, U. Mühle, K. Seidel, and J. Müller, "A multilevel FeFET memory device based on laminated HSO and HZO ferroelectric layers for high-density storage," in *IEDM Tech. Dig.*, Dec. 2019, pp. 28.7.1–28.7.4, doi: 10.1109/IEDM19573.2019.8993642.

[13] S. Yoon, S.-I. Hong, D. Kim, G. Choi, Y. M. Kim, K. Min, S. Kim, M.-H. Na, and S. Cha, "QLC programmable 3D ferroelectric NAND flash memory by memory window expansion using cell stack engineering," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, vol. 7, Jun. 2023, pp. 1–2, doi: 10.23919/vlsitechnologyandcir57934.2023.10185294.