Clarifying the Role of Ferroelectric in Expanding the Memory Window of Ferroelectric FETs with Gate-Side Injection: Isolating Contributions from Polarization and Charge Trapping

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***Abstract*—In this work, we performed a comprehensive experimental and modeling study, clarifying the role of ferroelectric materials in boosting the memory window of FeFETs with gate-side charge injection for the first time. We separated the ferroelectric contributions to the memory window into remnant polarization and top charge trap layer (CTL) trapping. Our findings demonstrate that: (i) Ferroelectric materials enhance the memory window in two ways: by switched more polarization when CTL traps more, which provides screening charges, and through their super-linear *Q-V* relationship that boosts the CTL electric field and enhances charge trapping; (ii) The contributions from polarization and CTL trapping mutually reinforce each other, resulting in a larger memory window compared to a ferroelectric + dielectric stack or a high-κ + CTL stack, where only one factor is active; (iii) Combined experimental data and TCAD simulations confirm that approximately one-third of the memory window is due to increased polarization, while two-thirds result from CTL trapping; (iv) The memory window can be further enhanced with a blocking oxide on top of the CTL, achieving up to a 16V window with an ONO blocking oxide.**

I. Introduction

The insatiable appetite for high density storage, especially in the era of data generation at an exponential rate and the large language models exploding, calls for higher capacity and lower power storage. Vertical NAND flash has been fueling this paradigm shift due to its cost efficiency and clear scalable path. However, such a scaling is met with significant challenges related with the poor write efficiency of Flash. Because of the inefficient tunneling process, flash memory write pulse voltage and pulse width are excessive, posing significant challenges in further scaling along the XY and Z dimensions. To address this challenge, recently, FeFET, has been shown to be highly promising by incorporating gate side injection (Fig.1(a)). It is known that in the conventional FeFET, the channel side charge injection causes many reliability concerns, as the charge trapping counteracts the polarization induced V_{TH} shift. However, if the gate side injection can be induced, rather than the channel side injection, the charge trapping can help boost the memory window [1]. There have been many promising reports that show a large memory window suitable for vertical NAND application (Fig.1(b)). Fig.1(c) summarizes the reported FeFET memory window including the conventional ones (i.e., follow a linear dependence on the ferroelectric thickness) and the ones exploit the gate side injection. Though this memory window boost is intuitive, the exact role that ferroelectric plays has not been clarified, which is critical for future memory optimization and reliability improvement. This work aims at clarifying the ferroelectric role and provides the insights.

There are two components in the memory window, one from the remnant polarization and one from the gate side charge trapping. Though polarization is present in all kinds of FeFET, the FeFET with top charge trap layer (CTL) boosts the switchable polarization, compared with the FeFET with only top dielectric without any trapping (Fig.2(a)). This is because the trapped charge in the gate side acts as screening charge, which can help polarization switching. To identify the role of ferroelectric in inducing charge trapping, it is important to compare with the stack with high-κ (HK) dielectric and the top CTL, in which case, no polarization is present. Looking at the *Q-V* relationship, the super-linear *Q-V* of FE can help reduce the required FE voltage drop compared with the HK for the same charge or induce more charge switching for the same voltage drop. From this analysis, it is clear that polarization and gate side charge trapping reinforce each other, thus jointly enhancing the window. In this work, we are clarifying such an interaction and separating each component in memory window.

II. Farbication Process

For a comprehensive study of the impact of gate stack layers on FeFET performance, experimental investigations were conducted in this work. Fig.3(a) demonstrates the control sample with10-nm-thick HZO and other three stacks: 10nm HZO with 5nm SiN_x on top (FE+CT), 10nm HfO_2 with 5nm SiN_x on top (HK+CT), and 10nm HZO with 5nm Al_2O_3 on top (FE+DE). The integration fabrication process flow is depicted in Fig.3(b). The fabrication is carried out on a P-type silicon. After phosphorus ion implantation and activation, the isolation oxide in the gate area is removed. The gate dielectric HZO, HfO_2, SiN_x, Al_2O_3 are deposited through atomic layer deposition (ALD) at 250°C. As for the FE+CT gate stack, additional 1nm and 2nm Al_2O_3 and 2nm SiO_2 are deposited to study the effect of blocking oxide. Moreover, the common flash structure $SiO_2/SiN_x/SiO_2$ (ONO) is fabricated as well. Tungsten (W) layer is sputtered serve as source, drain, and gate metal, followed by RTP annealing in forming gas (N_2+H_2, 350°C) and N_2 (500°C). Fig.3(c) shows the top view scanning electron microscopy (SEM). Fig.3(d) shows the transmission

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electron microscopy (TEM) of cross-sections of the four gate stacks of FeFET, and the energy-dispersive x-ray spectroscopy (EDS) line scans are shown in Fig.3(e), respectively. These TEM and elemental profiles confirm the intended thickness and material in the gate stack designs. The pulse I_D-V_G of top charge trapping layer and bottom ferroelectric layer were shown in Fig.3(f) and (g). The experimental results demonstrated FeFET with CTL is larger than dielectric layer (i.e., weaker charge trapping) and that with ferroelectric layer is larger than that with high-κ dielectric.

III. Clarifying the Role of Ferroelectrics

For detailed study, TCAD models are first built and calibrated based on the 2nm blocking oxide structure (Fig.4(a)). Ferroelectric Preisach model and SiN_x charge trap layer parameters are also given. The TCAD simulation can well reproduce experimental results (Fig.4(b)). With such models, the two contributors are studied: 1) Remnant polarization (P_{FE}), and 2) the super-linear Q-V. To study the first factor, TCAD simulations comparing the scenarios of enabling or disabling the top CTL trapping are conducted. Fig.5 (a) shows the average polarization at V_G=0V after write. It shows that the switched polarization is enhanced 3.3x with the CTL trapping compared with the one without trapping. As a result, MW can be enhanced due to $\Delta P_{FE}/C_{FE}$ component. Fig.5(b) shows two cycles of program/erase waveforms (±15V, 10μs) and the corresponding trapped electron/hole density. In Fig. 5(c), experimental I_D-V_G characteristics of 10nm HZO control FeFET (±4V, 10μs) and FE+CT with 2nm Al_2O_3 (±15V, 10μs) are compared, where MWs are 1.6V and approximately 12V, respectively. TCAD simulated I_D-V_G (Fig. 5(d)) are consistent with the experiments. Using the simulated results, the pure P_{FE} contribution is estimated to be 3.6V and the remaining 8.4V memory window comes from the CTL charge trapping (Fig.5(d)). **This clarifies the pure remnant polarization P_{FE} provides around 1/3 contribution in the enlarged MW, whereas 2/3 MW is due to the charge trapping effect.**

To show that the super-linear Q-V of ferroelectric can boost MW, a hypothetical nonlinear dielectric (Fig.6(a)) was implemented in TCAD. Fig.6(b) presents the Q-V implemented in TCAD with different nonlinearity. When the same voltage is applied, super-linear dielectric can gain a larger amount of charge (ΔQ_{NL}) than linear dielectric charge (ΔQ_L). This obviously induces higher injected charge in CTL to increase MW. And the experimental pulse I_D-V_G between FE+CT and HK+CT was shown in Fig. 6(c), which verifies the FE could achieve higher MW compared to HK. But the experiment also includes the polarization contribution (~4V in Fig.5(c) and (d)), excluding which the pure charge trapping contribution is about 4.7V, 1.7x of the HK+CT device. Fig.6(d) shows trapped electron density in the CTL during -15V program and electron loss after program. It shows that the larger the nonlinearity, the higher the trapped electrons. This charge trapping enhancement is originated from the enhanced electric field in the CTL (Fig.6(e)) as the FE field reduces with stronger nonlinearity.

After clarifying the role of ferroelectric, next with the help of TCAD simulations, the two components are further investigated by comparing the FE+CT and HK+CT stacks and cross-validated with prior analysis. The electric field in the CTL during both program (Fig.7(a)) and erase (Fig.7(b)) shows an enhanced CTL field and reduced FE field compared with HK case. The corresponding band diagrams for program (Fig.7(c)) and erase (Fig.7(d)) also shows the reduced FE field compared with HK. As a result, the trapped electrons during program (Fig.7(e)) and trapped holes during erase (Fig.7(f)). Fig.7(g) summarizes the trapped electrons/holes/space charges during programming/erase. From these results, it can be estimated that the HK+CT will exhibit around 4.6V window while the trapped contributed window is 8V for the FE+CT case, again 1.7x of the HK case, consistent with experiment.

IV. Characteristics of Gate Side Injection FeFETs Without and With Blocking Oxide

Further analysis of the fabricated devices is first conducted on the devices without a block oxide. Fig.8(a) and (b) shows the I_D-V_G curves with different programming voltages when initialized at the low-V_{TH} (LVT) and high-V_{TH} (HVT) state, respectively. The corresponding V_{TH} as a function of programming voltages are summarized in Fig.8(c) and (d), respectively for three different stacks, i.e., FE+CT, FE+DE, and HK+CT. It clearly shows that the slope of the incremental step pulse programming (ISPP) (Fig.8(e) and (f)) of the HK+CT is below 1, typically present for flash-based device, indicating that the V_{TH} increase is theoretically below the step size of programming pulse [2]. However, with the mutual reinforcement of the polarization and charge trapping, the ISPP slope can be well above 1, suggesting superior tuning efficiency of the FE+CT device. Fig.9(a) and (b) shows the band diagrams during zero bias convention for FE+CT and HK+CT. Due to the presence of polarization, the electric field can help retain the trapped charges (Fig.9(c)), thus slowing the charge loss during retention compared with HK+CT. Fig.9(d) compares the retention between the two stacks, consistent with the theoretical picture shown in Fig.9(a) and (b).

Next the impact of blocking oxides on the FeFET memory window is presented. Fig.10(a)-(c) shows the TEM, elemental mapping, and atomic composition along the gate stack with 2nm Al_2O_3 blocking oxide, respectively. The corresponding DC and pulsed I_D-V_G curves of different blocking oxide thicknesses shows that the MW increases with the blocking oxide thickness that 2nm Al_2O_3 has about 12V window with ±15V, 10μs programming pulses. In all the devices, an ISPP slope larger than 1 is observed. When comparing different blocking oxides (Al_2O_3 vs. SiO_2 vs. $SiO_2/SiN_x/SiO_2$), Al_2O_3 shows a similar window as SiO_2 while the ONO has a larger window, but also need a larger write voltage (Fig.10(i) and (j)).

V. Conclusion

This work firstly clarifies ferroelectric material and charge trapping mechanisms contributing to boosting MW in gate-side-injection FeFET through simulation and experimental results. This helps the better understanding and guide in FeFET design in 3D NAND with higher storage. With ±15V, 10μs pulse, FE+CT+2nmAl_2O_3 gate stack can reach to 12V memory window. Optimizing the gate stack (such as ONO structure) could potentially achieve better performance in future memory applications.

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Understanding the Role of Ferroelectric in Boosting the Memory Window of FeFET with Gate Side Injection

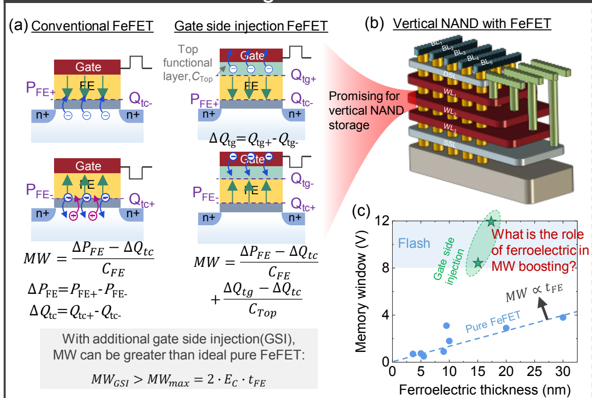


Fig.1. (a) Compared to conventional FeFET, MW can be enhanced by gate-side-injection (GSI) FeFET. (b) 3D Vertical NAND structure with GSI FeFET. (c) It is unclear what the role FE plays in boosting the GSI FeFET and studied here.

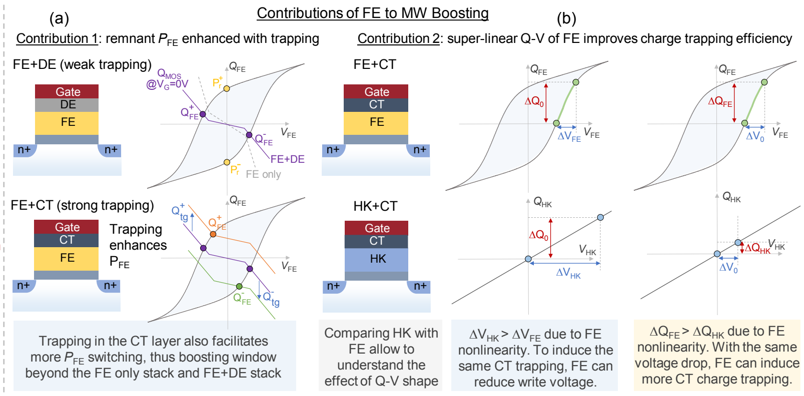


Fig.2. (a) Remnant polarization in ferroelectric can facilitate charge trapping, and vice versa to facilitate FE switching. (b) The super-linear Q-V curve in FE requires less applied voltage than high-κ stack to trap the same mount of charge, or more trapped charge under the same voltage, which improves the trapping efficiency.

Different Stacks Fabricated to Identify the Role of Ferroelectrics in Boosting the Window

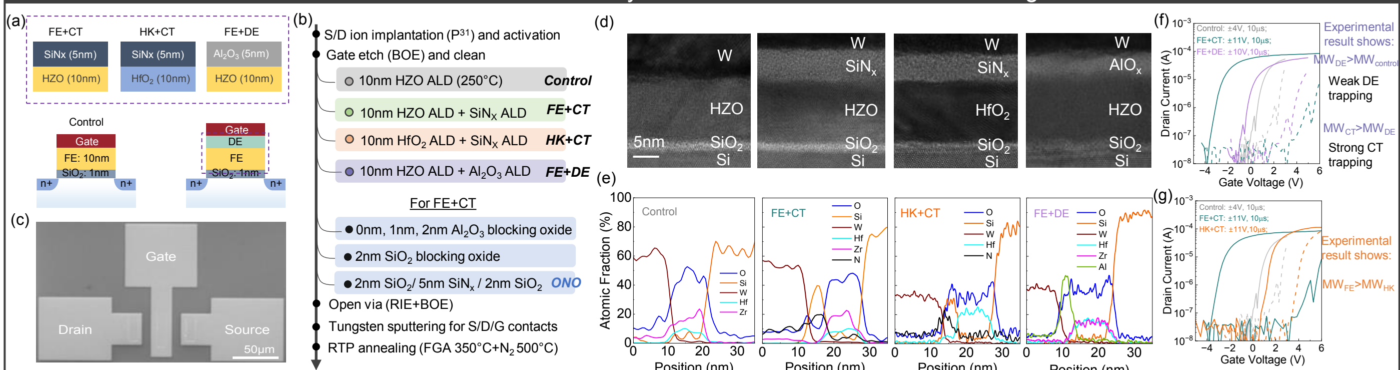
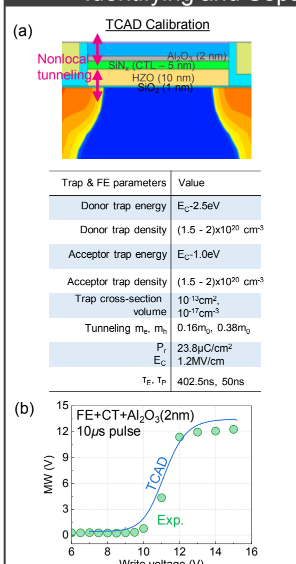


Fig.3. (a) FeFET gate stacks with HZO control sample, and three different FeFET stacks. (b) Integration process flow of proposed FeFETs. (c) SEM top view of fabricated FeFET. (d) Cross-sectional TEM images of proposed FeFETs. (e) Atomic composition of the gate stack cross-sectional direction. (f) Pulsed I_D-V_G comparison between FeFET with top CTL and dielectric layer, and CT stack shows improved MW. (g) Pulsed I_D-V_G comparison between ferroelectric and high-κ with CTL, which shows that FE improves MW. The AlO_x DE shows weak trapping comparing the control.

Identifying and Separating the Window Enhancement to Increased Remnant Polarization and Boosted CTL Trapping



Trap & FE parameters	Value
Donor trap energy	E_C-2.5eV
Donor trap density	(1.5 - 2)x10^{20} cm^{-3}
Acceptor trap energy	E_C-1.0eV
Acceptor trap density	(1.5 - 2)x10^{20} cm^{-3}
Trap cross-section / volume	$10^{-13}cm^2$, $10^{-17}cm^{-3}$
Tunneling m_e, m_h	0.16m_0, 0.38m_0
P_r, E_C	23.8μC/cm², 1.2MV/cm
τ_E, τ_P	402.5ns, 50ns

Fig.4. (a) TCAD calibration of FeFET structure and the modeling parameters table. (b) The TCAD models are well calibrated with and experimental results.

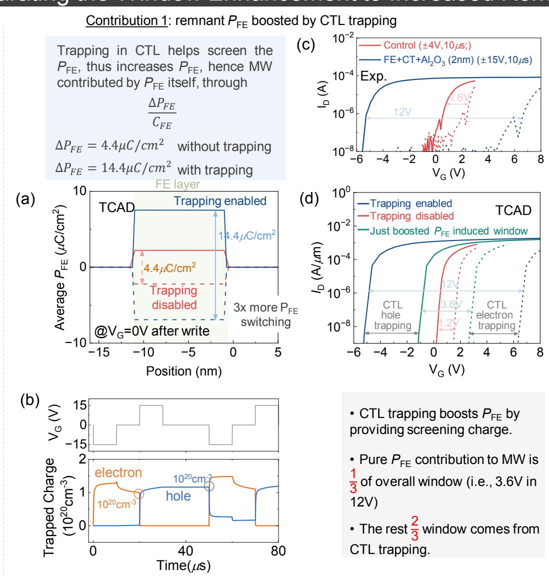


Fig.5. (a) Extracted polarization with and without charge trapping activated after write. (b) Extracted electron and hole charge density under program and erase versus time. (c) Pulsed I_D-V_G of control sample and FE+CT+Al_2O_3 FeFET. (d) I_D-V_G simulation comparison with and without charge trapping, and the separated contribution of P_{FE}.

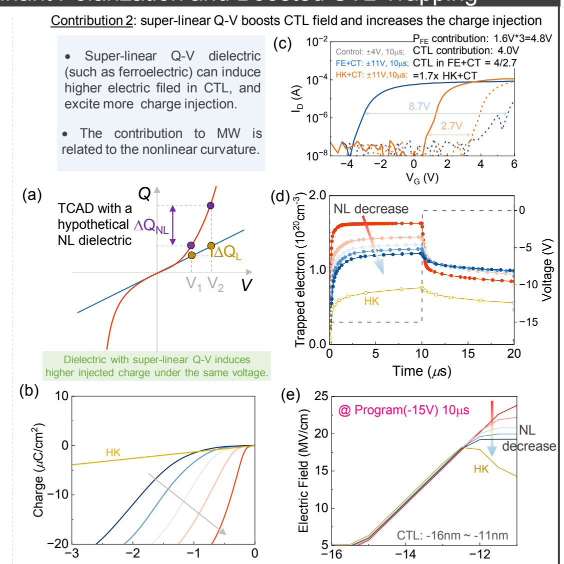


Fig.6. (a) Comparison between linear and super-linear dielectric Q-V. (b) Different curvature of non-linear dielectric Q-V in TCAD. (c) Pulse I_D-V_G of FE+CT and HK+CT gate stack. (d) Extracted trapped electron in different curvature of non-linear Q-V dielectric and HK stack. (e) Extracted electric field in CTL after program .

Detailed Analysis of Both Window Contributors Through Comparative Study of FE+CT and HK+CT Stacks

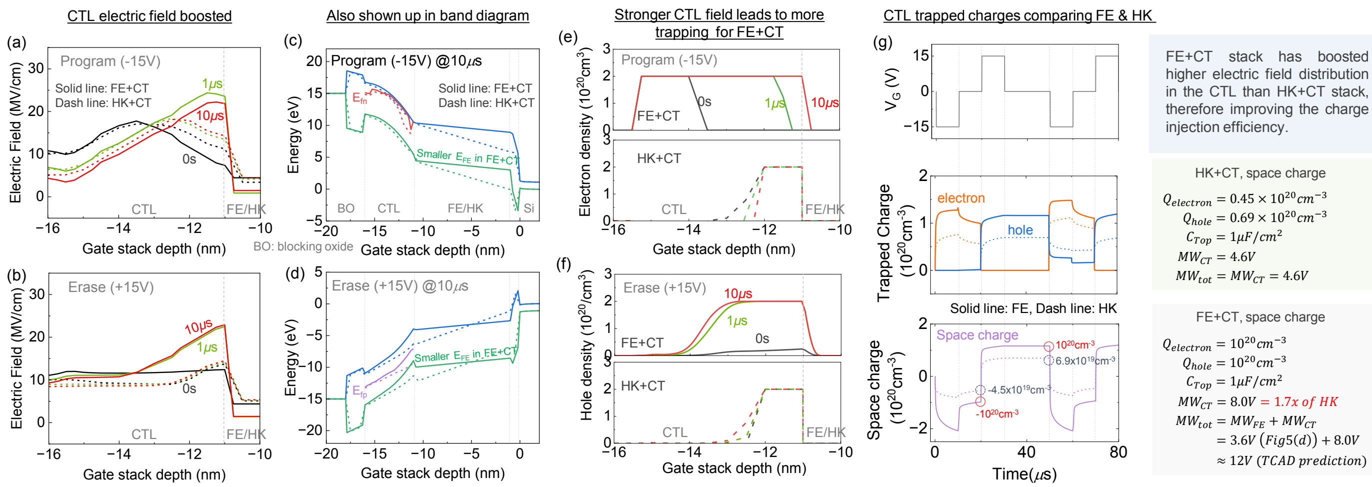
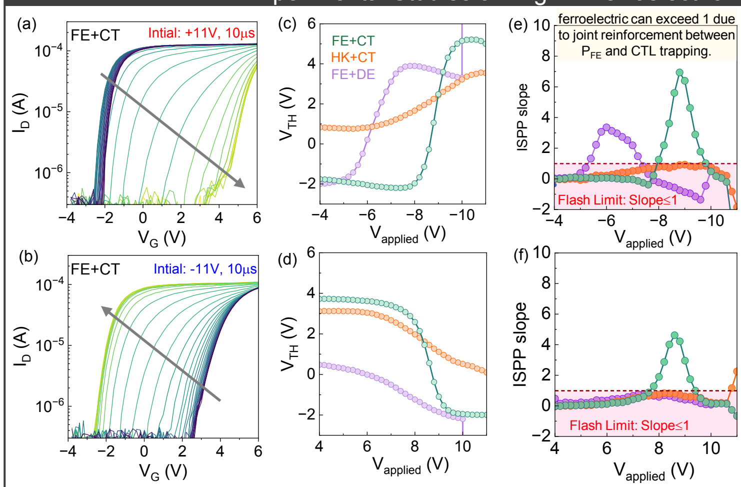


Fig.7. In program (-15V, 10μs), FE+CT and HK+CT comparison on (a) electric field on CTL, (c) energy band diagram, (e) trapped electron density. In erase (+15V, 10μs), FE+CT and HK+CT comparison on (b) electric field on CTL, (d) energy band diagram, (f) trapped hole density. (g) Waveforms of applied program/erase cycles, extracted electron and hole density, and total space charge in FE+CT and HK+CT in program/erase process.

Experimental Studies on High-κ/Ferroelectric Impact on Charge Trapping Layer (CTL)



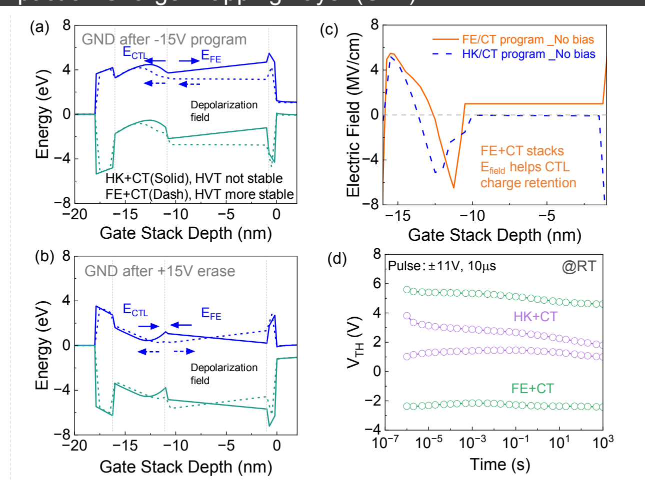


Fig.8. Switching dynamics I_D-V_G of FE+CT stack under initialization of (a) +11V, 10μs, (b)-11V,10μs. Extracted (c) low V_{TH}, and (d) high V_{TH} and the corresponding (e), (f) ISPP slope of three different gate stacks.

Fig.9. Band diagram of FE+CT and HK+CT (a) after program bias removed, (b) after erase bias removed. (c) Electric field after program bias removed. (d) Retention comparison FE+CT and HK+CT.

The Impact of Blocking Oxides on the FeFET Characteristics

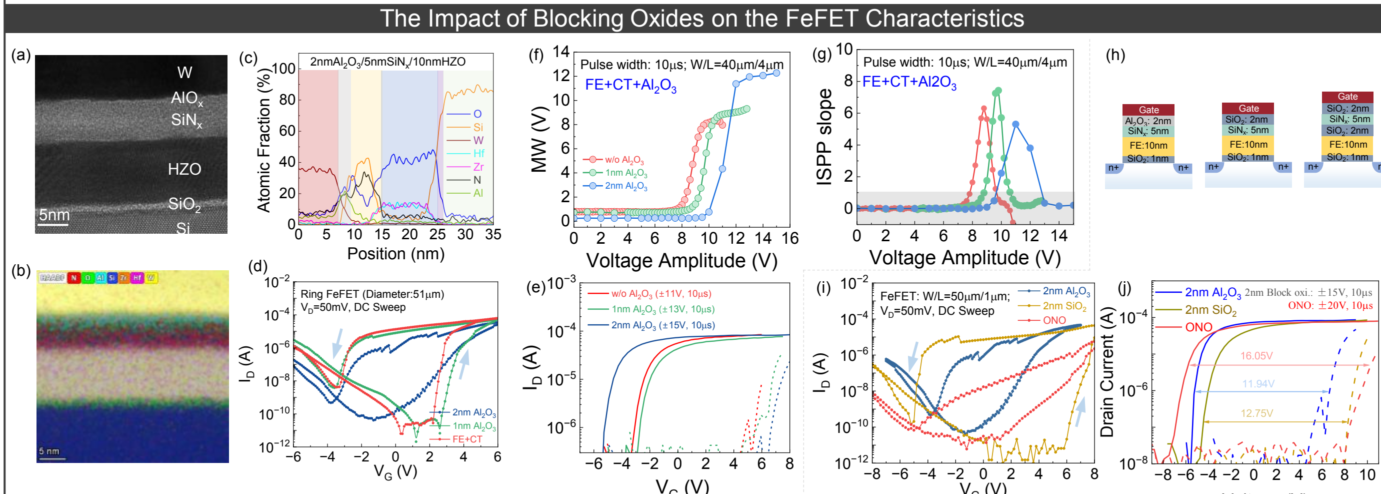


Fig.10. (a) TEM image of FE+CT+2nm Al_2O_3 structure. (b) Elemental mapping of the gate stack with blocking oxide. (c) Atomic composition of the gate stack cross-sectional direction. (d) DC I_D-V_G with different blocking oxide thickness. (f) Pulse I_D-V_G with different blocking oxide thicknesses. (f) switching dynamics and (g) ISPP slope of different blocking oxide thickness. (h) Comparison between different blocking oxide layers: Al_2O_3, SiO_2, ONO structures in (i) DC I_D-V_G, (j) Pulse I_D-V_G measurement results.