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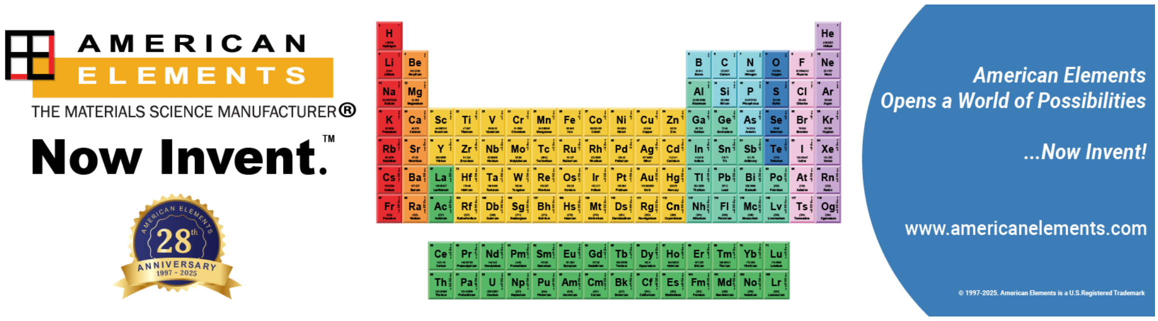

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Jayita Dutta,[1,a)] Rui Chen,[1] Virat Tara,[1] and Arka Majumdar[1,2,a)]

AFFILIATIONS

[1] Electrical and Computer Engineering (ECE) Department, University of Washington, Seattle, Washington 98195, USA
[2] Department of Physics, University of Washington, Seattle, Washington 98195, USA

[a)] **Authors to whom correspondence should be addressed:** jayitad@uw.edu and arka@uw.edu

ABSTRACT

Programmable photonic integrated circuits are expected to play an increasingly important role in enabling high-bandwidth optical interconnects and large-scale in-memory computing as needed to support the rise of artificial intelligence and machine learning technology. To that end, chalcogenide-based non-volatile phase-change materials (PCMs) present a promising solution due to zero static power. However, high switching voltage and a small number of operating levels present serious roadblocks to the widespread adoption of PCM-programmable units. Here, we demonstrate an electrically programmable wide bandgap Sb_2S_3-clad silicon ring resonator using a silicon microheater at a complementary-metal–oxide–semiconductor compatible voltage of <3 V. Our device shows a low switching energy of 35.33 nJ (0.48 mJ) for amorphization (crystallization) and reversible phase transitions with high endurance (>2000 switching events) near 1550 nm. Combining a volatile thermo-optic effect with non-volatile PCMs, we demonstrate 7-bit (127 levels) operation with excellent repeatability and reduced power consumption. Our demonstration of low-voltage and low-energy operation, combined with the hybrid volatile–nonvolatile approach, marks a significant step toward integrating PCM-based programmable units in large-scale optical interconnects.

I. INTRODUCTION

To support the rising demands of computing for artificial intelligence (AI), there is a clear need to transform both computing and communication systems.[1–6] On one hand, a large amount of data needs to move between electronic computers and servers. Optical interconnects present a promising solution thanks to their much lower latency and energy consumption compared to the traditional copper-based interconnects.[7–10] In particular, optical circuit switching systems are already being deployed in data centers,[11,12] as recently announced by Google. These switches are slow (e.g., Google is deploying micro-electro-mechanical switches), but they need to provide a very large change in optical properties with ultra-low loss. On the other hand, the growing demand for vector–matrix multiplication[13–16] poses a serious challenge for traditional computing architectures, including graphical processing units. This has led to an exploration of optical vector–matrix multiplication, which requires in-memory computing.[17–19] Both applications, optical circuit switching and vector–matrix multiplication, require ultra-compact, low-loss, programmable photonic units[20] with high endurance, compatibility with electronic integrated circuits (i.e., the actuation electrical power can be provided by on-chip circuits), and high bit-precision.[21–23]

While large-scale photonic integrated circuits (PICs) have now become available,[24–32] thanks to sophisticated fabrication techniques, truly programmable photonic circuits with the aforementioned properties remain missing.[33–36] We emphasize that most of the existing reconfiguration methods in integrated photonics are volatile (thermo-optic, free-carrier dispersion, and Pockels effect[37–42]) and are essentially optimized for high-speed switching. However, both optical circuit switching and vector–matrix multiplication will benefit from programmable photonic units, which are changed infrequently but have zero static power.[43–47] Chalcogenide phase-change materials (PCMs) offer a promising solution to more compact device size and zero static power owing to their strong optical index modulation $[\Delta n \sim O(1)]$ and zero static power consumption.[48–51]

PCMs possess two stable, reversibly switchable microstructural phases, namely, the amorphous phase (a-phase) and crystalline phase (c-phase), with significantly different optical refractive indices ($\Delta n \sim 1$). Due to their non-volatile phase transition under the ambient environment, PCMs do not require static power to maintain their state once switched. The large refractive index change (Δn) and non-volatility allow for the creation of compact, reconfigurable devices (~100 μm)[52,53] with zero static energy consumption.[50,54–58] Furthermore, PCMs are suitable for large-scale integration as they can be easily deposited by sputtering[50,54,56,58–62] or thermal evaporation[53] onto various integrated photonics material platforms, including silicon and silicon nitride. While traditional PCMs such as $Ge_2Sb_2Te_5$ (GST) and GeTe show strong optical absorption, emerging wide-bandgap PCMs, such as $Ge_2Sb_2SeTe_4$ (GSST),[63] Sb_2S_3,[64,65] and Sb_2Se_3,[66–69] offer new opportunities to reduce this absorption loss. These wide bandgap PCMs have garnered significant interest due to their potential for both large-area, endurable switching and repeatable, multilevel operation.[35,53,57,70–72] However, even though Sb_2Se_3 is also a promising PCM, selenium is highly toxic in nature.[73] A recent paper showed tuning of Sb_2Se_3 between its amorphous and crystalline states with a PIN heater,[69] which requires a high switching voltage (8.2 V for amorphization and 3.3 V for crystallization), incompatible with the standard driving voltage of Complementary-Metal–Oxide–Semiconductor (CMOS) electronic integrated circuits. Although the work showed both PCM and thermal tuning of the micro-ring resonators separately, the collective tuning was not demonstrated.

Notably, Sb_2S_3 has the widest bandgap among these emerging PCMs, providing transparency down to ~600 nm[66] in the amorphous phase. A previous experiment with Sb_2S_3 showed low-loss (<1 dB), endurability (>1000 cycles), and 5-bit operation by tuning PCM Sb_2S_3[51] and also its potential in high-volume manufacturing in 300-mm wafers.[61] However, the switching energy of the devices remained high, mainly limited by the sub-optimal design of our p++–i–n++ (PIN) doped silicon microheaters.[74] Moreover, due to the inherent stochastic switching behavior of the PCMs, the number of operation levels is limited.[75]

In this work, we show both low-energy switching of PCM Sb_2S_3 and a large number of intermediate levels at optical telecommunication wavelengths (C-band, ~1500–1560 nm). The low switching energy is achieved by optimizing our PIN microheater geometry. Both numerical and experimental results show that the switching energy monotonically reduces with the decrease in the intrinsic region width of the PIN microheater, although at the cost of a lower quality (Q) factor. An intrinsic region width of 0.9 μm is chosen to achieve a good trade-off, showing low switching voltages of less than 3 V (~25.7 mA current and 500 ns pulse duration, 35.33 nJ) and 1.6 V (~15 mA current and 20 ms pulse duration, 0.48 mJ energy) for amorphization and crystallization, respectively. This voltage and current can be easily provided by CMOS electronic integrated circuits. We show that such low power operations do not degrade the cyclability by demonstrating >10 000 switching events in total on a single device. Finally, we demonstrate ~7-bit operation (127 levels) using hybrid thermo-optic/PCM tuning, combining a coarse ~5 bit (22 levels) non-volatile tuning by PCM and a volatile finer tuning by thermo-optic. The CMOS compatible voltage/energy operation coupled with ~7-bit operation marks important steps toward PCM-based large-scale PIC systems.[28,76]

II. RESULTS

We use micro-ring resonators (MRRs) as the platform to demonstrate low-voltage, low-energy operation. Figure 1(a) shows the schematic of a silicon micro-ring resonator cladded with 10-μm-long, 0.45-μm-wide, and 20-nm-thick Sb_2S_3, and the cross-sectional view is on the right. The MRRs were fabricated on a standard silicon-on-insulator (SOI) wafer with a 220 nm silicon layer and a 2 μm buried oxide layer. All the rings have a bus-ring gap of 270 nm to achieve a near-critical coupling condition. The 500 nm wide waveguides were created by partially etching 120 nm of silicon. We then deposited 450 nm wide, 20 nm thick Sb_2S_3 stripes onto the SOI chip via sputtering and liftoff. The 50 nm smaller width compared to the waveguide compensates for the electron beam lithography (EBL) overlay tolerance and error from liftoff. The Sb_2S_3 films are electrically controlled via on-chip silicon PIN micro-heaters,[51,56,58] of which the intrinsic region width was varied from 0.9 to 1.9 μm to study its relationship with operation voltage, power, and Q-factor. The Sb_2S_3 stripes are encapsulated with 40 nm of thermal Al_2O_3 grown by atomic layer deposition (ALD) at 150 °C. This conformal encapsulation is critical for

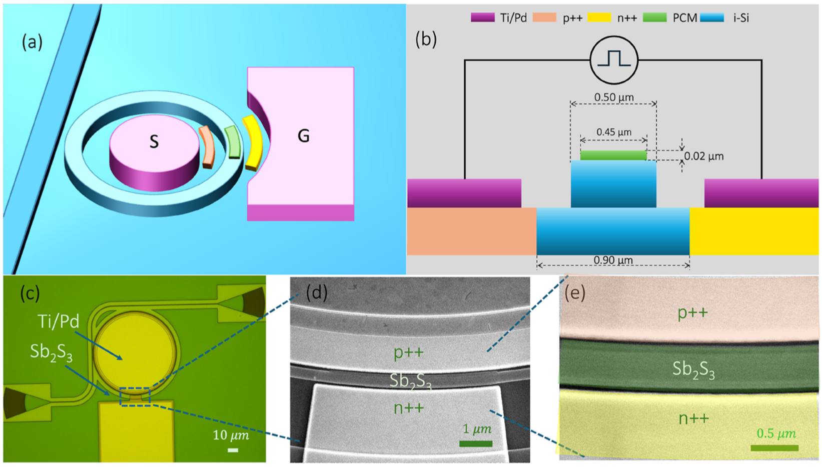

FIG. 1. A high Q ring resonator loaded with 10 μm long, 20 nm thick Sb_2S_3 (a). A schematic of the Sb_2S_3 loaded micro-ring resonator with low operation voltage and energy (b). A 2D schematic of the Sb_2S_3 loaded p++–i–n++ (PIN) micro-heater design (c). Optical microscope image of the micro-ring resonator (d). Scanning electron microscope (SEM) image of Sb_2S_3 loaded PIN micro-heater (e). Zoomed SEM view of Sb_2S_3 loaded PIN micro-heater. The Sb_2S_3 thin film, i-Si, n++, and p++ doped silicon regions are represented by false colors (green, blue, yellow, and orange, respectively).

preventing Sb_2S_3 from oxidation and thermal reflowing, which is essential for high endurance.[51] Figures 1(c) and 1(d) show the optical micrograph and scanning electron microscope (SEM) image of the MRR, respectively. Figure 1(e) shows a zoomed SEM image of a PIN micro-heater where the doping regions and Sb_2S_3 are false colored.

A. Optimization of operation voltage and switching energy by varying the intrinsic region width

We start with heat transfer simulations in COMSOL Multiphysics, where the intrinsic region width (w_i) of the PIN microheater is varied to optimize the switching energy. The COMSOL simulation couples semiconductor and heat transfer modules and, therefore, can capture the main physics of our device. The solid lines in Figs. 2(a) and 2(b) show the simulation results for w_i within 0.9 to 1.9 μm. We clearly see a monotonic reduction of the switching voltage and energy with the decrease in w_i. The increase in the amorphization voltage from 3 V at 0.9 μm to 5 V at 1.9 μm shows the importance of careful designing of the microheater geometry. We attribute this monotonic trend to two factors: (1) the increase in w_i increases the PIN diode resistance and reduces the current flow; and (2) the overall heating volume of the PIN microheater increases, thus requiring more energy. Importantly, the simulation shows that at w_i = 0.9 μm, CMOS-compatible pulses with 3 V amplitude (13.53 mA current) and 500 ns duration are already enough to amorphize the material. The Sb_2S_3 is heated above its melting temperature (801 ± 18 K[66]), after which it is quenched below the glass transition temperature of 573 K in 200 ns (quench rate ~2 K/ns).

Next, we experimentally validate our simulation results (the measurement results are shown by the circles in Fig. 2). The trend we observed in the experiment agrees qualitatively well with our simulation. The SEM images corresponding to different w_i are shown in Sec. 1 of the supplementary material (see Fig. 1 of the supplementary material). Experimentally, we have measured the switching conditions for partial amorphization for a fixed resonance wavelength shift of 0.12 nm (i.e., $\Delta\lambda$ = 0.12 nm) and not the maximum possible $\Delta\lambda$. This choice was made to ensure that the device is not damaged while finding the amorphization and crystallization conditions and all the devices with varying parameters can be measured. However, it is important to note that complete amorphization of Sb_2S_3 will require higher switching voltage and energy. For the PIN heater with w_i = 0.9 μm, complete amorphization of Sb_2S_3 will require higher voltage and energy by 10% and 47%, respectively, as shown in Sec. B and Sec. 2 of the supplementary material. The switching energy requirement is calculated as switching voltage multiplied by the estimated current from the measured IV curve multiplied by applied pulse duration. Furthermore, as shown in Figs. 2(a) and 2(b), the Q-factor decreases with the decrease in intrinsic region width and constitutes the design trade-off. As shown in Figs. 2(a) and 2(b), the energy requirement is higher by ~15% (~17%) for amorphization (crystallization) experimentally as compared to switching conditions computed for the center of PCM via COMSOL simulation (see the supplementary material, Secs. 2 and 3, Figs. 2 and 3). The observed higher energy requirement can be attributed to four factors: (1) in simulation, we have considered simplified 2D geometry to calculate the phase change requirement for the center of PCM but the actual geometry can be more complex, leading to non-uniform heat distribution and potentially higher energy requirements; (2) the actual kinetics of the phase-change process, including nucleation and growth rates, may be different in the experiment compared to the idealized rates assumed in simulations, requiring more energy to achieve a full phase transition in the experiment; (3) the interfaces between the PCM and surrounding materials can introduce additional thermal resistance or electrical contact resistance in reality as compared to the ones captured in simulation, leading to higher energy requirements in experiments; and (4) in reality there can be material inhomogeneity in terms of crystalline structure, or defect density, which can lead to different thermal and electrical properties compared to the idealized conditions used in simulations.[77–79] The variation in Q-factor and energy requirement with respect to variation in intrinsic region width measured across multiple devices is shown in the form of error bars in Figs. 2(a) and 2(b).

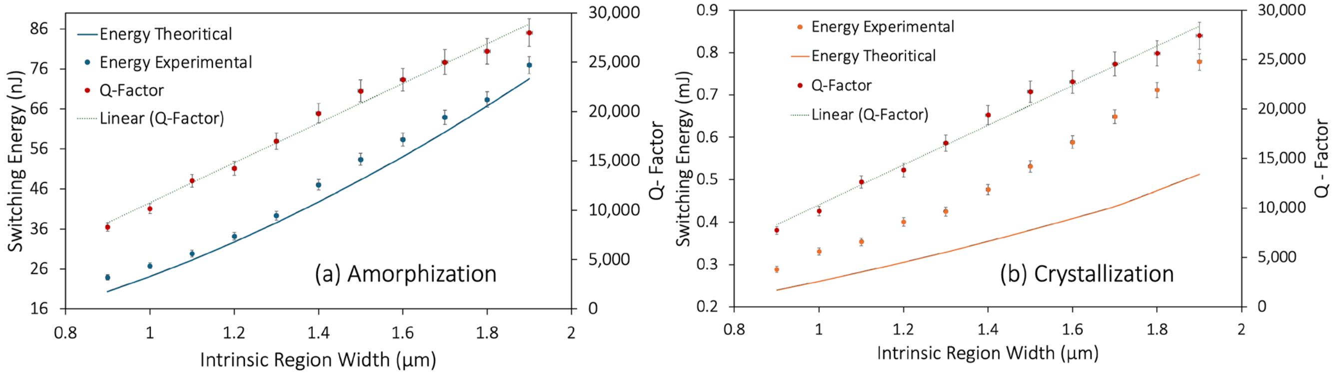

FIG. 2. Optimization of switching energy and Q-factor of Sb_2S_3 by varying the intrinsic region width of the PIN heater from 0.9 to 1.9 μm. (a).Variation from crystalline to partial amorphous state. (b) Variation from partial amorphous state to crystalline state. In both Figs. 2(a) and 2(b), the green dotted line acts as a guide to the eye to show the gradual increase in the Q-factor with the increase in intrinsic region width from 0.9 to 1.9 μm.

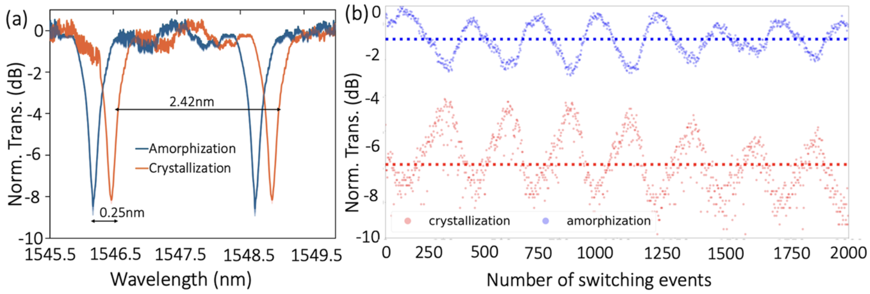

FIG. 3. Low power switching and endurance of Sb_2S_3 loaded micro-ring resonator with w_i = 0.9 μm. (a) Measured MRR spectra for crystallization (SET) and amorphization (RESET) (SET: 1.6 V, 20-ms-long, 0.48 mJ pulse to change Sb_2S_3 to the crystalline state; and RESET: 2.75 V, 500-ns-long, 35.33 nJ pulse to change Sb_2S_3 to the amorphous state). The spectra are averaged over five cycles, and the shadowed area shows the standard deviation. Norm. transmission stands for normalized transmission, normalized to a reference waveguide on the same chip. (b) Measured endurance for 2000 switching events (1000 crystallization and 1000 amorphization) with the same phase change conditions as mentioned in Fig. 3(a). The blue and orange scatterers represent the normalized transmission when Sb_2S_3 is in the amorphous and crystalline phases, respectively. The observed sinusoidal oscillation pattern in the endurance test is attributed to the self-heating effect of the silicon micro-ring resonator. The average transmission after amorphization and crystallization is indicated by the dotted lines. Norm. Trans. stands for normalized transmission, which is calculated as transmission (dB) = 10 $\times \log_{10}$ (transmitted power in mW), and the maximum transmission is normalized to 0 dB.

B. Low power actuation and endurance of Sb_2S_3 clad Si MRR

We then show more characterization results for the lowest voltage and energy device with w_i = 0.9 μm [Figs. 1(c)–1(e)]. The resonance spectra from 1545.5 to 1550 nm are shown in Fig. 3(a) (see Sec. 4 of the supplementary material for 1500–1560 nm). A resonance shift of ~0.25 nm is obtained [Fig. 3(a)] upon switching the Sb_2S_3 from the a-phase (blue) to the c-phase (orange). Considering the free spectral range of ~2.42 nm, this resonance shift amounts to a 0.2π optical phase shift per round trip. The observed condition for complete amorphization (RESET pulse) of Sb_2S_3 is a 500 ns pulse width at 2.75 V, which corresponds to a current of 25.7 mA and a switching energy of 35.33 nJ. The crystallization condition (SET pulse) is a 20 ms pulse at 1.6 V corresponding to a current of 15 mA and a switching energy of 0.48 mJ. The SET and RESET processes were repeated for five cycles, and the slight variation is shown as the standard deviation among the cycles by the shaded region in Fig. 3(a), showing excellent repeatability for the binary representation. The IV characteristics for the PIN microheater are shown in Sec. 5 of the supplementary material (Fig. 5 of the supplementary material). The applied amorphization pulse produces a very high temperature, which further activates the doped silicon. We observed that the condition became stable after around the first ten pulses. It is also noted that the device damage happened much more often during crystallization than amorphization due to the long pulse duration and low heater resistance. Even a slight increase in the voltage can lead to a significant increase in temperature, which can melt the silicon waveguides (see Sec. 6 of the supplementary material for SEM on damaged devices).

We show the endurance test result of the low-voltage, low-energy device in Fig. 3(b), demonstrating 2000 switching events (1000 switching cycles) with a pulsing rate of 10 Hz. We performed the endurance test in Fig. 3(b) by alternatively switching the device between the crystalline and amorphous state of the PCM. The laser was parked at ~1546.25 nm, which is in resonance with the micro-ring cavity for amorphous Sb_2S_3. We observed no performance degradation at the end of 2000 switching events, and the experiment was stopped only because of the long duration of the experiment. We noticed a sinusoidal modulating pattern, which can be attributed to the self-heating effect of the micro-ring resonator. To verify that this modulation is not related to PCM modulation, we repeated the cyclability test at a lower pulsing rate of 1 Hz (see Sec. 7 of the supplementary material). The frequency of the modulation remains the same (note the x-axis is in a different time scale), indicating this modulation is not related to the electrical pulses nor the PCMs.

Here, we provide a more detailed explanation of the constant oscillation. In a doped silicon micro-ring resonator, light is absorbed due to free-carrier absorption or two photon absorption, producing extra heat. Such a self-heating effect changes the effective refractive index of the ring by the thermo-optic effect, causing a shift in the ring resonance.[80,81] During the cyclability test, we initially parked the laser on resonance, leading to a strong light field in the ring. Due to the self-heating effect, the resonance is gradually shifted until the laser becomes completely off-resonant when the light inside the resonator becomes too weak to heat up the cavity. The resonator then gradually cools itself down to room temperature, causing the laser to be on-resonance again and repeating the previous process. Such cyclic phenomenon results in the sinusoidal pattern shown in the endurance test in Fig. 3(b). We note that this undesired effect can be weakened by reducing the laser power or by setting the laser slightly off-resonance. In our later measurements (Fig. S10), such an effect was eliminated by employing both practices.

C. 7-bit multi-level hybrid TO/PCM tuning

The inherent stochasticity of PCM switching limits the achievable number of levels, which can be compensated for by adding thermo-optic fine tuning on top of the PCM coarse tuning. In this configuration, the PIN diode heaters are used for both volatile and non-volatile tuning. With this hybrid tuning approach, we demonstrate a 7-bit multilevel operation (up to 127 levels). We started

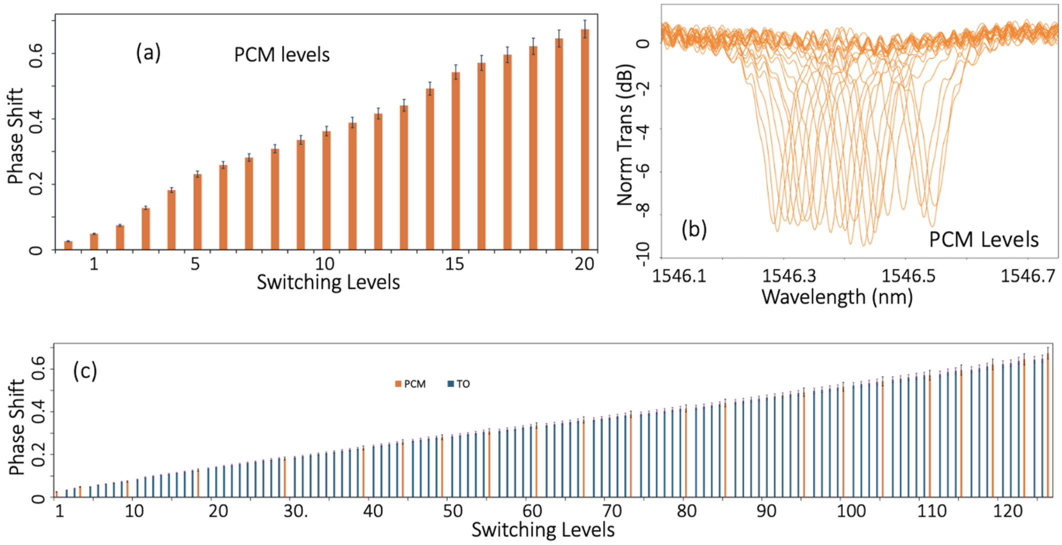

FIG. 4. Seven-bit tuning of micro-ring resonators using hybrid thermo-optic/PCM tuning. (a) Measured phase shifts by multilevel tuning of PCM Sb_2S_3 over 22 switching levels by applying a partial amorphization pulse with voltages ranging from 2.45 to 2.65 V, providing a resonance shift of $\Delta\lambda = 0.01$ nm in each step. The partial amorphization pulse changes the Sb_2S_3 optical phase in a coarse but nonvolatile fashion to achieve a phase shift of 0.02π in level 1 and going up to 0.2π at level 22. (b) The individual transmission spectra due to PCM tuning in the wavelength range of 1546.25–1546.5 nm. (c) Measured phase shifts by multilevel tuning of PCM Sb_2S_3 combined with the TO effect to obtain 127 switching levels, thus demonstrating a 7-bit multilevel operation. The PCM tuning is achieved by applying a partial amorphization pulse with voltages ranging from 2.45 to 2.65 V. In between two PCM tuned levels, precise thermal tuning (5–6 TO levels on average) is achieved using the same PIN diode heater by gradually increasing the DC voltage from 0.85 to 1.5 V. The orange and blue bars represent the phase shifts obtained due to PCM tuning and TO tuning, respectively. Norm. Trans. stands for normalized transmission, which is calculated as Transmission (dB) = 10 $\times \log_{10}$ (transmitted power in mW), and the maximum transmission is normalized to 0 dB.

the experiment by applying a 500 ns pulse at 2.45 V to partially amorphize the c-Sb_2S_3 device to demonstrate multiple levels. After one partial amorphization pulse, the resonant wavelength shifts to the left by 0.01 nm (i.e., $\Delta\lambda = 0.01$ nm), thus corresponding to an intermediate PCM level. The resonance shifts due to PCM tuning enlarge as we increase the amorphization voltage from 2.45 to 2.65 V, providing a resonance shift of $\Delta\lambda = 0.01$ nm in each step and 22 operation levels. The partial amorphization pulse changes the Sb_2S_3 optical phase in a coarse but nonvolatile fashion. Furthermore, we show 350 cycles in total for seven intermediate amorphization levels with only minimal variation in Fig. S10 of the supplementary material. To provide precise thermal tuning, we then applied DC voltage on the same PIN diode heater starting from 0.85 V up to 1.5 V. The resonance wavelength shifts to the left at the beginning because the free-carrier dispersion effect dominates the thermo-optic effect. When the applied voltage is larger than 1 V, red shifts appear. This shift in $\Delta\lambda$ is volatile, and the resonance shifts back upon removal of the DC voltage. Figure 4(c) shows 127 switching levels, with error bars indicating the range from the thermo-optic tuning and PCM tuning over two cycles. The thermo-optic levels were recorded by five repeated experiments in each cycle to ensure that the resonance shift was from the thermo-optic tuning and not from the PCM tuning. Figure 4(a) shows the phase shift for different switching levels via PCM tuning. The individual transmission spectra corresponding to each resonant wavelength shift due to PCM tuning for the first cycle are presented in Fig. 4(b). Another repeatable transmission spectrum tuned by PCM is demonstrated in Fig. S9 of the supplementary material. In between two PCM tuned levels, ~5 thermo-optic levels are recorded on average by gradually increasing the DC voltage in the range of 0.85–1.5 V. The phase shift ($\Delta\phi$) is calculated as

$$\Delta\phi = (\Delta\lambda/FSR)\cdot 2\pi, \tag{1}$$

where $\Delta\lambda$ corresponds to the resonant wavelength shift for a free spectral range (FSR) of 2.42 nm. The transmission spectra corresponding to the combined effect of thermo-optic and PCM tuning are shown in Sec. 8 of the supplementary material (Fig. 8 of the supplementary material). It is important to note that the thermo-optic levels show a much higher loss corresponding to the PCM levels, mainly due to the free carrier effect. Furthermore, we would like to note that in the process of doing additional multilevel endurance experiments on the same device, we were able to switch the PCM for >10 K events combining partial and complete amorphization and crystallization cycles.

III. DISCUSSION

In the future, the switching voltage and energy can be further reduced by suspending the PIN micro-heater, which prevents the generated heat from dissipating to the buried oxide and silicon substrate. This technique was used in thermo-optic phase shifters, exhibiting a great efficiency power reduction of >98%. Recently, this has been proposed for PCM switching in a partially suspended silicon micro-ring resonator.,[82] but no experimental demonstration has yet been reported. We note that one of the main challenges of this approach is engineering the structural stability to avoid deformation or thermal damage during the fabrication and operation. Furthermore, using multiple PCM islands instead of one single PCM patch might further improve the endurance of phase-change devices and enhance the granularity of the phase transitions, allowing for more intermediate levels. Each island will confine the phase transition to a smaller region, thus reducing the cumulative thermal and mechanical stress during switching. This localized switching can minimize the risk of material fatigue, defect accumulation, and degradation of the PCM or surrounding layers, which are common causes of failure in continuous PCM segments.[64,77,83] This approach may allow individual islands to be selectively switched, enabling partial operation and reducing the total number of switching events each island experiences, thereby prolonging the overall device lifetime. However, it may require more careful design and complex fabrication processes to ensure uniform switching behavior across all PCM islands. To achieve more operation levels, we can engineer the pulse shape to allow more precise control of the PCMs, such as multi-pulse techniques or pulse width modulation.[51] Furthermore, increasing the capping layer thickness or employing other more inert capping materials such as silicon nitride can also increase the endurance of PCM.[84]

It is important to note that the main novelty of this work lies in the demonstration of 127-level, low-energy hybrid tuning of micro-ring resonators, marrying nonvolatile PCMs for coarse but energy efficient tuning and the thermo-optic effect for precise tuning. It is well-known that PCM tuning is not deterministic for intermediate levels due to cycle-to-cycle structural differences. Bringing the deterministic thermo-optic tuning to fine-tune the response can overcome this long-standing limitation. On the other hand, compared to the pure thermo-optic approach, such a hybrid approach has a much lower static power—the device is first brought closer to the desired operation point and then applied with only slight voltage for thermal fine tuning. This will easily provide orders of magnitude lower average static power, depending on the levels achievable with PCMs and the system's static time. We also note that since the applied electric current for thermo-optic tuning is only tiny, the loss from the free-carrier dispersion effect as well as the thermal crosstalk is significantly reduced. As another important achievement, we achieved operation voltage compatible with CMOS driving voltages (<3 V) by optimizing microheater geometry, allowing for integration with CMOS EICs using various integration techniques. This is a crucial step for the further scale up of PCM-based programmable PICs for applications in data centers and AI.

In summary, we have demonstrated low-voltage and low-energy switching of PCMs by carefully engineering the PIN doped silicon microheaters. We numerically and experimentally studied the heating performance of PIN diode heaters and observed a monotonically increasing switching voltage with the increase in intrinsic region width. With a small intrinsic region of 0.9 μm, we demonstrate a CMOS-compatible switching voltage of 2.75 V (1.6 V) and an energy of 35.33 nJ (0.48 mJ) for amorphization (crystallization) of a 10-μm-long Sb_2S_3 on silicon waveguides. We further showed the 127-level operation of PCM-clad Si micro-ring resonators and over 10 thousand cycles in total by combining PCM coarse tuning with thermo-optic fine tuning. We emphasize that arbitrary intermediate levels can be repeatedly achieved by using the thermo-optic fine tuning to compensate for the randomness of PCM tuning, providing a much more accurate and finer quasi-continuous tuning method. Our work on low-voltage, low-energy, hybrid tuning of PCM photonic devices bridges the gap of CMOS compatible PCM switching, paving the way for scalable, co-packaged PCM-based electro-optical systems that meet the demands of AI, data centers, and neuromorphic computing.

IV. METHODS

A. SOI device fabrication

The fabrication of silicon photonic devices was conducted on a commercial SOI wafer featuring a 220 nm thick silicon layer atop a 2 μm thick SiO_2 layer (WaferPro). Electron beam lithography (EBL, JEOL JBX-6300FS) was used to write the device patterns using a positive-tone EBL resist (ZEP-520A), followed by partial etching to a depth of ~120 nm using a fluorine-based inductively coupled plasma etcher (ICP, Oxford PlasmaLab 100 ICP-18) with a mix of SF6 and C4F8 gases, achieving an etch rate of ~2.8 nm/s. The doping regions were formed through two additional EBL processes with PMMA, and removal of the surface native oxide layer was performed by immersing the chips in a 10:1 buffered oxide etchant (BOE) for 10 s, after which metal contacts were patterned through a fourth EBL step with PMMA. The metal deposition was achieved via electron-beam evaporation (CHA SEC-600) and subsequent lift-off of Ti/Pt (5 nm/180 nm). Measurements of PIN diodes with the variation in intrinsic region from 0.9 to 1.9 μm indicated a threshold voltage of ~0.8 V and a resistivity around 50 Ω. After a fifth EBL step to define the Sb_2S_3 window, a 40 nm Sb_2S_3 thin film was deposited from a Sb_2S_3 target (Plasmaterials) using a magnetron sputtering system (Lesker Lab 18), followed by a lift-off process. The Sb_2S_3 layer was then encapsulated with a 40 nm thick Al_2O_3 coating using thermal ALD (Oxford Plasmalab 80PLUS OpAL ALD) at 150 °C. The detailed fabrication process can be referred to from the cited paper.[51]

B. Heat transfer simulation

The power requirement for reversible switching of the doped silicon PIN heater was simulated using COMSOL Multiphysics, a commercial simulation software.[51,58,85] This simulation integrated a heat transfer model in solids with a semiconductor model to evaluate the transient response of the device.

C. Optical transmission measurement setup

The optical measurement setup consists of a vertical fiber-coupling setup angled at 25°, a thermoelectric controller (TEC, TE Technology TC-720), a tunable continuous-wave laser (Santec TSL-510), a manual fiber polarization controller (Thorlabs FPC526), and a low-noise power meter (Keysight 81634B) to measure the static optical transmission. TEC was used to maintain the stage temperature at 26 °C. Input light was provided by Santec TSL-510 with its polarization optimized by the polarization controller to achieve maximum fiber-to-chip coupling efficiency. For on-chip electrical switching, electrical pulses were applied to the on-chip metal contacts via a pair of electrical probes positioned with probe positioners (Cascade Microtech DPP105-M-AI-S). Crystallization and amorphization pulses were generated using a pulse function arbitrary generator (Keysight 81160A). The tunable laser, power meter, thermal controller, source meter, and pulse function arbitrary generator were all controlled through a LabView program.[58] The detailed optical measurement setup can be referred to from this cited paper.[51]

SUPPLEMENTARY MATERIAL

The supplementary material includes the measured optical and electrical characterization corresponding to varying PIN microheater geometry. The supplementary material further includes the heat transfer simulation performed in COMSOL Multiphysics software corresponding to the amorphization and crystallization of PCM for varying PIN heater geometry.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Jayita Dutta: Conceptualization (lead); Data curation (lead); Formal analysis (lead); Methodology (lead); Software (lead); Visualization (lead); Writing – original draft (lead); Writing – review & editing (lead). **Rui Chen**: Conceptualization (equal); Investigation (equal); Resources (equal); Supervision (equal); Validation (equal); Writing – review & editing (equal). **Virat Tara**: Methodology (supporting); Resources (supporting); Writing – review & editing (supporting). **Arka Majumdar**: Conceptualization (equal); Investigation (lead); Project administration (lead); Resources (equal); Supervision (lead); Validation (lead); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon request.

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