A Multi-Phase Injection-Locked 8-Phase 17 GHz Clock Generator with 6b Phase Rotation for Multi-Phase Wireline Receivers

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***Abstract*—A high frequency multi-phase clock generator circuit with a 6b phase rotator is presented for multi-phase wireline receivers. Multi-phase injection is used to efficiently generate and rotate 8 clock phases. Unlike prior rotator-based work, this work does not use time modulation, reducing the resulting deterministic jitter. A model is presented to study the nonlinearity introduced by the technique. The proposed 17 GHz circuit was implemented in the Intel 16 process and consumes 33 mW. The measured RMS jitter is 98 fs, and the measured DNLpp and INLpp are 1.26 and 4.05 LSB respectively.**

***Index Terms*—phase rotator, multi-phase clock generation, injection locked ring oscillator, multi-phase injection, phase interpolator**

I. Introduction

Next-generation hyperscale computers rely on interconnected systems that require significant boosts in datacenter network bandwidth. This is driving a demand for faster high-speed wireline systems. Multi-phase sampling has become the dominant technique for achieving high throughput in wireline receivers by maintaining the per-lane data rate and interleaving multiple lanes. Recently published receivers have used 8 or more clock phases. These multi-phase receivers are highly sensitive to clock jitter as they are used with high-loss channels where the receiver eye is significantly degraded. Sampling phase alignment must be performed on all the generated phases and must have high resolution to compensate for the degraded eye. These collective challenges make clock generation an increasingly large part of the wireline power budget.

Typically, receiver sampling phase alignment is accomplished by using a multi-phase clock generation (MPCG) circuit, such as an injection-locked ring oscillator (ILRO) or a phase-locked loop (PLL), followed by a phase interpolator (PI) to rotate the clock phase. Each additional sampling phase necessitates an additional PI, adding to the power and area cost. To avoid this cost, phase rotation must be performed on the reference side of the MPCG instead of the output side. This efficiently rotates all the generated phases at once.

In ILRO-based MPCGs, multi-phase injection (MPI) can be used to accomplish this. Prior MPI implementations cascade multiple MPCGs and inject all generated phases from one stage into the next, improving MPCG phase alignment and jitter filtering [1]. In this work, MPI is used to inject a single reference phase into multiple oscillator phases at once.

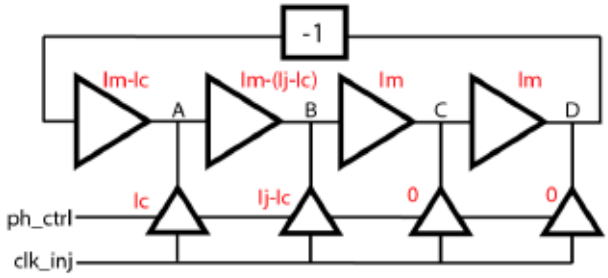

Fig. 1. Multi-phase injection-locked phase rotator concept. The core and injection drivers are labeled with their drive strength. Injection can be enabled for any adjacent pair of nodes. In this configuration, the injection phase will lock between nodes A and B.

II. Proposed Architecture

Fig. 1 shows the proposed concept. The core circuit is a ring oscillator with injectors in each stage. MPI is used to inject into two adjacent stages simultaneously, e.g. nodes A and B. When the injection strength *Ic* is at its maximum value *Ij*, injection will be phase-locked to node A. As *Ic* decreases, the phase lock will progressively shift from node A to node B. This culminates in phase-locking to node B when *Ic* reaches 0. The same procedure can then be repeated with nodes B and C and so forth to achieve full rotation. Rotating the lock phase will rotate all the ring oscillator's output phases together.

Prior work in this area has not fully explored the possible resolution [2] or has focused on time-modulated solutions [3] [4], which introduce undesired deterministic jitter. A high-resolution static, i.e., not time-modulated, solution has not been explored. In this work, the core oscillator has 8 phases, and the injection strength between two stages is varied in 8 steps, resulting in 64 total steps or 6-bit resolution.

A. Modeling

To study the static rotator phase integral non-linearity (INL) introduced by this MPI scheme, a model is presented in Fig. 2. Each injection stage is treated as a phase interpolator between the oscillator clock and the injection clock, while the non-injection stages are treated as typical delay stages. The free running oscillator frequency is assumed to be the same as the injection frequency. Under injection lock, the total period contributed by all stages should equal the injection clock

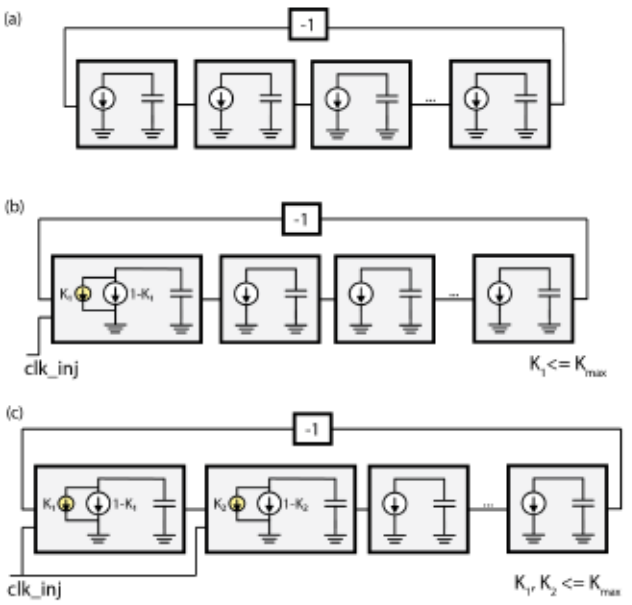

Fig. 2. (a) General oscillator model. Each stage contributes one stage delay (b) Single-phase injection model. (c) Multi-phase injection model.

period. When injecting solely into one stage (Fig. 2b), i.e., no MPI, the injection stage should contribute the same delay as any other non-injection stage, resulting in no static phase error. When injecting into two adjacent stages (Fig. 2c), the pair together should still contribute the same delay as two non-injection stages. Thus, under injection lock, the injection phase relative to the oscillator can be found by solving for the injection phase that yields the correct stage delay.

The resulting static phase INL from this model is shown in Fig. 3 for a 6b case. The worst-case phase error is improved by reducing the maximum injection ratio, K_{max}. However, reducing K_{max} also shrinks the phase noise filtering bandwidth, increasing jitter [7]. Thus, there is a trade-off between jitter and resolution. Our target power and jitter specification are met with less than 7 bits of expected resolution.

III. Circuit Implementation

The implemented circuit is presented in Fig. 4. At the core is a 4-stage differential CML-based ILRO. Each delay stage contains 5 NMOS differential pairs, as shown in Fig. 5. The primary pair (I1) is driven by the oscillator's internal signal and is always on. One pair (I2) is driven by the differential injection signal, and another (I4) is driven by the injection signal with a flipped polarity. Each of these injection pairs is complemented with another pair connected to the oscillator's internal signal (I3 & I5). When a given injector (e.g. I2) is turned off, the completed (I3) is turned on, allowing each stage to maintain the same current regardless of rotator code.

The injection ratio is set by the current ratio between the pairs driven by injection and the pairs driven by the oscillator's

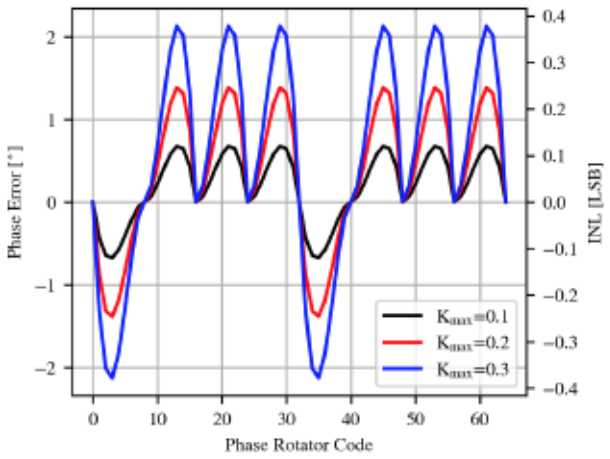

Fig. 3. Modeled phase error or INL for varying values of K_{max}. INL LSB is for a 6b case.

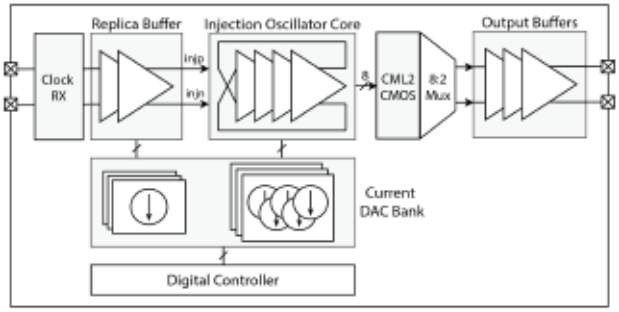

Fig. 4. Implemented phase rotator system architecture.

signal up to a maximum injection ratio K_{max}. Digitally-controlled current DACs are used to individually control the current for each NMOS pair based on the rotator code. In this design, each current DAC has 8 steps of injection control. To perform MPI, the injection into one stage linearly decreases while the injection in the next stage linearly increases.

Before the oscillator core, replica buffers and replica bias are used to condition the input reference signal. Following the oscillator core are CML2CMOS buffers. For testing, an 8:2 clock mux is included after the CML2CMOS buffers, followed by auxiliary output buffers . A digital controller is included to set the current DAC bits. Simulation results are shown in Fig. 6 for the complete system excluding the 8:2 mux and output buffers. Deviation from the model is attributed to layout assymmetries.

IV. Measurements

The proposed design was fabricated in the Intel 16 process [8], targeting a clock frequency of 17 GHz. The analog core area is 55 µm x 30 µm, and the digital core is 55 µm x 20 µm. For comparison, accomplishing the same functionality by using CMOS phase interpolators requires an analog core area of 53 µm x 60 µm. This proposed architecture presents

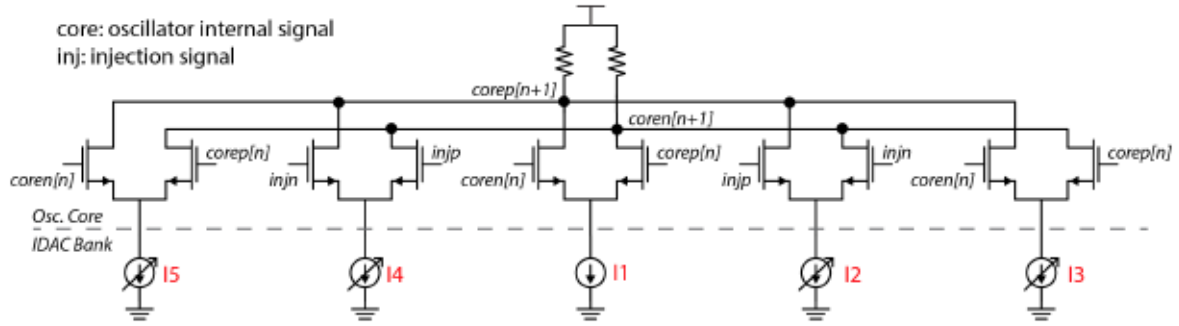

Fig. 5. Oscillator Stage.

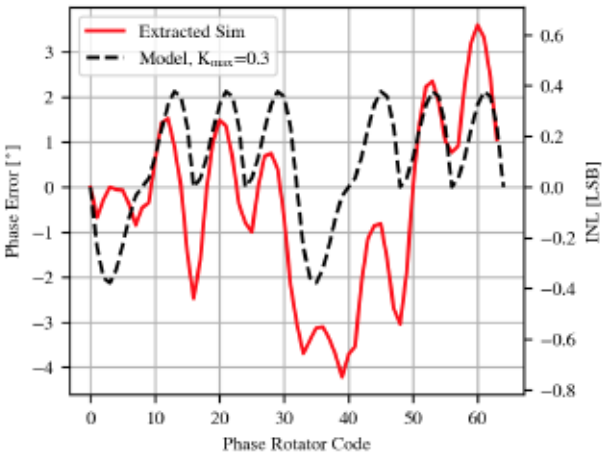

Fig. 6. INL comparison between model and extracted circuit simulation.

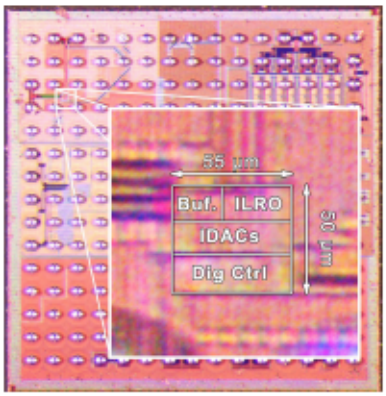

Fig. 7. Die micrograph.

a 50% analog area reduction. The measured analog power consumption, including the oscillator core, rotator, and input and output buffers, is 33 mW at 1.2V supply.

Fig. 8 shows the MPCG performance. At a fixed rotator code, the 8-phase error is measured to be under 17 degrees peak-to-peak across all phases. The phase noise at 1 MHz

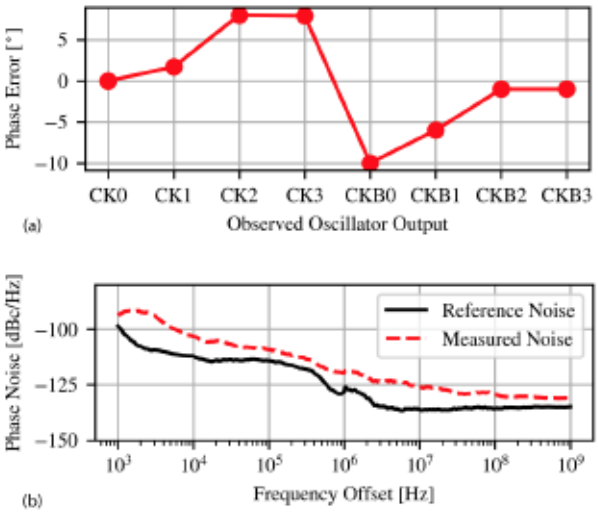

Fig. 8. (a) Measured MPCG error and (b) phase noise spectrum.

offset frequency is -119.6 dBc/Hz. The measured integrated RMS jitter from 10KHz to 1GHz is 98 fs. Jitter is not significantly impacted by rotator code and varies by less than 3 fs. This is expected since the current into each stage is constant across all codes.

INL was measured for each of the 8 output phases. The best and worst curves are shown in Fig. 9. Generally, the INL curve contains the expected systematic behavior from modeling. However, the size of the error peaks exceeds expectations by approximately a factor of 2, with additional deviations coming from MPCG error. Fig. 10 summarizes the DNLpp and INLpp for all outputs. For this 6b design, the worst static DNLpp and INLpp are 1.26 LSB and 4.05 LSB respectively. Dynamic performance was measured by observing the output spectrum while incrementing the rotator phase code. The code incrementation was controlled by the digital controller and clocked up to 48 MHz. The largest spur varies between -27.4 and -28.8 dBc at +/- 0.75 MHz offset, depending on the selected output phase. This correlates with the FFT of the INL. The integrated fractional spur is -24.0 dBc.

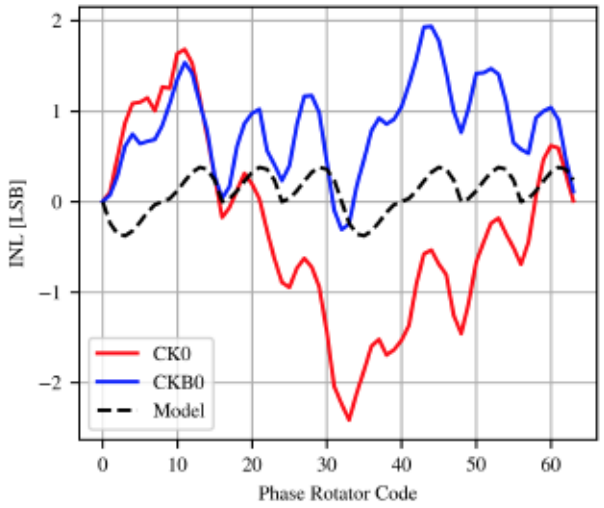

Fig. 9. Measured best (CKB0) and worst (CK0) INL curves.

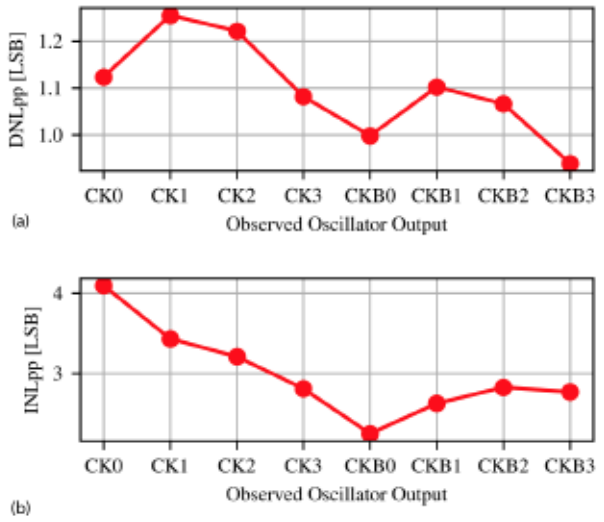

Fig. 10. (a) Measured DNLpp and (b) INLpp for all clock outputs.

Table I compares the performance of the proposed circuit with other multi-phase clock generators. Ref. [2] [3] and [5] demonstrate similar phase rotator-based techniques, while [1] and [6] demonstrate PI-based techniques. Compared to prior phase rotator-based work, this work demonstrates the best jitter (PLL) FOM and multi-phase generation efficiency (MPCG FOM) while demonstrating high resolution rotation. Compared to the PI-based work, this work presents comparable jitter performance and phase resolution. By performing simultaneous rotation, it achieves better MPCG multi-phase generation efficiency.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Metrics	This Work	PR-based			PI-based	
		[2]	[3]	[5]	[1]	[6]
Architecture	MPI-ILO-PR	MPI-ILO-PR	MPI-ILO-PR	MPI-ILO-PR	MPI-ILO + PI	QLL + PI
Process	16	65	45	16	65	7
Freq [GHz]	17	3.7	4.05	7	7	16
Number of Phases	8	2	8	8	2	2
Integrated Jitter [fs RMS]	88	1400	1700	254	84	80
Number of Bits	6	7	7	8	7	7
Resolution [ps]	0.92	2.11	1.93	0.56	1.12	0.49
INL [LSB]	2.4	-[a]	1.20	0.59[b]	1.15[b]	1.44[b]
INLpp [LSB]	4.05	-[a]	2.20[b]	1.14	1.72	1.74
DNL [LSB]	0.7	0.71	0.40	0.75[b]	0.76[b]	1.27[b]
DNLpp [LSB]	1.26	0.90[b]	0.70[b]	1.31	1.13	0.87
Supply [V]	1.2	1	1	1.2	1.2	1.2
Power [mW]	33.6	4.4	14.3	11.4	22.95[c]	22.4
PLL FOM	-244.9	-230.6	-223.8	-241.3	-247.9	-248.4
MPCG FOM	-266.2	-239.3	-238.9	-258.8	-259.4	-263.5

[a]Not reported. [b]Estimated from charts. [c]Includes MPCG and PI.

$$\text{FOM}_{\text{PLL}} = 10\log_{10}\left((\text{Jitter}_{\text{RMS}})^2\left(\frac{\text{Power}}{1\text{mW}}\right)\right)$$

$$\text{FOM}_{\text{MPCG}} = 10\log_{10}\left((\text{Jitter}_{\text{RMS}})^2\left(\frac{\text{Power}}{1\text{mW}}\frac{1\text{GHz}}{\text{Frequency}}\frac{1}{\text{Num. Phases}}\right)\right)$$

V. CONCLUSIONS

This paper presented a technique for efficient multi-phase clock generation and rotation. Multi-phase injection was used to perform high-resolution rotation, and a model was presented to determine the introduced nonlinearity. This phase rotator technique achieves better MCPG efficiency than PI-based techniques at comparable frequencies. By using a static injection method, the proposed technique also significantly improves jitter over prior phase rotators. The circuits in this work were generated using BAG3++, and the generator code is released under open-source licenses [9].

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