A 23–28-GHz Doherty Power Amplifier With a PVT Insensitive Power Detection for Adaptive Biasing

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***Abstract*—This letter presents a compact Doherty power amplifier (PA) featuring a single transformer balun. A novel envelope power detector architecture is introduced for high-bandwidth (BW) adaptive biasing, that is, insensitive to process–voltage–temperature (PVT) variations. The measured PA attains a saturated power (P_{sat}) exceeding 20.2 dBm and a power gain of 19.5 dB across the frequency range of 23–28 GHz. Moreover, it exhibits a peak power added efficiency (PAE) of 38% and a 6-dB power back-off (PBO) PAE of 27% at 25 GHz. The proposed adaptive biasing scheme enables a modulation BW of up to 800 MHz for a 64-QAM signal. Under this setting, the average output power (P_{avg}) is measured at 11.3 dBm with an RMS error vector magnitude (EVM) of −24.5 dB and an average PAE of 15.5%. The PA is fabricated in Global Foundries 45-nm-SOI technology with a compact area of 0.27 mm^2. To the best of the authors' knowledge, this work is the first to demonstrate robust performance for Doherty PAs across PVT variations.**

***Index Terms*—CMOS, Doherty, envelope detector, error vector magnitude (EVM), high efficiency, power amplifiers (PAs), power back-off (PBO), process–voltage–temperature (PVT).**

I. Introduction

Modern communication systems demand high-order modulation schemes to achieve high-data rates. These schemes, with high-peak-to-average power ratios (PAPRs), require power amplifiers (PAs) with high linearity to minimize out-of-band emissions and meet error vector magnitude (EVM) requirements through reducing both the amplitude and phase nonlinearity [1]. However, the elevated PAPR forces PAs to operate at reduced average power levels, significantly lowering average power-added efficiency (PAE).

Doherty PAs [2] have been thoroughly investigated in literature to improve PBO efficiency. The functionality of the Doherty PA relies on the presence of two amplifiers, namely, the main and auxiliary amplifiers. The proper coordination between the main and auxiliary amplifiers, with input power, is crucial for the PAE and EVM performance of the Doherty PA. This power-dependent operation necessitates adaptive bias circuits, enabling fast activation of the auxiliary amplifier as power surpasses the requisite threshold. Consequently, a practical issue arises for Doherty PAs which lies in the substantial variation of output voltage in these adaptive bias circuits with PVT, thereby degrading the Doherty PA's performance.

This work presents a Doherty PA design with a robust performance across PVT variations through introducing a novel power detector architecture for PVT insensitive adaptive biasing. This detector employs a feedback mechanism, ensuring a detector gain dependent on the ratio between resistor values while maintaining the required BW for 5G NR signals. Additionally, The proposed Doherty PA has a compact area by utilizing a differential CLC impedance inversion network based on the lumped model of the transmission line, coupled with the use of a single transformer [3].

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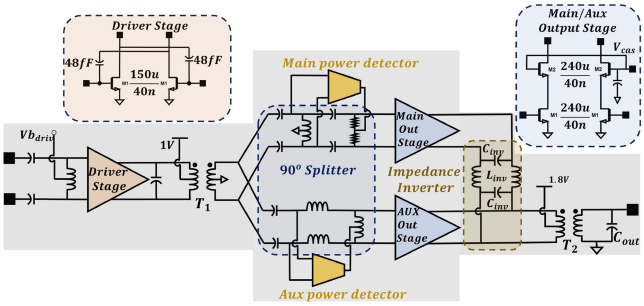


Fig. 1. Top schematic for the Doherty PA.

II. Circuit Design

A. Doherty PA Implementation

Fig. 1 illustrates the schematic view of the proposed PA, featuring a Doherty output stage with a single driver amplifier. To ensure a compact footprint, meticulous design of the output network is essential. A single transformer balun T2 is used to match the output load to the PA R_{opt}, which is the load needed to achieve the best compromise between output power and PAE. The amplitude and phase imbalances of the balun are targeted below 0.25 dB and 5°, respectively, to ensure precise combining of the differential signals. A lumped CLC network is used as the impedance inverter to provide $2R_{opt}$ at low power for the main amplifier and R_{opt} for both main/aux amplifiers at high power, this provide the load modulation needed in the Doherty PA to increase the PAE at 6-dB PBO [2]. The L and C values are determined through the equations outlined in [4]. The transistor drain parasitic capacitance can be absorbed into the CLC network attaining high-BW across frequency.

The implementation of the main and auxiliary output stages involves designing a common-source amplifier with cascode transistors, utilizing a 1.8-V supply for the output stage while using transistor dimensions of $W/L = 240\ \mu$m/40 nm to support the required high-output power. A lumped LC 90° input splitter is used to compensate for phase differences between the main and auxiliary stages. To enhance the compactness of the PA, a single class AB driver is employed using a 1-V supply. The driver is implemented using a common source stage, $W/L = 150\ \mu$m/40 nm, with capacitive neutralization to attain maximum gain while ensuring a stable performance.

B. Proposed Power Detector for Adaptive Biasing

Fig. 2(a) illustrates the schematic of the conventional power detector. In this configuration, *vinp* and *vinn* denote the differential inputs of the PA, where $V_{inp} = A\cos(\omega t)$ and $V_{inn} = -A\cos(\omega t)$. These inputs are sensed through a sensing capacitor C_{sen}, while V_{cm} represents the common mode voltage for the detector transistors and W signifies the width. The DC output voltage of the detector, used for biasing the PA transistors, is determined by the following equation:

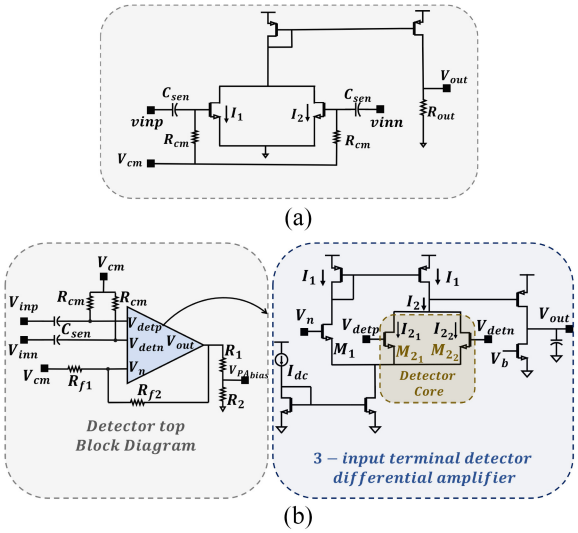


Fig. 2. Conventional and proposed power detectors. (a) Conventional power detector for adaptive biasing. (b) Proposed power detector for adaptive biasing.

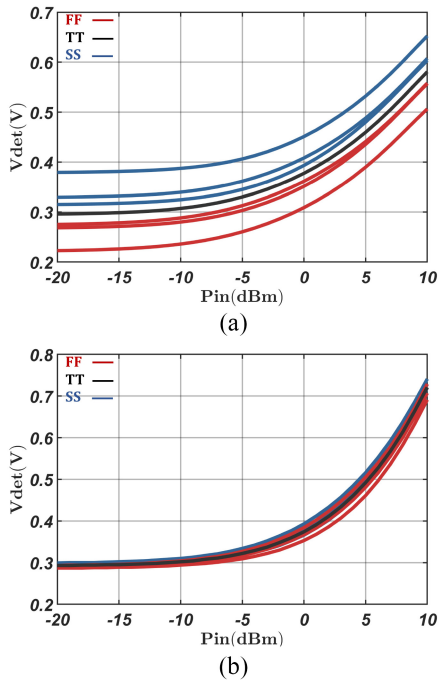


Fig. 3. Conventional and proposed detector output voltages across PVT. (a) Conventional detector output voltage across PVT. (b) Proposed detector output voltage across PVT.

$$V_{\text{out}} = \frac{\mu_n C_{ox} W}{L} \times \left((V_{cm} - V_{\text{th}})^2 + \frac{A^2}{2} \right) \times R_{\text{out}}. \tag{1}$$

This equation is dependent on the process parameters, resulting in significant variation across PVT, as shown in Fig. 3(a).

To address this challenge, a new architecture, depicted in Fig. 2, is proposed. This design relies on the concept of operational amplifiers (op-amp) in closed-loops, which exhibit reduced PVT variations. Similar to the conventional detector, *vinp* and *vinn* represent the PA differential inputs which are sensed using C_{sen}. Instead of employing an op-amp with two differential terminals, a three-terminal detector amplifier is utilized. Transistor M_2 is split into two transistors, M_{2_1} and M_{2_2}, each with a width of $W/2$, and both transistors constitute

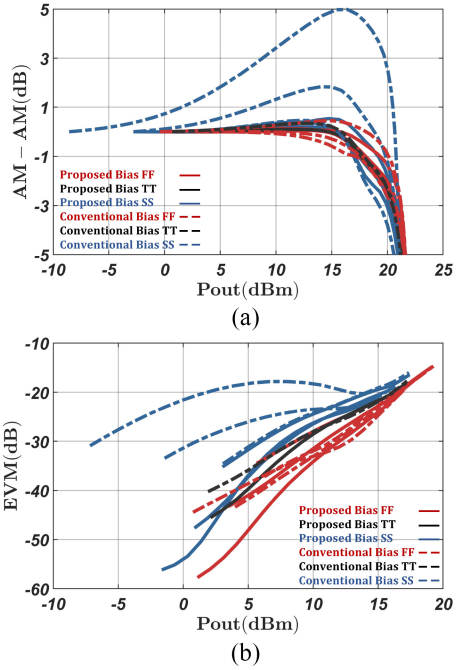


Fig. 4. Simulated AM-AM and EVM of the Doherty PA using conventional and proposed adaptive biasing across process and temperature corners. (a) Simulated AM-AM for both adaptive bias methods. (b) Simulated EVM for both adaptive bias methods.

the power detection core. In essence, the power detector is embedded into the op-amp. The gate voltages of these transistors are connected to the sensed nodes from the PA input while having V_{cm} as the common mode voltage. This leads to current I_2 of

$$I_2 = \frac{\mu_n C_{ox} W}{2L} \times \left((V_{gs_{cm}} - V_{th})^2 + \frac{A^2}{2} \right). \tag{2}$$

The third terminal V_n will be incorporated into a negative feedback configuration, utilizing two feedback resistors R_{f1} and R_{f2}. Transistor M1 maintains a width of W and common mode voltage (V_{cm}), similar to M_{2_1} and M_{2_2}. The output voltage from this negative feedback configuration will be connected to a voltage divider of R_1 and R_2 which will adjust the common mode voltage to be suitable for the class AB bias in case of the main PA and class C bias in case of the aux PA. The negative feedback will force the currents I_1 and I_2 to be nearly the same due to the high gain. I_1 is given by

$$I_1 = \frac{\mu_n C_{ox} W}{2L} \times \left((V_{gs_{cm}} - V_{th})^2 + 2(V_{gs_{cm}} - V_{th}) V_{n_{ac}} + V_{n_{ac}}^2 \right) \tag{3}$$

where $V_{n_{ac}}$ can be defined as the AC voltage above the common mode level V_{cm} for the node V_n. Solving (2) and (3) together leads to $V_{n_{ac}}$ of

$$V_{n_{ac}} = \sqrt{(V_{gs_{cm}} - V_{th})^2 + \frac{A^2}{2}} - (V_{gs_{cm}} - V_{th}). \tag{4}$$

The output voltage of the detector $V_{PA_{\text{bias}}}$ can therefore be calculated as

$$V_{PA_{\text{bias}}} = \left(V_{cm} + V_{n_{ac}} \times \left(1 + \frac{R_{f1}}{R_{f2}} \right) \right) \left(\frac{R_2}{R_1 + R_2} \right). \tag{5}$$

The above equations illustrate that the output voltage of this detector remains nearly unaffected by PVT variations, as depicted in Fig. 3(b), where a V_{cm} of 0.3 V is used.

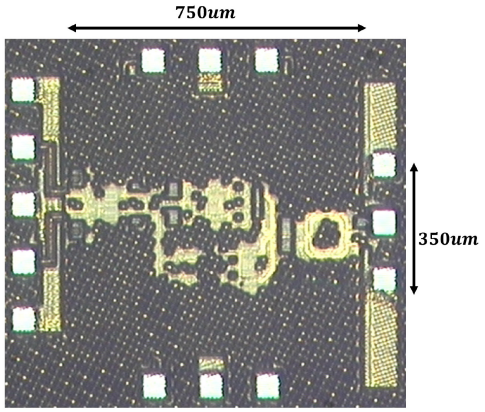


Fig. 5. Chip micrograph for the Doherty PA.

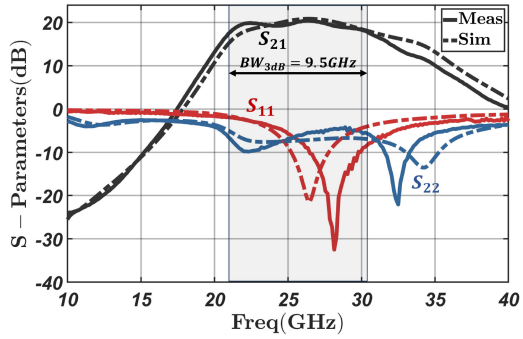


Fig. 6. Measured *S*-parameters for the Doherty PA.

To assess the performance improvement of the Doherty PA with the proposed adaptive biasing compared to the conventional method, simulations of AM-AM (variation in power gain relative to low-power gain) and EVM (64-QAM 100-MHz modulated signal) across process and temperature corners are conducted. For both adaptive biasing methods, the V_{cm} is linked to a current mirror, enabling a common mode voltage that tracks the PVT variations of the PA. The simulation results, depicted in Fig. 4, indicate significant enhancement across process and temperature corners with the proposed adaptive biasing scheme.

The power detector is capable of supporting high-channel bandwidths of up to 800 MHz. The bandwidth limitations are contingent on the closed-loop bandwidth of the detector amplifier, which is approximately 2 GHz in this design.

III. Measurement Results

A prototype amplifier has been designed and fabricated in Global Foundries 45-nm SOI process. The chip micrograph is shown in Fig. 5. The chip has a core area of 350 μm × 750 μm, excluding the pads. Differential GSGSG pads are employed for the input, while single-ended GSG pads are utilized for the output. The DC pads are wire-bonded onto a printed circuit board (PCB) and connected to decoupling capacitors.

The measured *S*-parameters of the proposed PA, shown in Fig. 6, achieves S21 of 20 dB with 3-dB small signal gain BW from 21 to 30.5 GHz. The large-signal continuous wave measurements indicate a Psat of 21.3 dBm, an output 1-dB compression point (OP1dB) of 17.4 dBm, and a peak PAE of 38% at 25 GHz, with the PAE reaching 27% at 6-dB back-off from Psat, as shown in Fig. 7(a). The measured AM-PM of the PA exhibits less than 5.5 ° at the OP1dB of the PA. In addition, Fig. 7(b) illustrates that across the

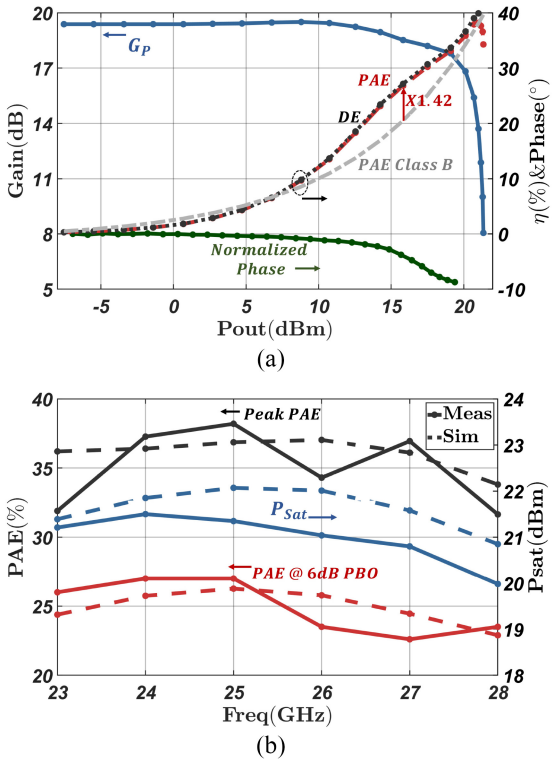


Fig. 7. Measured continuous wave results for the proposed PA across Freq. (a) Measured power gain, AM-PM, PAE, and drain efficiency (DE) across Pout. (b) Measured PAE and P_{sat} for the proposed PA.

frequency range from 23 to 28 GHz, this PA attains more than 20.2-dBm P_{sat}, over 32% peak PAE, and more than 23% PAE at 6-dB PBO. The measured *S*-parameter and continuous wave results exhibit a strong correlation with the simulation results, revealing a maximum deviation of 0.8 dBm in Psat across frequency. This variance could be attributed to the measurement setup, the output probe and cable, which shift the impedance seen by the PA from its nominal 50 ohms.

For modulated signal measurements shown in Fig.8, the PA exhibits an EVM of −26.5 dB for a 100-MHz single carrier (SC) 64-QAM signal, delivering approximately 0.8 Gb/s at an average P_{out} of 12.1 dBm with 17.5% average PAE. It also achieves an EVM of −25 dB for a 100-MHz 64-QAM OFDM signal at an average P_{out} of 11.2 dBm with 13.5% average PAE. Additionally, the PA records an EVM of −24.5 dB for an 800-MHz SC 64-QAM signal, achieving around 6.4 Gb/s at an average P_{out} of 11.3 dBm with 15.3% average PAE, and an EVM of −25 dB for an 800-MHz 64-QAM OFDM signal at an average P_{out} of 10.8 dBm with 12.9% average PAE. Notably, when the modulation bandwidth increases from 100 to 800 MHz, the average P_{out} varies by only 0.8 dBm for SC and 0.5 dBm for OFDM, demonstrating the effectiveness of the adaptive biasing circuit for this bandwidth range.

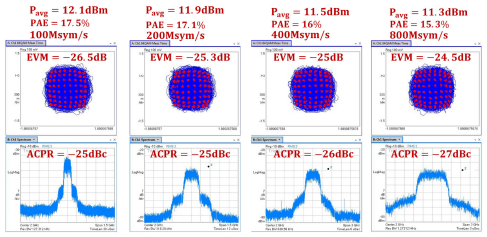
Table I provides a summary of the measurement results for this PA compared to previously published Doherty PAs operating in a similar frequency band. In comparison, the proposed PA achieves an optimal balance between data rate and average PAE within a compact core area.

IV. Conclusion

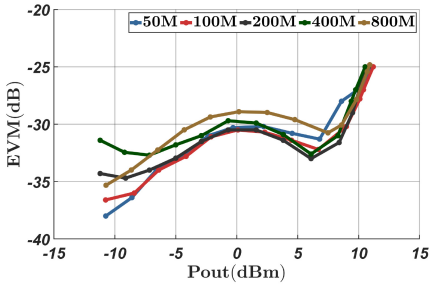
This letter presented a Doherty PA design with a novel adaptive biasing approach characterized by its insensitivity to PVT variations. An accompanying analysis demonstrates the PVT-insensitive response, which is subsequently validated through simulation results.

TABLE I
COMPARISON WITH STATE OF THE ART

Reference	This Work				[3]	[5]	[6]	[7]
Tech	45nm CMOS SOI				28nm CMOS	22nm FD-SOI	40nm CMOS	40nm CMOS
VDD (V)	1.8				1.8	2.4	1	1.8
Freq (GHz)	25				27	28	27	27
Gain (dB)	19.5				16.5	26.1	21.8	17.4
Psat (dBm)	21.3				18.8	22.7	N/A	20.43
OP1dB (dBm)	17.4				17.5	21.1	20	20.2
Peak PAE (%)	38				30	28.5	39.8	39.1
PAE @ 6dB PBO (%)	27				21%	22.1	31	34
Modulation	64QAM SC		64QAM OFDM		64QAM OFDM	64QAM SC	64QAM SC	64QAM OFDM
Data rate (Gb/s)	0.8	6.4	0.8	6.4	0.8	2.4	4.8	0.6
EVM (dB)	-26.3	-24.5	-25	-25	-25	-25.1	-24.6	-24
P_{out} (dBm)	12.1	11.3	11.2	10.8	11.4	10.9	11.36	9.35
PAE avg (%)	17.5	15.3	13.5	12.9	18.1	9.2	17.6	16.4
Area (mm^2)	0.27				0.16	0.2	1.38	0.37



(a)



(b)

Fig. 8. Measured EVM for 64-QAM SC and OFDM signals. (a) Measured EVM for 64-QAM modulated signal with different symbol rates. (b) Measured EVM for 64-QAM OFDM modulated signal with different symbol rates across Pout.

A fabricated prototype demonstrates compact area, exhibits wideband modulation and can be used to build linear and efficient PAs for 5G-NR.

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