Wideband High-Gain Amplifiers in 45-nm CMOS SOI Operating at $0.56f_{\max}$: An Analytical Approach on Reversed Feedback Amplifiers

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Abstract— This article presents a novel feedback amplifier (FBA) architecture to realize sub-terahertz, high-gain, wideband amplifiers. The proposed topology employs a gain-boosting technique in each amplifier cell to increase the gain of a multistage amplifier over a broad bandwidth (BW) when cascaded with a conventional FBA (CFBA). The amplifier cell provides a close-to-$G_{\max}$ gain even when passive losses are present. The multistage amplifier topology is compact and does not need inter-stage matching networks (ISMNs) between its internal cells. Two proof-of-concept *G*-band amplifiers were implemented in a 45-nm CMOS silicon-on-insulator (SOI) process to verify the feasibility of the proposed architecture. These prototypes achieve peak gains of 14 and 20.4 dB, peak saturated output powers of 6 and 6.1 dBm, power-added efficiencies (PAEs) of 3.8% and 3.7%, and minimum noise figures (NFs) of 6.2 dB over 156–193.8 and 157.4–194.2 GHz, respectively. To the best of the authors' knowledge, the presented amplifiers in this work obtain the highest BW among the CMOS amplifiers operating at near-$f_{\max}$.

Index Terms— CMOS, *D*-band, feedback amplifier (FBA), $f_{\max}$, gain boosting, maximum achievable gain ($G_{\max}$), mm-wave, wideband amplifier.

I. INTRODUCTION

TECHNOLOGIES such as high-resolution imaging, advanced radars, and seamless sensing demand consistent, high-power, broadband operation in mm-wave frequency bands. Due to the relatively large unallocated bandwidth (BW) available in *D*- and *G*-band spectra, ultra-fast, low-latency communication with data rates as high as 100 Gb/s is feasible at these bands [1], [2], [3]. At sub-THz frequencies, communication systems require multiple gain blocks to compensate for the increased propagation loss and atmospheric attenuation and to boost the signal strength over a broad frequency range [4], [5]. These gain blocks need active devices with a high $f_{\max}$

to support operation at sub-THz frequencies. HBT devices in SiGe and InP technologies have achieved $f_{\max}$ values of over 700 GHz, but they are expensive and offer less integration compared to CMOS. As scaling of CMOS continues, devices with $\approx$400-GHz $f_{\max}$ are accessible for circuit designers, and thus, sub-THz gain blocks can also be implemented in CMOS.

Sub-THz circuit design in CMOS is, however, challenging. At the *G*-band, the dissipative loss associated with device internal parasitics and passive elements dominates the device performance. Consequently, the maximum available gain (G_{ma}) of the transistors declines dramatically, particularly over half-$f_{\max}$. One remedy to overcome this problem is to cascade multiple stages to obtain a higher gain, but this increases the chip area and dc power consumption. Another solution is to enhance the gain per amplifier stage by employing positive feedback and boosting the device gain up to $G_{\max}$ [6], [7], [8], [9], [10], [11], [12], [13], [14], while preserving unconditional stability ($K \geq 1$). Indeed, it was shown by Singhakowinta and Boothroyd [11] that under a linear, lossless, reciprocal (LLR) embedding network, an active two-port (A2P) can obtain maximum achievable gain of $G_{\max} = (2U-1)+2(U(U-1))^{1/2}$, where U is the unilateral gain of the device [12]. Nonetheless, $G_{\max}$ techniques used in feedback amplifiers (FBAs) have been realized only over a narrow BW ($\leq$12%) [2], [6], [7], [8], [9], [10].

To improve the BW, one can adopt the stagger tuning technique by employing multiple cascaded stages tuned at different center frequencies. Despite the wideband gain response, stagger-tuned amplifiers (STAs) often suffer from poor input or output return losses, because each constituting stage is narrowband and exhibits poor matching responses (i.e., S_{11} and S_{22}) at the center frequency of other stages [1], [15], [16]. With the utilization of shunt-embedding and pre-embedding, dual-peak $G_{\max}$-core can be achieved from a transistor, which enhances the gain simultaneously at two different frequencies [2], [17], [18]. A 12% BW is reported in [2] using this technique. However, these amplifiers also suffer from poor matching and the gain of the second peak in $G_{\max}$ is lower than that of first, and thus, the designer has to sacrifice the lower band gain to maintain a flat S_{21}, which also inevitably sacrifices and decays the return loss (S_{11} and S_{22}) [2], [19], [20].

The foregoing discussion suggests that the problem of designing FBAs with high gain and wide BW at near-$f_{\max}$ frequencies needs to be addressed. As such, this work focuses on a feedback topology discussed in [4] and [22]
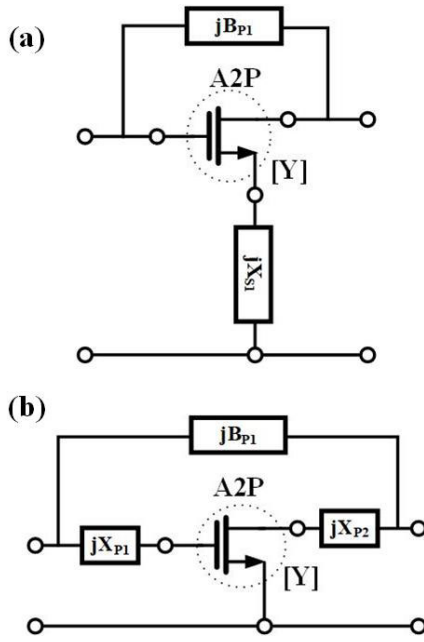
Fig. 1. Structures of CFBAs. (a) A2P embedded by parallel and series embeddings simultaneously. (b) A2P pre-embedded by X_{P1} and X_{P2} and shunt-embedded by B_{P1}.

Fig. 2. Proposed RFBA topology.

and shows its potential for achieving G_{max} over a large BW. The gain-boosting techniques have been reviewed, and the power gain, noise figure (NF), BW, termination impedances, and stability of the feedback cell are studied in the gain plane. Moreover, the cascaded configuration of the feedback cells is analyzed and modeled as an artificial transmission line (TL) shunt-loaded with negative resistors.

To validate the analyses, two G-band amplifiers were designed and implemented in a 45-nm CMOS silicon-on-insulator (SOI) process. The amplifiers achieve 14- and 20.4-dB peak gain over 156–194-GHz ($\approx$21%) BW. The saturated output power (P_{sat}) of both prototypes varies between zero to 6 dBm, depending on the supply voltage level. The amplifiers achieve 6.2–13-dB NF, which is among the best achieved at G-band. To the authors' knowledge, the proposed amplifiers feature the highest BW among the CMOS amplifiers operating at the G-band.

The remainder of this article is organized as follows. FBA architectures and the structure under study are reviewed in Section II. The theoretical analyses are presented in Section III. The performance metrics such as the power gain and BW of the cascaded configuration are investigated in Section IV. The designed amplifiers in 45-nm CMOS SOI technology are explained in Section V, followed by the measured results in Section VI. A summary of this article is provided in Section VII.

II. STRUCTURES OF FEEDBACK AMPLIFIERS

A. Conventional Feedback Amplifiers

Fig. 1 shows the two common structures of FBAs that have been widely discussed in the literature and can potentially lead the A2P to G_{max} operation point [2], [6], [7], [8], [9], [10]. A2P is modeled with admittance parameters. In Fig. 1(a), the G_{max}-core is realized by adding two reactive elements to
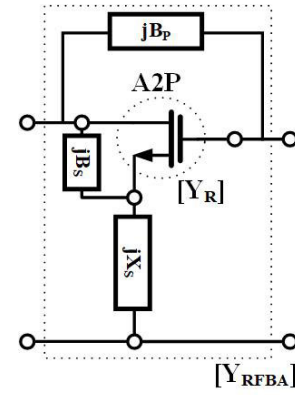
A2P (parallel embedding with admittance of jB_{P1} and series embedding with impedance of jX_{S1}), and Fig. 1(b) shows the G_{max}-core with three reactive elements (pre-embeddings with impedances of jX_{P1} and jX_{P2}, and then, parallel embedding with admittance of jB_{P1}). Nonetheless, the latter structure is preferred, since the series embedded in the former is capacitive [7], [8], [9], and thus, a $\lambda/4$ TL is required to bias the source of the transistor, which adds complexity and additional loss to the structure.

B. Proposed Feedback Amplifier Structure

Fig. 2 depicts the structure of the proposed novel FBA. Unlike conventional structures, the transistor (A2P) in this structure is used in the reverse direction, where its drain and gate are connected to the input and output ports, respectively. The idea of using a transistor in the reverse direction with passive feedback was first proposed in [21] and detailed later in [22], in which the structure is named "constructive-wave amplifier." The analysis gives a good understanding of how signal amplification can be achieved from the constructive-wave structure, from which several takeaways are noticeable.

1) The topology only includes a shunt embedding using a TL.
2) The structure is assumed to be terminated to 50 Ω in the input and output ports, and thus does not include input or output matching networks (IMNs and OMNs).
3) The loading effect of transistor parasitics on the TL is neglected.
4) Only a single optimum design point is determined in which the TL has a length of $\lambda/4$ and characteristic impedance of 50 Ω at the operation frequency.

Considering the above key points, both the topology of the structure and its analysis include several limitations that cause suboptimal operation. As a result, we first revise the topology and then present a more general and comprehensive analysis. The A2P in the proposed structure is embedded simultaneously by parallel and series embeddings. A passive element with an admittance of jB_P between the input and output terminals of the A2P provides shunt-embedding and the series embedding is realized by adding a passive element with an impedance of jX_S in series with the common terminal of the A2P. Moreover, a pre-embedding element with an admittance of jB_S is added to the structure in between the drain and source

nodes. This pre-embedding is capacitive ($C_{\mathrm{ds,ext}}$) and can be absorbed into the drain–source parasitic capacitance of the device (see Section III-A). Several key points are considered in the analysis.

1) Series embedding is added to the topology, which makes the structure capable of $G_{\max}$ operation.
2) As an extra degree of freedom in design, a pre-embedding element (jB_{S}) is included, helping structure implementation and passive losses compensation (see Section III-B).
3) The analysis uses the Y-parameters of the transistor and hence takes into account the full effect of the device's parasitic components.
4) Similar to [7], [8], [9], and [10], the structure is mapped into the gain-plane, and, therefore, the space for design points is given. Optimum load and source impedances are also deducible from the analysis.

We refer to the proposed amplifier as "reversed FBA" (RFBA) for the rest of this article.

III. ANALYSIS OF THE REVERSED FEEDBACK AMPLIFIER

A. Maximum Achievable Power Gain ($G_{\max}$) Operation Point

The maximum available gain (G_{ma}) of an A2P can be boosted to U or $G_{\max}$ with the appropriate design of an LLR embedding network. The definition of U is independent of the direction of the device, and, therefore, $G_{\max}$ should be obtainable from RFBA shown in Fig. 2 as well. The gain-plane approach used in FBA analysis [8], [10] also provides a good graphical representation in the study of the stability and power gain of the RFBA. With the definition of maximum stable gain (MSG) as $A = Y_{21}/Y_{12}$, the loci of constant gain and K-stability factor contours can be located in the gain-plane with axes $x = \Re(1/A)$ and $y = \Im(1/A)$. Therefore, using the admittance parameters of the RFBA cell extracted in Appendix A and assuming $|-Y_{12}/\Delta Y| = |Z_{12}| \ll |X_{\mathrm{S}} + B_{\mathrm{P}}\Delta Z_{\mathrm{S}}|$, the coordinate of the RFBA in the gain-plane is obtained from

$$\frac{1}{A_{\mathrm{RFBA}}} = 1 + j\frac{\frac{Y_{21}}{\Delta Y}}{X_{\mathrm{S}} + B_{\mathrm{P}} \cdot \Delta Z_{\mathrm{S}}}. \quad (1)$$

From [8] and [9], an embedded A2P achieves $G_{\max}$ in the coordinate of the point $(-1/(2U-1+2(U(U-1))^{1/2}), 0)$ of the plane. Thus, for $G_{\max}$ operation, the embedding networks of the RFBA should be designed to satisfy the conditions

$$\Im\left(\frac{\frac{Y_{21}}{\Delta Y}}{X_{\mathrm{S}} + B_{\mathrm{P}} \cdot \Delta Z_{\mathrm{S}}}\right) = 1 + \frac{1}{2U-1+2\sqrt{U(U-1)}} \quad (2a)$$

$$\Re\left(\frac{\frac{Y_{21}}{\Delta Y}}{X_{\mathrm{S}} + B_{\mathrm{P}} \cdot \Delta Z_{\mathrm{S}}}\right) = 0. \quad (2b)$$

To verify (2), a 13.6-μm transistor in a 45-nm CMOS SOI process is used as A2P, and the embedding elements (X_{S} and B_{P}) as well as their corresponding physical implementation at 180 GHz are illustrated in Table I. The pre-embedding jB_{S} is implemented by $C_{\mathrm{ds,ext}}$. For each variation of $C_{\mathrm{ds,ext}}$, solving (2) leads to two $G_{\max}$ operation points, and both cases are realized by TLs for X_{S} and B_{P} implementation. The associated calculated characteristic impedances (Z_{S} and Z_{P}) and electrical length (l_{S} and l_{P}) of the TLs show that only the

TABLE I
THEORETICAL EMBEDDING CALCULATION TO ACHIEVE $G_{\max}$ FOR A 13.6-μm TRANSISTOR AT 180 GHz IN 45-nm SOI

B_{S} (m℧)	$C_{\mathrm{ds, ext}}$ (fF)	X_{S} (Ω)	B_{P} (m℧)	Z_{S} (Ω), l_{S} (deg.)	Z_{P} (Ω), l_{P} (deg.)
∞	0	69.7	-17.15	50, 54.3	65, 63.8
∞	0	606.7	-9.79	50, 85.3	105, 76.6
-2.26	2	68.2	-17.7	50, 53.7	65, 60.4
-2.26	2	336.1	-10.92	50, 81.5	105, 60.7
-4.52	4	65.3	-18.4	50, 52.7	65, 56.6
-4.52	4	251.8	-11.86	50, 78.8	105, 53.4

Bias point: $J = 300\ \mu\mathrm{A}/\mu\mathrm{m}$, $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 0.6$ V. Channel length: 40-nm.
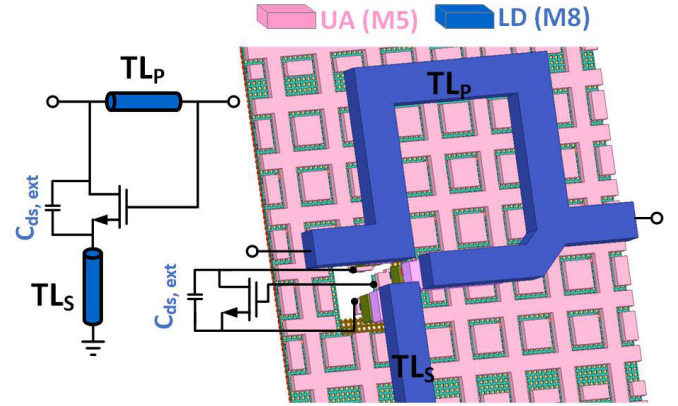

Fig. 3. Pre-embedding ($C_{\mathrm{ds,ext}}$) used to boost the power gain of the RFBA.

first solution is practical since the 105-Ω TL in the second case is not easy to implement in the aforementioned process. Furthermore, l_{S} and l_{P} tend to decrease with higher $C_{\mathrm{ds,ext}}$, thereby introducing lower TL losses which is favorable at mm-wave frequencies.

B. Gain-Boosting Technique Through Device Pre-Embedding

In practice, the loss introduced by embedding elements limits the performance of the proposed RFBA. Therefore, the pre-embedding is employed as an alternative gain-boosting technique to compensate for the losses of the embeddings and is implemented with the additional $C_{\mathrm{ds,ext}}$ placed in between the device's drain and source nodes. Fig. 3 represents an RFBA as well as its physical layout in which $C_{\mathrm{ds,ext}}$ is taken as a design variable. TL$_{\mathrm{S}}$ is not completely shown in Fig. 3. For a given length of TL$_{\mathrm{P}}$ and TL$_{\mathrm{S}}$ simulated using 3-D EM-simulator, G_{ma} of the RFBA is plotted in Fig. 4, and the results illustrates that G_{ma} increases with higher $C_{\mathrm{ds,ext}}$ at 190 GHz, while the amplifier is unconditionally stable below 190 GHz for all $C_{\mathrm{ds,ext}}$ values. The pre-embedding $C_{\mathrm{ds,ext}}$ changes ΔY and ΔZ_{S} in (17), and for a given length of the embedding TLs, it moves the coordinate of the RFBA to the left in the gain plain, thereby leading to higher gains close to $G_{\max}$ operation point and overcoming the loss.

C. Noise Figure

The NF of FBAs has been analyzed in [23], [24], [25], and [26], where a two-port network with internal noise sources is
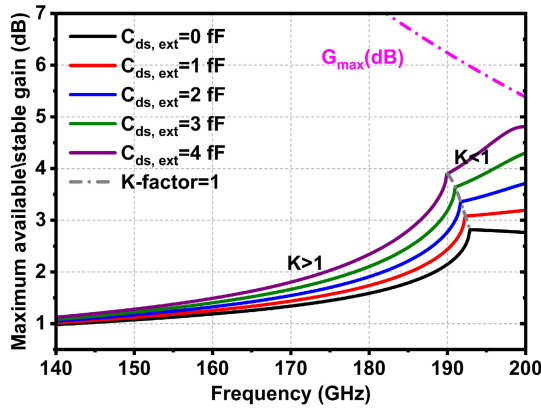
Fig. 4. $C_{ds,ext}$ variation effect on G_{ma}/G_{ms} of an RFBA. The transistor size is 13.6-μm with a 40-nm channel length. Bias point: $J = 300 \ \mu A/\mu m$, $V_{GS} = V_{DS} = 0.6$ V.

Fig. 5. Equivalent noise model of (a) A2P and (b) series- and parallel-embedded A2P.

represented with a noise-free two-port preceded by two equivalent noise sources V_n and I_n [see Fig. 5(a)]. The NF of the A2P is expressed in terms of four noise parameters: the equivalent noise resistance R_n, uncorrelated equivalent conductance G_u, and correlation admittance Y_c. The works demonstrate an accurate mathematical derivation of NF of an embedded A2P only with a single feedback element (either series- or parallel-embedding). Using the method developed in [23], we present a general noise analysis of the A2P embedded by both series and parallel embeddings. The analysis provided applies to both conventional FBA (CFBA) and RFBA structures (see Figs. 1 and 2). Fig. 5(b) shows the embedded A2P with its equivalent input-referred sources V_n' and I_n'. The pre-embedding element jB_s is absorbed into the y-parameters of A2P and does not change the minimum NF. The equivalent noise parameters are derived in Appendix B. Using (18)–(20), the NF of the embedded A2P is demonstrated as

$$\text{NF} = 1 + \frac{G_u}{G_s}|B + A\psi|^2 + \frac{R_n}{G_s}|\psi + Y_c(B + A\psi)|^2 \quad (3)$$

in which $\psi = E + DY_s$, and Y_s and G_s are the source admittance and conductance, respectively.

To study the effect of series- and parallel embeddings on the noise performance of RFBA, two cases are considered.

1) The RFBA is aimed for the minimum noise matching. From (3) and (18)–(21), minimum NF (NF_{min}) is calculated for each coordinate of the gain-plane. The constant NF_{min} contours are plotted in Fig. 6(a). The optimum impedances for noise matching are also derived and the associated gain contours are added to the plot. It can be seen from the graph that the RFBA can achieve 3-dB maximum gain with an NF slightly higher than 4.5 dB, while operating close to the stability boundary.
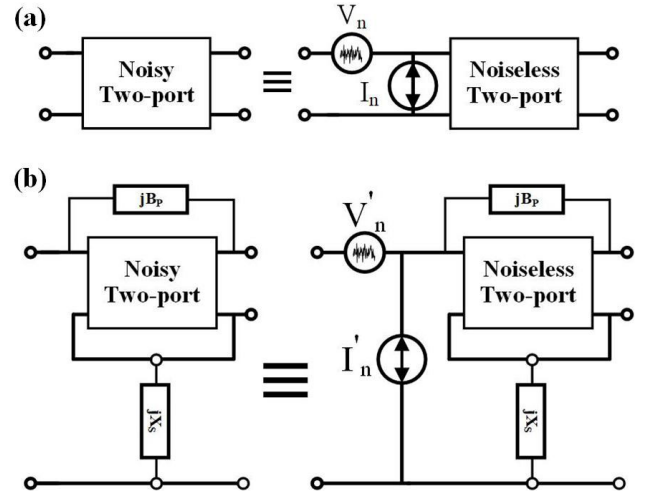
2) The RFBA is aimed for the best gain performance, and thus, designed for maximum available gain. Using the source and load conjugate-matching impedances, the corresponding NF is extracted from (3). The constant NF contours are graphed in Fig. 6(b) varying from 2 to 9 dB. It can be seen from the graph that the upper horizontal half ($\Im(1/A) > 0$) obtains a better NF.

Comparing the two cases, the former does not show a superior simultaneous noise and gain performance over the latter, and its gain is limited to 3 dB. The latter is preferred for an actual design with a gain range of 8.6 dB. Including pre-embedding leads to similar results to Fig. 6. Finally, the NF of a multistage RFBA is derived as

$$\text{NF}_{casc.} = \frac{\text{NF} - G^{-1}}{1 - G^{-1}} \quad (4)$$

where G is the gain [27], and its contours are plotted in Fig. 6(c).

IV. Cascaded Reverse Feedback Amplifiers

Due to low available gain from a single-stage amplifier in the mm-waveband, several amplifying cells (amp-cells) need to be cascaded to attain the desired gain. An inter-stage matching network (ISMN) is required in between the cells to terminate the amp-cell to the desirable load and source impedances. However, ISMNs are lossy (1–2 dB at the G-band) and often limit the BW. To avoid such issues, we investigate the performance of the cascaded amp-cells while no ISMN is included, and its performance is compared to the conjugate-matched cascaded amp-cells.

$$Y_{S,IT} = \frac{Y_{11,RFBA} - Y_{22,RFBA}}{2} + \frac{\sqrt{\left(Y_{11,RFBA} + Y_{22,RFBA}\right)^2 - 4Y_{21,RFBA}Y_{12,RFBA}}}{2} \quad (5a)$$

$$Y_{L,IT} = \frac{Y_{22,RFBA} - Y_{11,RFBA}}{2} + \frac{\sqrt{\left(Y_{11,RFBA} + Y_{22,RFBA}\right)^2 - 4Y_{21,RFBA}Y_{12,RFBA}}}{2} \quad (5b)$$

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Fig. 7. Mismatch loss $(G_{IT,dB} - G_{ma,dB})$ contours on the gain-plane at 175 GHz for an embedded 13.6-μm NMOS transistor in 45-nm CMOS SOI ($L_g = 40$ nm). Bias point: $J = 300$ μA/μm, $V_{GS} = V_{DS} = 0.6$ V.

Fig. 8. Equivalent circuit of the RFBA cell terminated to iterative impedances used for transducer gain analysis.

then, the maximum G_{IT} is selected for each point in the gain-plane. Fig. 7 illustrates the mismatch loss $(G_{IT,dB} - G_{ma,dB})$ due to the elimination of ISMNs in between the amp-cells. Cascading multiple RFBAs with no ISMNs is beneficial in terms of gain, BW, and die area.

1) Because ISMNs presents 1–2-dB dissipative loss and often limit the BW at G-band, any design point chosen inside the -2-dB contour in Fig. 7 will result in the same or better gain performance compared to G_{ma} as well as higher BW for two or more cascaded amp-cells. Later, it will be shown that the loaded TL_p is equivalent to an artificial TL, and hence, all cells are intrinsically matched.

2) The ISMN exclusion from the design leads to an area-efficient amplifier.
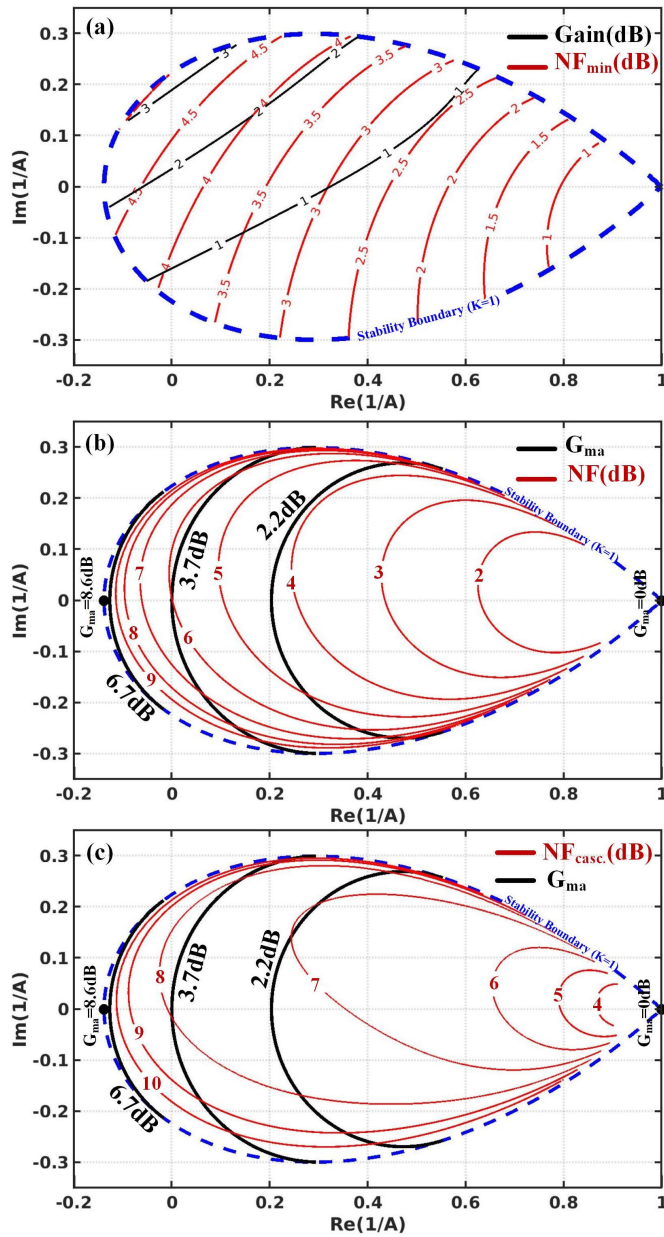

Fig. 6. (a) Contours of constant minimum NF (NF$_{min}$) as well as corresponding gain achieved from minimum NF matching on the gain-plane. (b) Contours of equi-G_{ma} and associated NF under conjugate-matching condition ($U = 3.7$ dB). (c) NF contours of cascaded RFBAs along with equi-G_{ma} contours of a single stage RFBA at 175 GHz. The transistor size is 13.6-μm with a 40-nm channel length. Bias point: $J = 300$ μA/μm, $V_{GS} = V_{DS} = 0.6$ V.

A. Iterative Impedance

Assuming an infinite chain of identical cascaded RFBAs, all amp-cells experience identical source (Y_S) and load (Y_L) admittances which are called iterative admittances ($Y_{S,IT}$ and $Y_{L,IT}$). The corresponding termination admittances are given in (5), as shown at the bottom of the previous page. Having calculated $Y_{S,IT}$ and $Y_{L,IT}$, we can derive the associated transducer power gain (G_{IT}) and compare it to G_{ma}. For each point in the gain-plane, the associated shunt-embedding TL_p shown in Fig. 3 can be implemented over a range by adjusting its characteristic impedance (Z_p). TLs are assumed to be lossless. To find the best G_{IT}, hence, Z_p is swept from 40 to 90 Ω, and
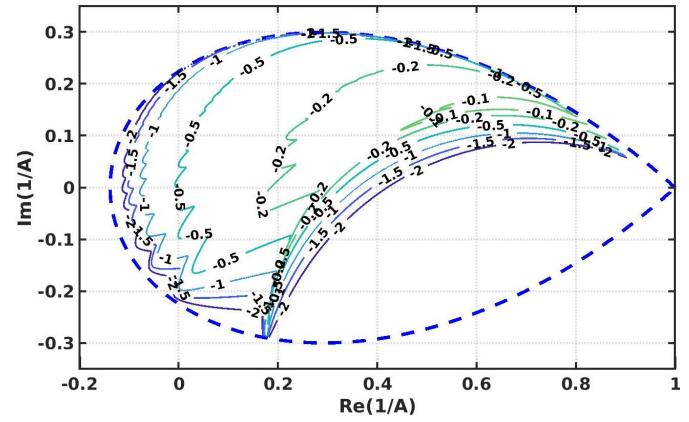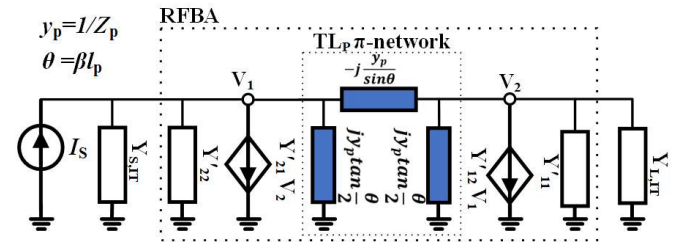
B. Analytical Behavior of Cascaded RFBAs

Fig. 8 shows the equivalent circuit of an RFBA terminated to iterative impedances, which is used to analyze the RFBA transducer gain. TL_p is substituted with its equivalent π-network, where $y_p = 1/Z_p$. The Y-parameters of the network loading the line represents the reversed device with series embedding and pre-embedding and are shown in (15) in Appendix A, where $B_S = C_{ds,ext}\omega$ and $X_S = Z_S \tan\theta$ ($\theta = \beta l_p$ in which $\beta = 2\pi/\lambda$ is the wavenumber). From KCL analysis, both voltage controlled current sources (VCCSs) in Fig. 8 can be replaced with their equivalent
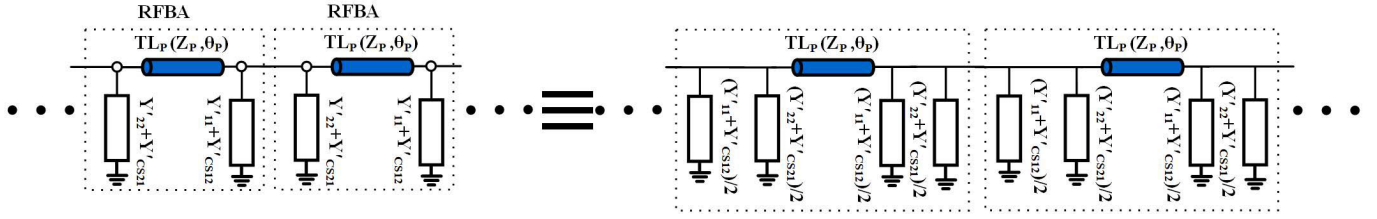
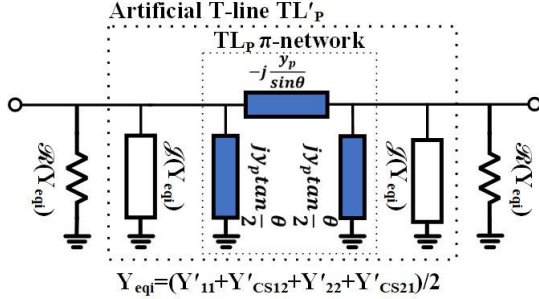Fig. 9.   Equivalent circuit of the cascaded RFBA cells.

Fig. 10.   Simplified equivalent circuit of a cell in a cascaded configuration of RFBAs.

admittances as

$$Y'_{CS12} = \frac{Y'_{12}V_1}{V_2} = -\left(Y_{21,RFBA} - \frac{j(y)_p}{\sin\theta}\right)\frac{Y_{22,RFBA} + Y_{L,IT}}{Y_{21,RFBA}} \quad (6a)$$

$$Y'_{CS21} = \frac{Y'_{21}V_2}{V_1} = -\left(Y_{12,RFBA} - \frac{jy_p}{\sin\theta}\right)\frac{Y_{21,RFBA}}{Y_{22,RFBA} + Y_{L,IT}}. \quad (6b)$$

Fig. 9 depicts the simplified model of RFBA cells in a cascaded configuration in which VCCSs are replaced with their equivalent admittances. The model presented herein applies only to the forward-propagating signal. Thanks to ISMN exclusion, shunt loadings of the TL_P can be shared between the cells, and as a result, a single cell model is simplified to TL_P with symmetric shunt loading (Y_{eqi}), which is

$$Y_{eqi} = \frac{Y'_{22} + Y'_{11} + Y'_{CS21} + Y'_{CS12}}{2}. \quad (7)$$

Fig. 10 concludes the final equivalent circuit of a cell in a cascaded configuration of RFBAs. The shunt loading Y_{eqi} is separated into imaginary and real parts. TL_P symmetrically shunt-loaded with $\Im(Y_{eqi})$ creates a new π-network and is equivalent to an artificial TL, whose characteristic impedance (Z'_P) and propagation factor (e^γ) [28] are

$$Z'_P = \frac{1}{\sqrt{y_1(y)_2 + \frac{y_2^2}{4}}} \quad (8a)$$

$$e^\gamma = 1 + \frac{y_2}{2y_1} + \sqrt{\frac{y_2}{y_1} + \frac{y_2^2}{4y_1}} \quad (8b)$$

where

$$y_1 = -j\,\frac{y_p}{\sin\theta} \quad (9a)$$

$$y_2 = 2j\left(\Im(Y_{eqi}) + y_p\,\tan\frac{\theta}{2}\right). \quad (9b)$$

To summarize, we showed that cascaded RFBAs can be modeled as a cascade of artificial TLs (TL'_P) symmetrically shunt-loaded with frequency-dependent resistors [$\Re(Y_{eqi})$]. Ideally, without the shunt resistive loading, the gain of a cascaded TL'_P is equal to one in its passband, and both attenuation and amplification can be obtained from the structure given $\Re(Y_{eqi})$ is positive or negative, respectively. Since power amplification is targeted in the forward direction, the shunt loading of the TL'_P has to be a negative resistor, while a positive resistor is favorable in the reverse direction to guarantee stability.

To evaluate the behavior of the proposed model, a 13.6-μm NMOS transistor in the 45-nm SOI process biased at $J = 300\ \mu A/\mu m$, $V_{GS} = V_{DS} = 0.6$ V is chosen and embedded with 50-Ω TLs ($\theta_P = 59.3°$ and $\theta_S = 65.4°$ at 180 GHz). No pre-embedding is included for simplicity, and its effect on the design parameters is discussed later in Section V-A. The resulting characteristic impedance (Z'_P), propagation factor (e^γ) of TL'_P, and $\Re(Y_{eqi})$ are graphed in Fig. 11. The equivalent artificial line TL'_P is a bandpass filter with resonance frequencies of 85 and 202 GHz. It can also be seen from Fig. 11 that the following holds.

1) *For 85 GHz $< f <$ 202 GHz (Passband):* Z'_P and γ are real and imaginary, respectively. The phase of e^γ increases from zero at 85 GHz and reaches 90° at 175 GHz. Then, it starts decreasing and reaches zero again at 202 GHz. In the passband, $|e^\gamma| = 1$.

2) *For $f <$ 85 GHz and $f >$ 202 GHz (Stopband):* Z'_P is imaginary and e^γ becomes real and higher than one, showing a rising attenuation.

Hence, signal amplification can only occur in the passband of TL'_P and only if it is loaded with a negative resistor. Graphed in Fig. 11(c), $\Re(Y_{eqi})$ has four resonance frequencies 140,197,207, and 239 GHz, and it becomes negative at 140 GHz $< f <$ 197 GHz and 207 GHz $< f <$ 239 GHz. The latter is out of scope due to its occurrence in the stopband, while the former determines the amplification range that can be achieved from the structure in this specific example. At resonance frequencies of 140 and 197 GHz, the transducer power gain obtained from cascaded RFBAs is 0 dB and reaches the maximum of 1.8 dB in the passband [see Fig. 11(c)]. Also, a small variation of Z'_P in the amplification range provides reasonable input and output matching conditions for the full cascaded amplifier, highlighting the superior matching performance of RFBA over CFBA.

C. Center Frequency (f_c)

The simplified model of Fig. 12 is utilized to find the center frequency of cascaded RFBAs. TL_0 has a constant
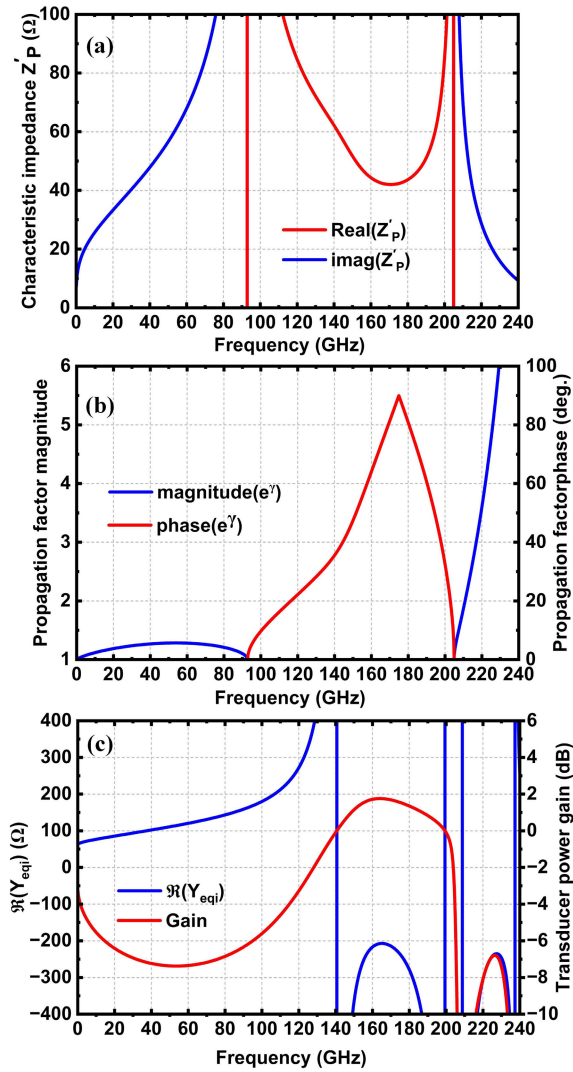
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Fig. 13. Transducer power gain (G_{IT}) of a 50-Ω TL shunt-loaded with negative resistors and terminated to its associated iterative impedances.

solution of $\theta = 0.5\pi$, and hence, the maximum gain is

$$G_{IT,max} = Z_0^2\left(\sqrt{Y_0^2 + G_n^2} + G_n\right)^2 \qquad (11)$$

which shows peak gain can be increased with higher G_n or Z_0. Fig. 13 graphs G_{IT} for a 50-Ω TL with 0.5π length at 175 GHz, and shunt-loaded with negative resistors ranging from 50 to 300 Ω. The structure has flat responses over a wide BW and achieves higher gain with higher G_n. The graph also shows that f_c remains unaffected by the value of G_n and is at 175 GHz, as the line corresponds to a quarter wavelength at that frequency. Referring back to the propagation factor plotted in Fig. 11(b), TL_P' is also centered at 175 GHz with an electrical length of $\pi/2$. Nevertheless, since $\Re(Y_{eqi})$ and Z_P' are frequency-dependent, and also, $\Re(Y_{eqi})$ peak has a slight shift from 175 GHz, the simulated f_c deviates from 175 about 3 GHz.

D. Bandwidth

In the cascaded configuration of RFBAs, the variation of the propagation factor (e^γ), Z_P', and $\Re(Y_{eqi})$ causes gain change over the frequency [see Fig. 11(c) and (10)]. The total gain of the cascaded RFBA cells is the multiplication of the gain of each individual cell (G_{IT}). To find 3-dB BW of n-cascaded cells, first, the power gain of the single stage ($G_{IT@fx}$) at the 3-dB frequency (f_k) of n-stage amplifier is determined from

$$20\log\left(\frac{G_{IT,max}}{G_{IT@fk}}\right)^n = 3. \qquad (12)$$

Then, the calculated value of $G_{IT@fk}$ is mapped into Fig. 11(c) and the 3-dB BW corresponding frequencies are extracted. For instance, for $n = 9$, BW is 27.4 GHz, from 153 to 179 GHz, and it is in close agreement with the simulation results (149–174 GHz).

E. Reverse Gain

A similar approach is utilized to analyze the reverse gain of cascaded RFBAs shown in Fig. 14. Similar to forward gain modeling, here the VCCSs are replaced by their equivalent admittances

$$Y_{CS21r}' = -\left(Y_{12,RFBA} - \frac{jy_p}{\sin\theta}\right)\frac{Y_{11,RFBA} + Y_{S,IT}}{Y_{12,RFBA}} \qquad (13a)$$

$$Y_{CS12r}' = -\left(Y_{21,RFBA} - \frac{jy_p}{\sin\theta}\right)\frac{Y_{12,RFBA}}{Y_{11,RFBA} + Y_{S,IT}}. \qquad (13b)$$

Fig. 11. (a) Characteristic impedance (Z_P') of TL_P'. (b) Propagation factor (e^γ) of TL_P'. (c) $\Re(Y_{eqi})$ and power gain for a 13.6-μm NMOS transistor in 45-nm SOI embedded with 50-Ω TLs ($\theta_P = 57.8°$ and $\theta_S = 65.4°$ at 175 GHz). Bias point: $J = 300\ \mu A/\mu m$, $V_{GS} = V_{DS} = 0.6$ V.
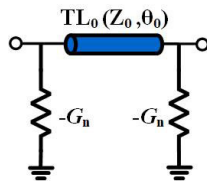

Fig. 12. TL loaded with shunt negative resistors.

characteristic impedance with the propagation factor of $e^{-j\theta}$ and is loaded with shunt constant negative resistors (G_n). Assuming the structure terminated to its corresponding iterative impedances and $Y_0 = 1/Z_0$, G_{IT} is derived as

$$G_{IT} = -Z_0^2\ \sin^2\theta$$
$$\times \left(\sqrt{Y_0^2 + G_n^2 + 2jG_nY_0\ \cot\theta} + G_n + jY_0\ \cot\theta\right)^2. \qquad (10)$$

At center frequency, G_{IT} must reach its peak value. This implies that the derivative of G_{IT} is zero, which leads to the
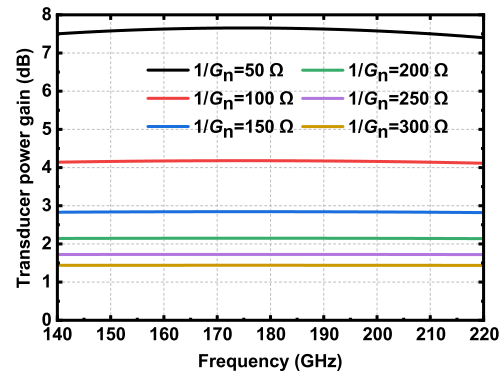
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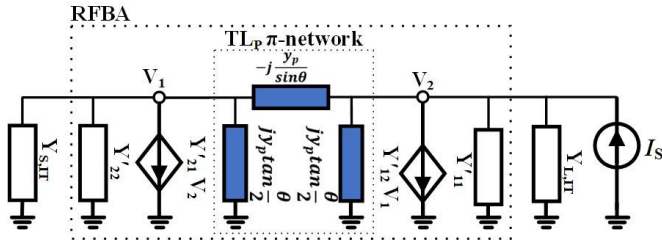8   IEEE JOURNAL OF SOLID-STATE CIRCUITS

Fig. 14. Equivalent circuit of the RFBA cell terminated to iterative impedances used for reverse gain analysis.

Fig. 16. G_{ma}/G_{ms} and stability factor of CFBA and RFBA for an embedded 13.6-μm NMOS transistor in 45-nm CMOS SOI ($L_g = 40$ nm). Bias point: $J = 300$ μA/μm, $V_{GS} = V_{DS} = 0.6$ V.

F. Cascade of RFBA and CFBA

Here, we propose a new technique that utilizes cascading two single-peak G_{max}-cores tuned at two different frequencies to achieve high-gain and wideband response simultaneously. G_{ma}/G_{ms} of a 13.6-μm NMOS transistor embedded in both CFBA and RFBA structures is plotted in Fig. 16. CFBA has a peak G_{ma} achieving 8 dB at 150 GHz (f_1) and is unconditionally stable above that, while the RFBA obtains its G_{ma} peak with 4 dB gain at 190 GHz (f_2) and is unconditionally stable below it. Therefore, an unconditionally stable amplifier with flat S_{21} between f_1 and f_2 can be realized by cascading both structures. To compensate for the lower G_{ma} of RFBA at f_2 compared to that of CFBA at f_1, multiple cells of RFBAs should be cascaded, which gives a degree of freedom to the designer to tune for the best performance. The proposed technique is equivalent to stagger-tuning; however, full matching is achievable across the BW, thanks to the artificial TL structure of RFBA cells.

V. CIRCUIT DESIGN

Two G-band amplifiers are designed and implemented in a 45-nm CMOS SOI process with eight metal layers and a trap-rich substrate. The design employs thin-oxide floating-body nMOS FETs with a 40-nm channel length. Transistor layout techniques discussed in [29], [30], and [31] were employed to minimize interconnect parasitics. Double-side contacts and a relaxed pitch are incorporated into the gates to minimize resistance. Considering the device power consumption and G_{ma} at the G-band, the design uses the transistor size of 13.6 μm (16 × 850 nm) for all amp-cells, which has an f_{max} of 273 GHz when referenced to the fourth metal layer (C1). The top 4.1-μm-thick aluminum layer (LD) is employed to implement TLs, and all passive networks above the fourth metal layer (UA–LD) including RF pads are simulated using 3-D electromagnetic simulator.

Fig. 17 presents the schematics of the designed amplifiers for the two variants. Amp-A [see Fig. 17(a)] consists of ten-cascaded stages, including one CFBA and nine RFBA cells. The transistors in Amp-A are biased at $J = 272$ μA/μm, $V_{GS} = V_{DS} = 0.58$ V. Amp-B [see Fig. 17(b)] has 11-cascaded stages, including two CFBA and nine RFBA cells with the bias point of $J = 235$ μA/μm, $V_{GS} = V_{DS} = 0.55$ V. The bias points are chosen based on the gain requirement while minimizing power consumption. We have avoided the
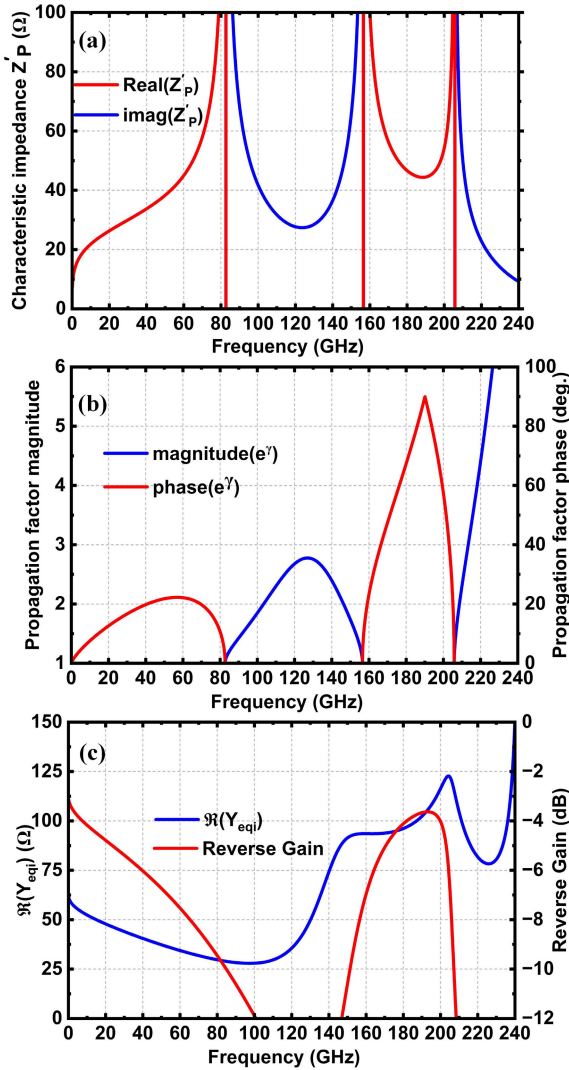

Fig. 15. (a) Characteristic impedance (Z'_P) of TL$'_P$, (b) propagation factor (e^γ), and (c) $\Re(Y_{eqi})$ and power gain in the reverse direction for a 13.6-μm NMOS transistor in 45-nm SOI embedded with 50-Ω TLs ($\theta_P = 57.8°$ & $\theta_S = 65.4°$ at 175 GHz). Bias point: $J = 300$ μA/μm, $V_{GS} = V_{DS} = 0.6$ V.

Graphed in Fig. 15, TL$'_P$ in the reverse direction has pass-bands of 0–90 and 155–205 GHz; however, it is shunt-loaded with resistors ($\Re(Y_{eqi}) > 0$) at all frequencies [see Fig. 15(c)], confirming the attenuative functionality of the RFBA cell in the reverse direction. This is because the positive feedback is only present in the forward direction, which generates negative resistance. Conversely, there is an absence of feedback in the reverse direction. This behavior is required for stability. The reverse gain is presented in Fig. 15(c).
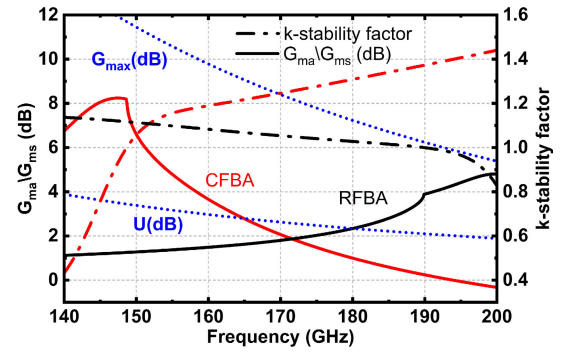
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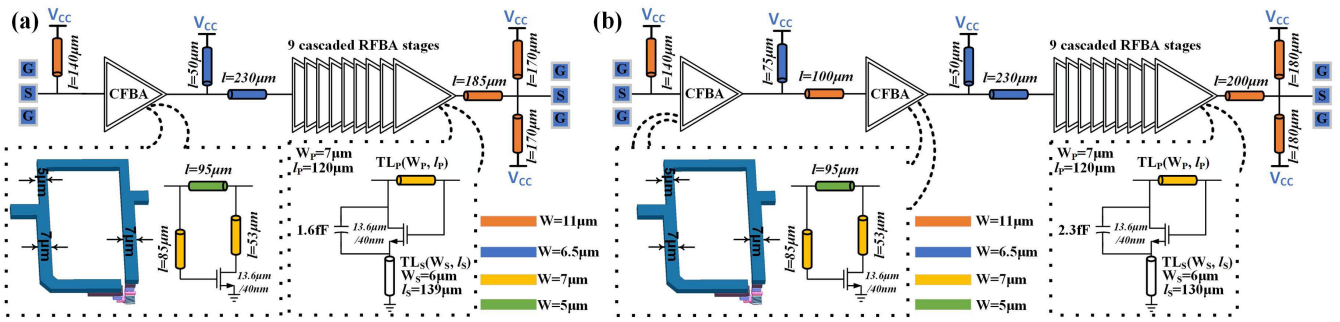

Fig. 17.   Circuit diagram of designed BW-extended *G*-band amplifiers. (a) Amp-A prioritizes a flat gain and wide BW. (b) Amp-B is designed to achieve higher gain.
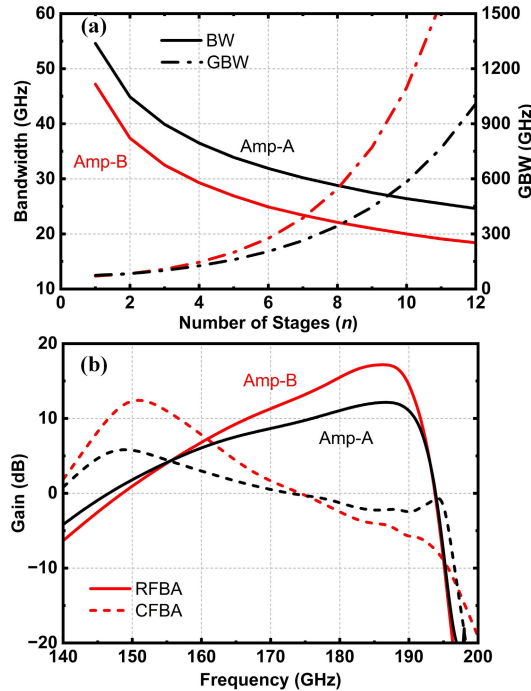

Fig. 18.   (a) Theoretical BW and GBW of RFBA cells in Amp-A and Amp-B versus a number of stages. (b) Post-layout EM-simulated gain of RFBA and CFBA cells in Amp-A and Amp-B versus frequency.

Fig. 19.   Chip micrographs of Amp-A (top) and Amp-B (bottom). The chip dimensions of Amp-A and Amp-B are 0.6 × 1.33 and 0.58 × 1.5 mm, respectively.

additional loss from using a dc block capacitor between the gates and drains; however, for more tuning and design flexibility, the gates and drains can be biased separately in amp-cells. Several shunt stubs are included in the matching networks (MNs) to bias the amplifier and balance V_{DD} across the chip. ISMNs are only included in between CFBA and the first RFBA cell, as well as in between cascaded CFBA stages. Post-layout simulated G_{ma} of both CFBA and RFBA cells are plotted in Figs. 4 and 16. The design goal is to obtain above 12 dB gain with 3-dB BW exceeding 35 GHz for both variants.

A. RFBA Cell

Two different types of RFBA cells are employed in the design. In Amp-A, the RFBA cell is optimized for maximum BW, while Amp-B aims for higher gain by including larger $C_{ds,ext}$ (see Fig. 4) and an extra CFBA cell. Also, a longer TL_S moves the coordinate of the amp-cell to the right in the gain-plane, resulting in lower gain and broader BW. Thus, the length of TL_S in Amp-A is higher than that in Amp-B
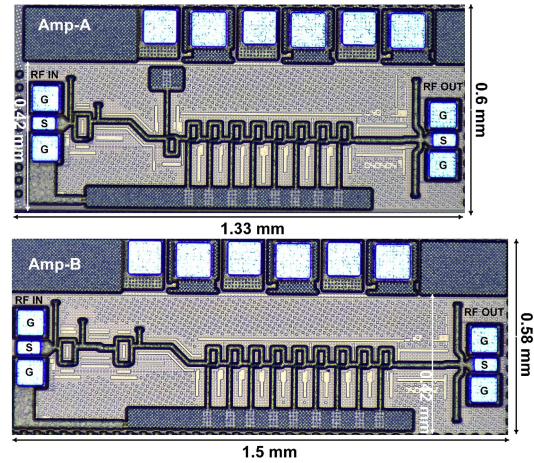
to achieve a flatter gain. Fig. 18(a) depicts the theoretical BW and gain BW product (GBW) for the two variants of RFBA cells. There are two main trade-offs between gain and BW to consider. First, in cell design, the selection of design parameters (TL_P, TL_S, and $C_{ds,ext}$) leads to either broader BW (Amp-A) or higher gain and GBW (Amp-B). Second, having more cascaded cells tends to decrease BW despite higher gain. For this work, we have chosen to use nine cascaded RFBA cells to ensure that at least a minimum gain of 11 dB is achieved. No MN is included in between the RFBA cells since their input and output impedances are very close to the conjugate matching impedances. OMN including the RF output pad was designed to terminate the RFBA cells to the required $Y_{L,IT}$. Here is the summary of post-layout simulation results of a single cell RFBA.

1) The coordinates of the Amp-A and Amp-B in the gain plane are (0.47, 0.28) and (0.37, 0.29) at 175 GHz.
2) The passband of TL_P' is 46 GHz < f < 194.5 GHz.
3) $\Re(Y_{eqi})$ remains negative (amplification range) in 146.8 GHz < f < 194.2 GHz. The designer has to make sure that the amplification range of the RFBA also covers the CFBA operation band; otherwise, RFBA would be attenuative when cascaded with a CFBA cell.
4) The phase of the propagation factor reaches 0.5π at 174 GHz.
5) The peak negative resistance of $\Re(Y_{eqi})$ is −280 (Amp-A) and −220 Ω (Amp-B) at 178 GHz.

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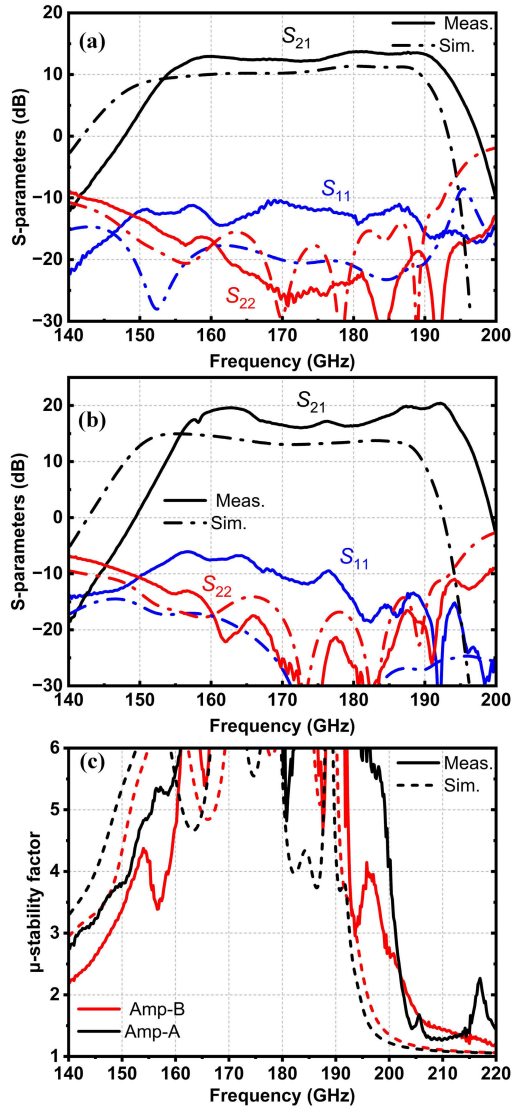
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Fig. 20. Measured (solid) and simulated (dashed) S-parameters of (a) Amp-A, (b) Amp-B, and (c) μ-stability factor. The devices in Amp-A are biased at $J = 272$ $\mu A/\mu m$, $V_{GS} = V_{DS} = 0.58$ V. Amp-B has the bias point of $J = 235$ $\mu A/\mu m$, $V_{GS} = V_{DS} = 0.55$ V.

6) G_{IT} is 1.4 (Amp-A) and 1.75 dB (Amp-B) at 178 GHz and only 0.2 dB less than G_{ma}, which justifies the exclusion of MNs in between the RFBA cells.
7) 3-dB BW for nine cascaded RFBA cells is theoretically 27.5 GHz for Amp-A (162.3–189.8 GHz) and 21 GHz for Amp-B (167.6–188.6 GHz).
8) The NF of cascaded cells [see Fig. 6(c)] is 9.3 (Amp-A) and 8.8 dB (Amp-B) at 175 GHz.

The finalized post-layout design of nine cascaded RFBA cells, including the surrounding dummy structures, exhibits performance deviations compared to a single-cell configuration. These changes are due to inter-cell coupling and asymmetric dummies around the cells which alter the effective length of TL_P and TL_S. The post-layout EM simulation results of RFBA cells in Amp-A and Amp-B are plotted in Fig. 18(b) and summarized below.

1) The peak gain frequency is centered at 186.6 (Amp-A) and 186.2 GHz (Amp-B).
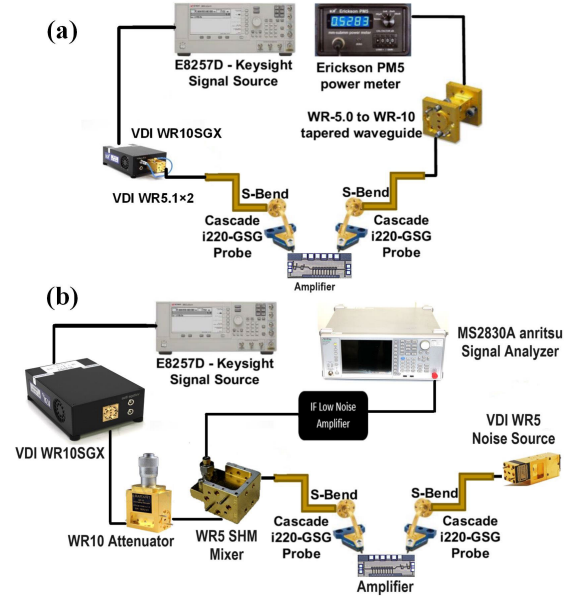2) The amplification range is 146.6–193.8 (Amp-A) and 148.6–193.8 GHz (Amp-B).

Fig. 21. Setups for (a) large-signal and (b) NF measurements.

3) At the peak gain frequency, G_{IT} is 1.4 (Amp-A) and 1.9 dB (Amp-B).
4) 3-dB BW is 172.2–191.4 GHz for Amp-A and 177.2–190.2 GHz for Amp-B.

The post-layout performance meets the targeted BW exceeding 35 GHz when cascaded with CBFA cells; however, the designer can fine-tune the aforementioned parameters by employing layout techniques and creating more isolation in between the cells.

B. CFBA Cell

The CFBA cell is designed and embedded to boost the gain at the lower-end of the amplification band (see Fig. 16) and hence extend the BW. The theoretical derivation of embeddings to achieve G_{max} peaking in CFBAs is discussed in [2]. The decision regarding the number of CFBA cells to cascade in the design relies only on the criteria of flattening the gain response achieved from RFBA cells. Therefore, Amp-A employs a single cell of this type, whereas two cells of CFBAs are utilized in Amp-B due to its RFBA cells' higher gain. CFBA cells are conjugately matched to RFBAs and optimized to flatten S_{21}. RF pads are treated as part of IMN and OMN. CFBA NF is 5.5 dB at 175 GHz, and their post-layout EM-simulated gain in Amp-A and Amp-B is plotted in Fig. 18(b). Unlike traditional STAs and dual-peak G_{max}-core amplifiers, the presented amplifier provides input and output matching over its entire amplification band.

VI. MEASUREMENT RESULTS

Fig. 19 shows the die photograph of the fabricated amplifiers. The dimensions of the Amp-A and Amp-B excluding the dc pads are 0.42×1.33 and 0.42×1.5 mm, respectively. The S-parameters of the amplifiers were measured by a Keysight N5247A PNA-X connected to two VDI WR-5.1 frequency extenders. Fig. 20 illustrates the measured and simulated S-parameters. Amp-A maintains a flat gain response,
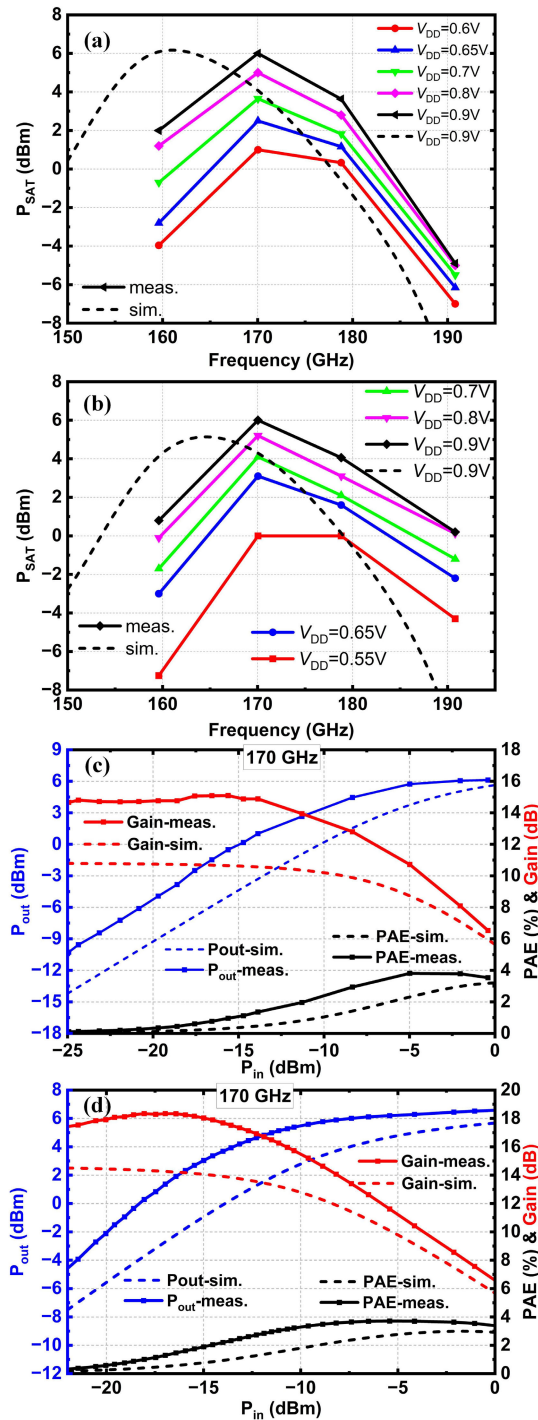
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Fig. 22. Measured (solid) and simulated (dashed) saturated output power (P_{sat}) of (a) Amp-A and (b) Amp-B versus frequency operating at various supply voltage levels. Measured gain, PAE, and output power of (c) Amp-A and (d) Amp-B versus input power at 170 GHz ($V_{DD} = 0.9$ V).
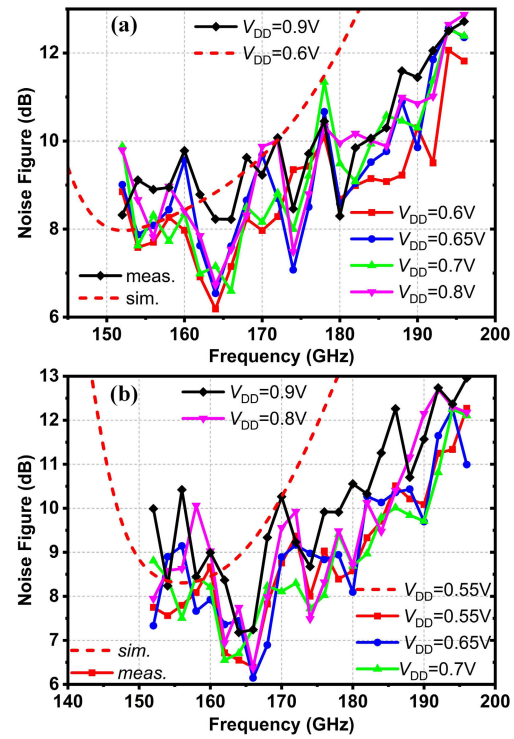

Fig. 23. Measured (solid) and simulated (dashed) NF (dB) of (a) Amp-A and (b) Amp-B versus frequency at various supply voltage levels.

gain, and the measured center frequency is shifted up by almost 4%. The discrepancies are likely due to inaccuracies related to process variation of $C_{ds,ext}$ and electrical length of TL_S. Both amplifiers are unconditionally stable with the μ-factor above one [see Fig. 20(c)].

Fig. 21(a) presents the large-signal measurement setup. The losses of the probes and S-bends are de-embedded, and the power reference planes are at the probe tips [32]. P_{sat} of Amp-A and Amp-B at different supply voltage (V_{DD}) levels versus RF frequency are demonstrated in Fig. 22(a) and (b), respectively. P_{sat} varies in the range of -7 to 6 dBm depending on the V_{DD} value. At higher- and lower-end of the BW, P_{sat} is lower than that of the center frequency in both amplifiers due to higher gain-boosting and soft compression [33]. The measured gain, power-added efficiency (PAE), and output power of the Amp-A and Amp-B with 0.9-V supply are shown in Fig. 22(c) and (d). At 170 GHz, Amp-A attains peak P_{sat} and OP1dB of 6/2.8 dBm with associated PAE of 3.8%/2%, while for Amp-B, the peak P_{sat} and OP1dB reach 6.1/4.4 dBm with associated PAE of 3.7%/2.6%, respectively. The results show a good consistency with their simulation counterparts.

The amplifiers' NF were measured across the 152–196-GHz frequency range utilizing the setup depicted in Fig. 21(b). Calibration was performed for the VDI WR5.1-band noise source, subharmonic mixer, and IF amplifier collectively, and the probe and waveguide losses were de-embedded. As shown in Fig. 23, the NF of both amplifiers is in the range of 6.2–13 dB and slightly better than that of the simulation due to the higher gain in measurements. The performance of the designed amplifiers is compared to the similar published works operating at close to f_{max} frequencies in Table II. The gain, NF, BW, power consumption, and figure of merit (FOM)

reaching a maximum of 14 dB, and has a 3-dB BW spanning from 156 to 193.8 GHz. Furthermore, the amplifier experimentally achieves full matching across the BW with input and output reflection coefficients better than -10 and -16 dB, respectively. Amp-B demonstrates a maximum gain of 20.4 dB, with a passband ripple of 4.2 dB, within a BW ranging from 157.4 to 194.2 GHz. The measured S_{11} and S_{22} remain lower than -6 and -13 dB across the BW, respectively. Compared to simulation results, both amplifiers achieve higher

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TABLE II
COMPARISON WITH OTHER AMPLIFIERS OPERATING AROUND $f_{\max}/2$

Reference[△]	Topol.[◇]	Process	$f_{\max}$ (GHz)	Freq. (GHz)	BW$_{\text{F}}$ (%)	$\frac{f_c}{f_{\max}}$	S_{21} (dB)	P_{DC} (mW)	Area (mm^2)	NF (dB)	OP1dB (dBm)	P_{sat} (dBm)	FoM[⋆]
TMTT-2021 [1]	2 CE	55-nm SiGe	370	110-175	46.8	0.37	20.6	24	0.08[†]	NA	0	NA	NS
MWTL-2023 [3]	7 CE	130-nm SiGe	500	140-220	45.6	0.35	15.5	46	0.48	6.1	−2.2	5	11.4
ICECS-2019 [37]	3 CE	130-nm SiGe	450	150-206	31.9	0.39	22	65	0.65	NA	1	5	15.7
WiMob-2019 [36]	7 CE	130-nm SiGe	450	140-220	45.6	0.39	19	42	0.55	7.1	−7.5	0	11.2
TST-2022 [34]	4 Cas.	130-nm SiGe	450	247-314	24	0.62	15	268	0.58	NA	3.3	5	5.4
JSSC-2019 [2]	4 CS	65-nm CMOS	395	227-257	12.4	0.61	13.9	23.8	0.14	NA	−5	-3.3	3.5
JSSC-2021 [6]	2 CS	28-nm CMOS	395	247	NA	0.63	18	21.5	0.3	NA	−9.5	0.1	NS
TMTT-2018 [35]	4 CS	28-nm FD SOI	390	143-166	14.9	0.4	15.7	32	0.34	8.5	−3	1.5	5.8
TCAS1-2021 [38]	5 CS	28-nm CMOS	420	186-200	7.3	0.46	14.3	45	0.31	NA	−2	1.5	1.1
RFIC-2021 [39]	1 CS	28-nm FD SOI	390	174-194	10.9	0.47	7.6	5.1	0.12	NA	−8	−3.7	0.7
This Work	10 FBA	45-nm CMOS SOI	310[§]	156-193.8	21.7	0.56	14	21.5	0.8	6.2	2.8	6	10[℘]
This Work	11 FBA	45-nm CMOS SOI	305[§]	157.4-194.2	NS*	0.57	20.4	19.25	0.87	6.2	4.4	6.1	NS*

[△] Spec values for other works were extracted from their text or otherwise estimated from the plots.
[◇] Topolo.: Topology, FB: feedback, CE: common-emitter, CS: common-source, and Cas.: cascade.
[†] Active area of the chip.
[⋆] FOM = P_{sat}[dBm] + Gain[dB] + $20\log(f_c/f_{\max})$+$10\log(\text{BW}_{\text{F}})$-$10\log(P_{\text{DC}})$
[§] $f_{\max}$ is reported for the chosen device and bias point.
[℘] P_{sat} measured at minimum power consumption is included from Fig. 21.
[*] Due to 4.2-dB ripple in the band, BW$_{\text{F}}$ is not calculated.

represent new performance benchmarks at these frequencies. The amplifiers achieve the highest BW as well as the highest gain/P_{dc} among all the CMOS counterparts at the G-band. Furthermore, Amp-A features extremely broadband matching (S_{11} and $S_{22} < -10$ dB) over entire 140–220-GHz band.

VII. CONCLUSION

The RFBA topology is introduced in this article and is studied in terms of power gain, NF, and operation BW. The RFBA cell achieves gain-boosting by using pre-embedding and embedding elements together. The cascaded RFBAs behave similarly to an artificial TL periodically loaded by negative resistors and hence are internally matched, eliminating the need for ISMNs that introduce dissipative loss and limit the BW. Further BW extension is achieved by cascading a CFBA and the RFBA, realizing a high gain over a broad BW. To validate the theoretical analyses, two amplifier prototypes were designed and fabricated in a 45-nm CMOS SOI process with $f_{\max}$ of 310 GHz. The first amplifier achieves an average gain of 12 dB over 156–193.8 GHz, whereas the second amplifier features an average gain of 17 dB at 157.4–194.2 GHz. Both designs provide gain up to $\approx 0.63 f_{\max}$ while achieving 6.2–13-dB NF and 6-dBm peak output power. To the authors' knowledge, the showcased amplifiers in this work accomplish the highest BW among the CMOS amplifiers operating at the G-band.

APPENDIX A
ADMITTANCE PARAMETERS OF THE EMBEDDED A2P

Assuming Y as the admittance parameters of the A2P in Fig. 1, it can be simply shown that

$$Y_R = \begin{bmatrix} Y_{22} & Y_{21} \\ Y_{12} & Y_{11} \end{bmatrix} \tag{14}$$

where the admittance matrices of the reversed device in Fig. 2 is expressed with Y_R. The Y-parameters of the network loading the shunt embedding represent the reversed device with series embedding and pre-embedding as

$$\begin{bmatrix} Y'_{22} & Y'_{21} \\ Y''_{12} & Y''_{11} \end{bmatrix} = \frac{\left[\begin{bmatrix} \frac{Y_{22}+jB_{\text{S}}}{\Delta Y} + jX_{\text{S}} & \frac{Y_{21}}{\Delta Y} - jX_{\text{S}} \\ \frac{Y_{12}}{\Delta Y} - jX_{\text{S}} & \frac{Y_{11}}{\Delta Y} + jX_{\text{S}} \end{bmatrix}\right]}{\Delta Z_{\text{S}}}. \tag{15}$$

Finally, the equivalent admittance parameters of the RFBA are derived as

$$Y_{\text{RFBA}}$$
$$= \frac{\left[\begin{bmatrix} \frac{Y_{22}+jB_{\text{S}}}{\Delta Y} + jX_{\text{S}} + jB_{\text{P}}\Delta Z_{\text{S}} & \frac{Y_{21}}{\Delta Y} - jX_{\text{S}} - jB_{\text{P}}\Delta Z_{\text{S}} \\ \frac{Y_{12}}{\Delta Y} - jX_{\text{S}} - jB_{\text{P}}\Delta Z_{\text{S}} & \frac{Y_{11}}{\Delta Y} + jX_{\text{S}} + jB_{\text{P}}\Delta Z_{\text{S}} \end{bmatrix}\right]}{\Delta Z_{\text{S}}} \tag{16}$$

where

$$\Delta Y = Y_{11} \cdot (Y_{22} + jB_S) - Y_{12} \cdot Y_{21} \tag{17a}$$

$$\Delta Z_S = \frac{1 + jX_S(Y_{11} + Y_{22} + Y_{12} + Y_{21} + jB_S)}{\Delta Y}. \tag{17b}$$

APPENDIX B
NOISE PARAMETERS OF THE EMBEDDED A2P

The corresponding noise parameters of the embedded A2P (R_n', G_u', and Y_c') in Fig. 5(b) are derived as

$$R_n' = R_n|D|^2|1 + AY_c|^2 + G_u|AD|^2 \tag{18}$$

$$Y_c' = \frac{D^*}{R_n'}\big(R_n(1 + A^*Y_c^*)(E + Y_c(B + AE))$$

$$+ G_u A^*(B + AE)\big) \tag{19}$$

$$G_u' = G_u|B + AE|^2 + R_n|Y_c(B + AE) + E|^2 - R_n'|Y_c'|^2 \tag{20}$$

where

$$A = jX_S\frac{Y_{22} + Y_{21}}{Y_{21} - jX_S\Delta Y} \tag{21a}$$

$$B = \frac{Y_{21}}{Y_{21} - jX_S\Delta Y} \tag{21b}$$

$$D = \frac{Y_{21} - jX_S\Delta Y}{Y_{21} - \Delta Y(jX_S + jB_P\Delta Z_S)} \tag{21c}$$

$$E = jB_P\frac{Y_{21} + Y_{11}}{Y_{21} - \Delta Y(jX_S + jB_P\Delta Z_S)}. \tag{21d}$$

The Y-parameters represent the admittance parameters of the A2P with the pre-embedding element.

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