# On the Origin of Holes During Polarization Reset in Floating Body Ferroelectric FETs Towards Improving Switching Efficiency

Zhouhang Jiang[1]*, Yi Xiao[2]*, Milind Weling[3], Halid Mulaosmanovic[4], Stefan Duenkel[4], Dominik Kleimaier[4], Steven Soss[4], Sven Beyer[4], Rajiv Joshi[5], Mohamed Mohamed[6], Scott Meninger[6], Xiao Gong[7], Vijaykrishnan Narayanan[2], and Kai Ni[1]
[1]University of Notre Dame; [2]Pennsylvania State University; [3]EMD Group; [4]GlobalFoundries Fab1 LLC & Co. KG; [5]IBM Thomas J. Watson Research Center; [6]MIT Lincoln Laboratory; [7]National University of Singapore
*Equal contribution; (email: zjiang3@nd.edu)

2024 IEEE International Electron Devices Meeting (IEDM) | 979-8-3503-6542-9/24/$31.00 ©2024 IEEE | DOI: 10.1109/IEDM50854.2024.10873452

***Abstract*— In this work, we performed a comprehensive combined experimental and modeling study on the polarization reset mechanisms of floating body (i.e., channel) ferroelectric FETs, an important class of device with growing interests due to added functionalities and improved reliabilities. Using fully-depleted silicon-on-insulator (FDSOI) FeFET as a classical example, we demonstrate that: 1) without hole generation mechanisms, floating body FeFETs during reset is simply a capacitor divider, with negligible ferroelectric voltage drop for switching; ii) Band-to-band-tunneling (BTBT) around gate-to-S/D overlap even with zero drain bias generates holes to facilitate the reset in FDSOI FeFET, though at a slower speed and hold the reset state; iii) With scaling, S/D inner fringe field can enable fast reset, thus offering a potential efficiency boost approach; iv) a compact FDSOI FeFET model is developed that can capture the BTBT effect and reproduce the observed behaviors; v) the reset mechanism is also validated in a NAND string composed of FDSOI FeFETs, demonstrating its relevant applications. These insights show the strategies in improving reset efficiency, i.e., enhanced BTBT and inner fringe field.**

## I. Introduction

$HfO_2$ based FeFET has been a competitive candidate for embedded nonvolatile memory regime owing to its energy efficiency, superior scalability and CMOS compatibility. Bulk FeFET has been heavily studied over the last decade and its polarization set and reset processes are very efficient as the electrons from S/D during set and holes from the body during reset can effectively screen the polarization (Fig.1(a)). However, many emerging FeFETs that can provide new functionalities (e.g., FDSOI FeFET), excellent reliability (e.g., back-end-of-line (BEOL) FeFET), or superior electrostatics (e.g., gate-all-around (GAA) FeFET) all have floating body, that is disconnected from hole reservoir. During polarization reset as demonstrated in Fig.1(b), the path of screening holes is cutoff from body which hinders the reset process. Therefore, it is important to look at other hole generation mechanisms and understand its role in the reset operation.

Typically, holes can be generated through either Shockley-Read-Hall (SRH) generation, band to band tunneling (BTBT) at gate-to-drain overlap (i.e., GIDL) or BTBT at junction sidewall (Fig.1(c)). In this work, to fully grasp the resetting process of floating body FeFETs and thereby enhance the switching efficiency, FDSOI FeFET is examined as a representative example. Understanding such mechanisms are critical for many applications as it directly impacts the available memory window that can be leveraged. As an illustration, in the flash-based vertical NAND array, where the string channel is disconnected from p-type substrate, the erase operation requires hole generation through the gate-induced-drain-leakage (GIDL) at the select transistors. As shown in Fig.2(a), the erase of the traditional NAND flash requires extremely high drain bias (20V) at both bit line (BL) and source line (SL) to enable a large enough GIDL current to erase the whole block. Recently, ferroelectric has shown great promise in vertical NAND application as it can enable a large memory window at lower operation voltages and improved speed compared with flash [1], it is important to understand the polarization reset mechanisms in FeFETs with floating body. In this work, through comprehensive experimental and modeling studies, we show that it is possible to generate efficient holes through the BTBT at low drain bias, reducing the concern over the reliability and power consumption. Fig.2(b) illustrates that only a small drain bias is needed for erasing in a floating body FeFET.

## II. Device Under Test

In this work, 28nm bulk FeFET [1] and 22nm FDSOI FeFET [2] are utilized. TEMs are shown in Fig.3(a)/(b) for bulk and FDSOI FeFETs, respectively. As an illustrative example of floating body FeFET, the FDSOI FeFET is adopted and compared side by side with bulk FeFET, in the hope of revealing the physical mechanisms. Under ±4V, 10$\mu$s (solid line)/1$\mu$s (dashed line) write pulses, the $I_D$-$V_G$ characteristics of both bulk and FDSOI FeFETs with W/L=0.5$\mu$m/0.5$\mu$m are shown in Fig.3(c)/(d), respectively. It shows that the low threshold voltage (LVT) state for both devices are similar while the high threshold voltage (HVT) state shows distinctive behavior. It shows that with 1$\mu$s pulse width, full polarization switching is not possible. This will be further studied later.

During the positive set operation, both bulk and FDSOI FeFETs have the same response in the channel, where the electrons from both source/drain are supplied to the channel to screen the polarization, as shown in Fig.4(a)/(b). Since the set process for bulk and FDSOI can benefit from electron supply from S/D, therefore, both of them can set even below 100ns at 4V as shown in Fig.4(c)/(d). By write FeFETs into HVT state, then by applying +4V and +2V pulse with different pulse

width, the polarization switching happens for both bulk/FDSOI FeFETs roughly at the same pulse width as demonstrated in Fig.4(e)/(f). Moreover, the retention of LVT is shown in Fig.4(g)/(h) for bulk/FDSOI FeFETs, respectively. These indicates the electrons are stable and could hold the polarization for a long retention time without significant loss.

## III. Reset in Floating Body FeFETs

During reset in a FDSOI FeFET, where no direct hole supply from the body is available, the whole stack can be modeled as a simple capacitor divider (Fig.5(a)), where all capacitors are connected in series. Note that this could be true even for p-doped substrate with medium doping. The discrepancy between bulk and FDSOI FeFET during reset can be observed in the transient simulation shown in Fig.5(b), where the voltage drops in ferroelectric layer, $V_{FE}$, in the FDSOI device is much smaller than the bulk one. The capacitor divider picture of the stack is also validated by the excellent match between the TCAD and SPICE simulations as demonstrated in Fig.5(c), using the same set of parameters. With no BTBT accounted here, these results raise the question regarding whether floating body FeFETs can be reset at all.

To answer that, Fig.6(a)/(b) demonstrate the reset dynamics of both bulk and FDSOI FeFETs. All the devices are initialized to the LVT state for study. From the switching dynamics, two observations can be drawn: 1) FDSOI FeFET could fully reset as the bulk FeFET, though the basic electrostatics say otherwise; 2) FDSOI FeFET reset takes a longer time than the bulk FeFET at higher reset voltages (Fig.6(c)) while at a similar speed when the reset voltage is small. These suggest a slow hole generation mechanism that can enable full reset in FDSOI FeFETs. Also as shown in Fig.6(d), given a long reset pulse width namely 10ms, both bulk and FDSOI FeFETs could switch to HVT at low voltage. Besides, the HVT retention of bulk/FDSOI FeFET is investigated as illustrated in Fig.6(e)/(f), respectively. By increasing the write pulse width from 1$\mu$s to 1ms, the HVT state in bulk FeFETs becomes more stable. Besides, the HVT state is also stable, confirming the FDSOI FeFET could hold generated holes.

## IV. Evidence of BTBT

To explain the two observations, first the gate-to-channel capacitance, i.e., $C_{GC}$-$V_G$, is measured and shown in Fig.7(a)/(b) for bulk/FDSOI FeFETs respectively. It clearly shows the signature of electron-hole pair generation in FDSOI FeFET at negative gate voltages, even at frequency of 100kHz. This means that with 10$\mu$s response time, hole generation is already happening, thus confirming what is observed in the switching dynamics. Next the DC $I_D$-$V_G$ curves are also measured, covering a wide range of drain biases. Interestingly, at small drain bias (e.g., 5mV), a strong hole generation as leakage current is present in FDSOI FeFETs as shown in Fig.7(c)/(d). This indicates that the drain bias is not the main driver for the hole generation, but the gate bias. Then band diagrams along the channel extracted from TCAD simulations (Fig.7(e)/(f)) confirm the strong channel to S/D band bending in FDSOI FeFET because of almost no $V_{FE}$ drop during reset process, thus leading to the strong BTBT generation. Then the TCAD simulations of reset process with and without BTBT model activated further confirm that the polarization could switch in 10$\mu$s (Fig.7(g)) which is consistent with our experimental results. Last, the generation rate of BTBT as demonstrated in Fig.7(h) shows that it is almost concentrated at the gate-to-drain junctions.

The reset dynamics are also studied for scaled short channel bulk/ FDSOI FeFETs as demonstrated in Fig.8(a)/(b), respectively. Interestingly both of these two devices could reset quickly (Fig.8(c)), suggesting a promising strategy in improving switching efficiency, i.e., $L_G$ scaling. This speed enhancement with scaling originates from the increased effective $V_{FE}$ in shorter device as the inner S/D fringe field penetrates a larger portion of the $L_G$ as illustrated in Fig.8(d). The vertical $E_{FE}$ also confirms the scaling does help the FDSOI FeFET over the reset process.

## V. Compact Model

Given the understanding of the reset process, we then augment our previously developed compact model for FDSOI FeFET [3] with an additional BTBT module. The model is composed of the FDSOI baseline, leveraging the Leti-UTSOI model [4] as well as the multi-domain nucleation-limited FE model [5]. The BTBT model calculates the lateral field and the generated hole density as shown in Fig.9(c). Surface potential and lateral electric field show excellent match with TCAD (Fig.9(d)/(e)). Fig.9(f)/(g) demonstrates the transient waveforms for pulse width of 100ns and 10$\mu$s, respectively. The model is able to capture that with the BTBT module introduced, a full reset is achieved for 10$\mu$s. While at 100ns, not much polarization switching happens. The $I_D$-$V_G$ characteristics are also shown in Fig.9(h)/(i). Again, confirms the delayed reset process due to the slow BTBT rate.

## VI. NAND String Operation

With such an understanding on the polarization reset mechanisms, we demonstrate that it can be applied in NAND FeFET array. With a string composed of 3 FDSOI FeFETs (Fig.10(a)), the center FeFET can be reset to a degree as the single device, thus confirming the possibility as demonstrated in Fig.10(c)-(f). Comparing the flash based NAND string that demands a high drain bias to complete the block erase operation, namely around 20V, FeFET could potentially improves the reliability and lowers the power consumption.

## VII. Conclusion

We have performed comprehensive experimental and modeling efforts in clarifying the polarization reset mechanisms in an important class of floating body FeFETs. We have shown that in Si channel floating body device, the BTBT effect can contribute holes at a slow speed. With gate length scaling, the S/D inner fringe field also helps device reset. Additionally, a NAND string composed of FDSOI FeFETs is shown to be able to full reset as the single FDSOI FeFET.

**Acknowledgement:** This work was primarily supported by SUPREME and PRSIM, two of the SRC/DARPA JUMP 2.0 centers, NSF 2347024 and 2312884, and the United States Air Force under Air Force Contract no.FA8702-15-D-0001. Any opinions, findings, conclusions, or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the United States Air Force. The TCAD modeling was supported by U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences Energy Frontier Research Centers program under Award Number DESC0021118. It is also funded by the Federal Ministry for Economics and Energy (BMWi) and by the State of Saxony in the framework "Important Project of Common European Interest (IPCEI)".

**References**: [1] S. Yoon et al., VLSI 2023; [2] M. Trentzsch et al., IEDM 2016; [3] S. Dünkel et al., IEDM 2017; [4] Z. Jiang et al., VLSI 2022; [5] T. Poiroux et al., TED 2015; [6] S. Deng et al., VLSI 2020;

## Motivation: Mechanisms of Polarization Reset in Floating Body FeFETs Are not Well Understood

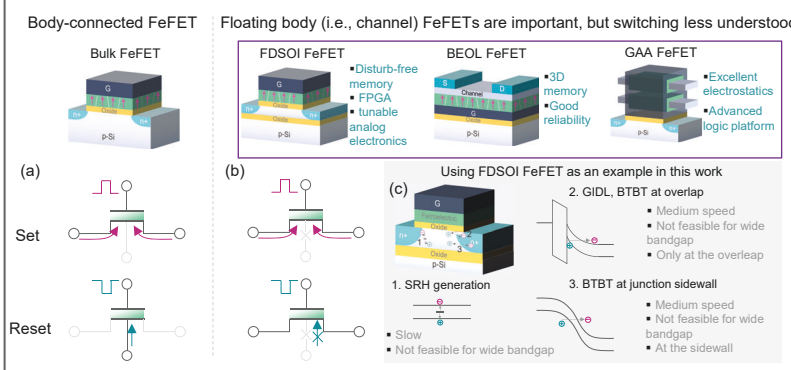


Fig.1. (a) With hole supply from p-type body, bulk FeFET can reset the polarization efficiently. (b) However, many emerging important FeFETs have floating body without hole supply, making reset process inefficient. (c) Using FDSOI FeFET as an example, different hole generation mechanisms need to be examined.

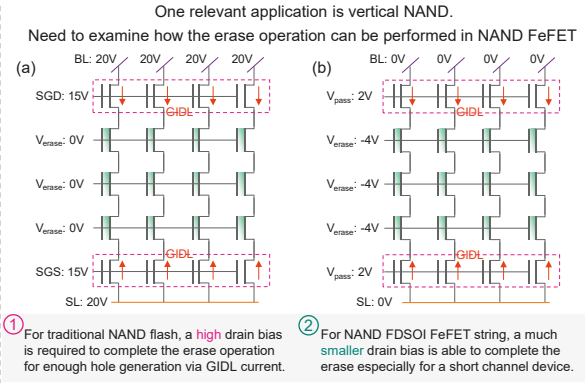


Fig.2. (a) conventional 3D NAND flash requires high drain bias to erase the block. While (b) FDSOI FeFET NAND string could work with a small drain voltage to erase.

## Bulk and FDSOI FeFETs for Study

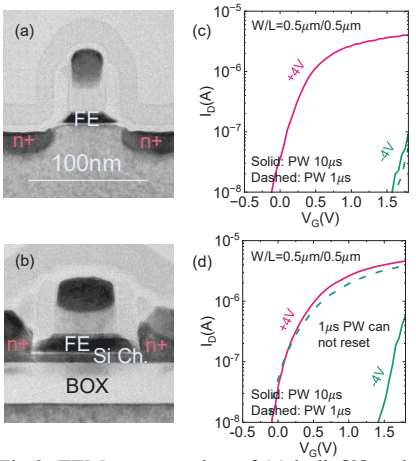


Fig.3. TEM cross-section of (a) bulk [2] and (b) FDSOI [3] FeFET with (c)/(d) corresponding $I_D$-$V_G$ characteristics programmed with +/-4V and 10$\mu$s and 1$\mu$s.

## Polarization Set Processes Are Efficient in Both Bulk and FDSOI FeFET

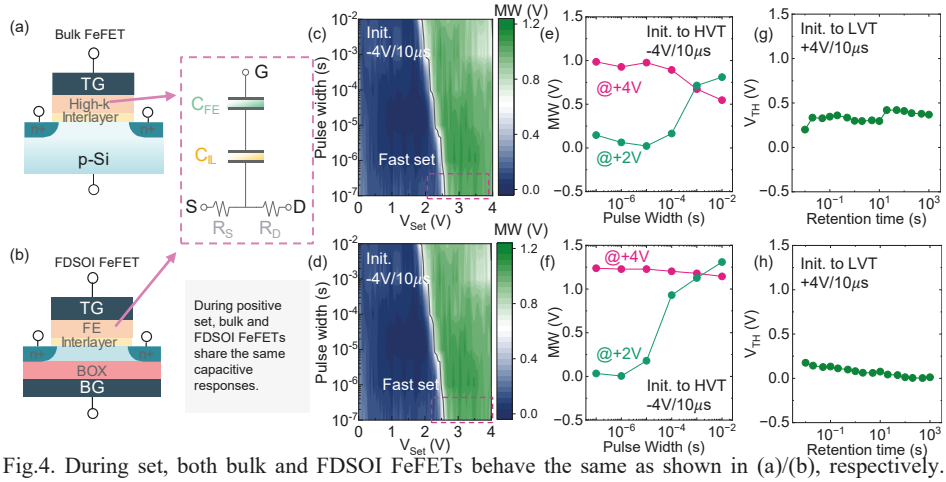


Fig.4. During set, both bulk and FDSOI FeFETs behave the same as shown in (a)/(b), respectively. (c)/(d) Fast set of polarization at high voltage is seen for both bulk and FDSOI FeFET. For initialization to LVT state, MW vs. PW is demonstrated in (e)/(f) for bulk/FDSOI FeFET. Retention of LVT state is seen in (g)/(h) for bulk/FDSOI FeFET. All these suggest the same polarization set process.

## Electrostatics in FDSOI FeFET

## Basic Electrostatics Can Not Explain the Measured Reset Dynamics in FDSOI FeFET

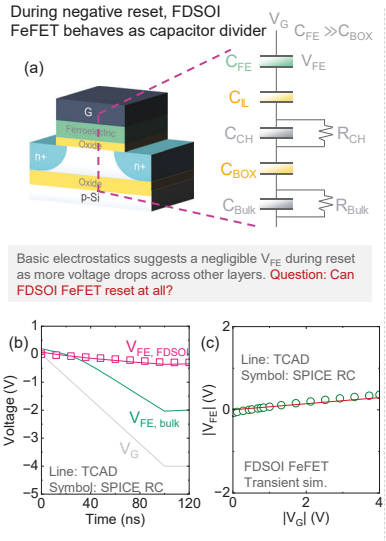


Fig.5. (a) FDSOI FeFET behaves as a capacitor divider. (b) Comparing with bulk, $V_{FE}$ is negligible in FDSOI. (c) The capacitor divider physical picture is also verified with TCAD.

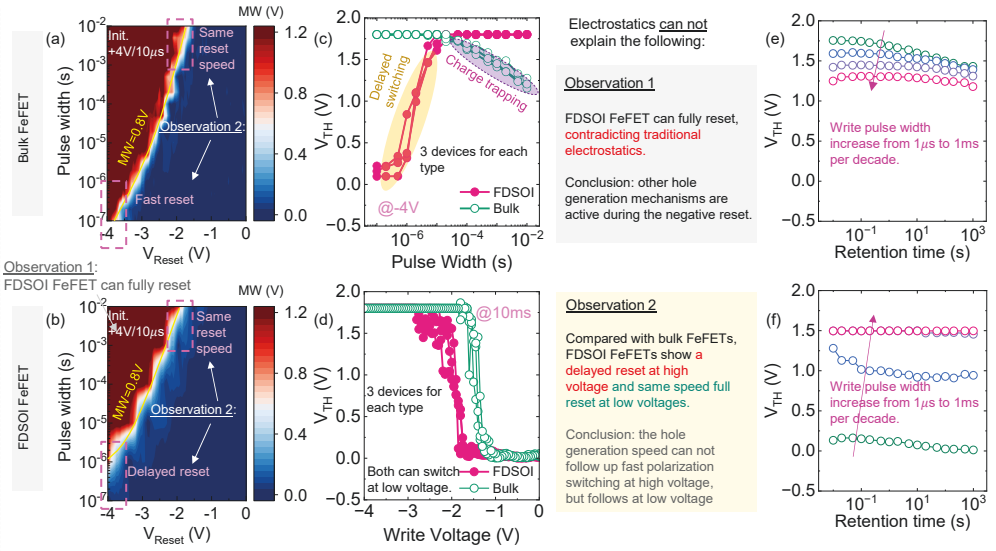


Fig.6. Reset dynamics of (a) bulk and (b) FDSOI FeFETs. (c) Slow/fast reset is seen for FDSOI/bulk FeFETs at high reset voltage. It still shows a full reset, though slower. At low voltages, two devices have similar reset speed. (d) At 10ms pulse width, both bulk and FDSOI FeFET could fully reset. (e)/(f) The retention of bulk and FDSOI FeFETs initialized to the HVT state, respectively. These results suggest the existence of slow hole generation mechanism that helps polarization switching in FDSOI FeFET.

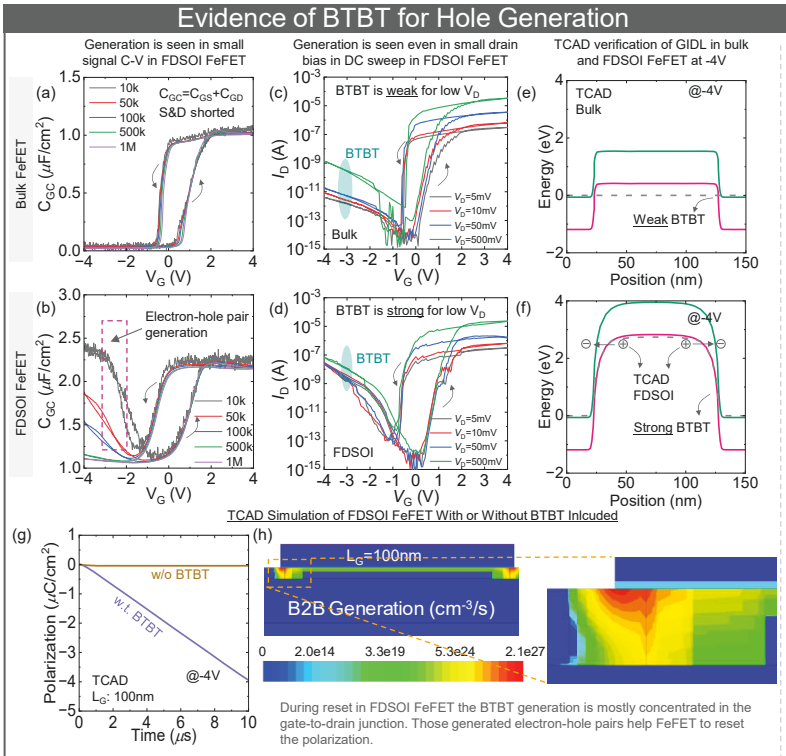


Fig.7. (a)/(b) $C_{GC}$-$V_G$ for bulk and FDSOI FeFET, respectively. Strong electron-hole generation is seen in FDSOI FeFET even at 100kHz. (c)/(d) The same BTBT is present in $I_D$-$V_G$ for both bulk/FDSOI FeFETs. Even at 5mV drain bias, BTBT is seen in FDSOI FeFET, suggesting it is driven by negative gate bias. (e)/(f) The band diagrams during reset for bulk/FDSOI FeFET. (g) depicts the $P_{FE}$ resets due to BTBT. (h) demonstrates the generation rate of BTBT for $L_G$=100nm.

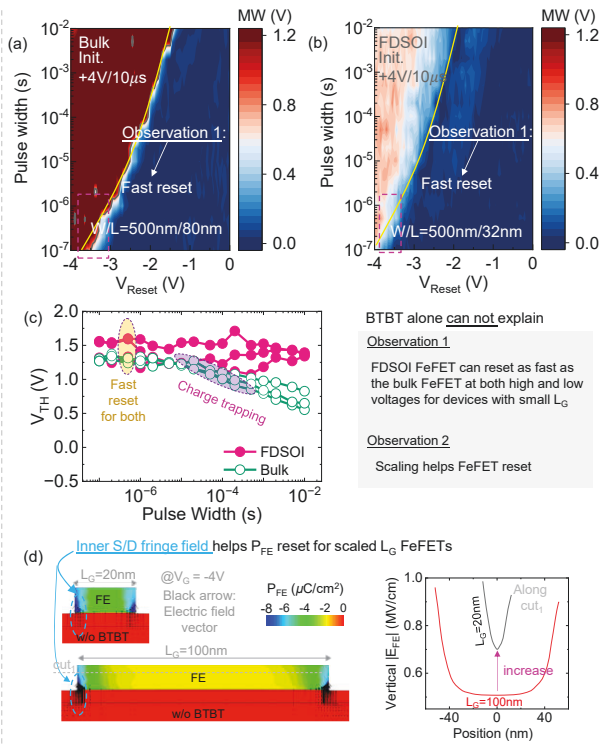


Fig.8. (a)/(b) Reset dynamics of scaled bulk/FDSOI FeFETs. (c) Reset in scaled FDSOI FeFET is as fast as bulk FeFET. (d) This is because S/D inner fringe field enhances the FE field close to the S/D, which can help reset $P_{FE}$ for scaled devices. Thus fast $P_{FE}$ reset is seen. Thus scaling could improve reset efficiency.

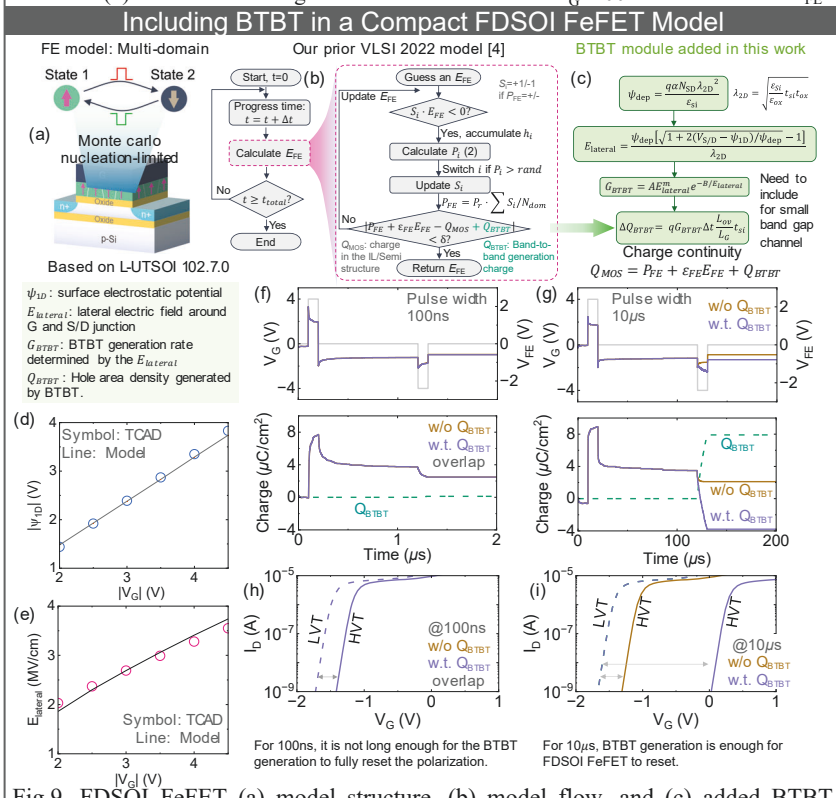


Fig.9. FDSOI FeFET (a) model structure, (b) model flow, and (c) added BTBT module. (d) and (e) show that the model captures the surface electrostatic potential and lateral electric field around gate to S/D junction. (f)/(g) Simulated transient waveforms for 100ns/10$\mu$s write pulse. (h)/(i) The corresponding $I_D$-$V_G$ characteristics for 100ns/10$\mu$s matches the experiments in Fig.6(b).

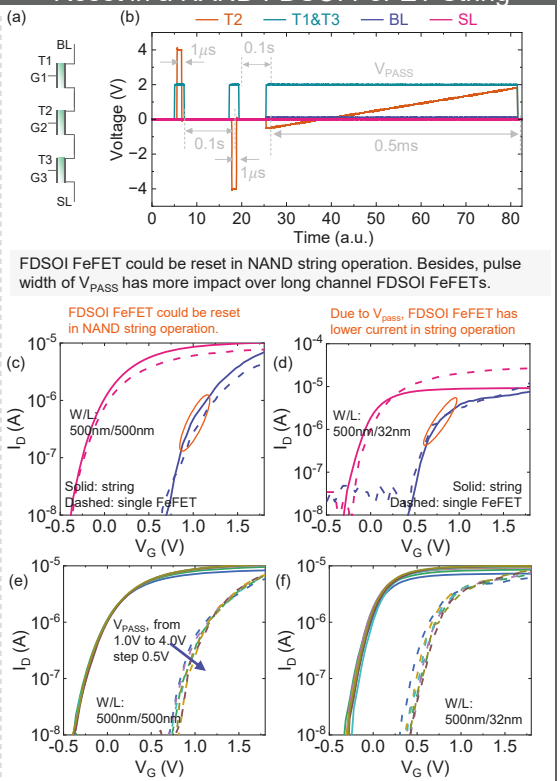


Fig.10. (a)/(b) shows the schematic representation of FeFET NAND string and transient waveform. (c)/(d) FeFETs in a string can reset as a single device. (e)/(f) The impact of $V_{PASS}$ amplitude over string operation.