HermEIS: A Parallel Multichannel Approach to Rapid Spectral Characterization of Neural MEAs

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Abstract—**The promise of increasing channel counts in high density ($> 10^4$) neural Microelectrode Arrays (MEAs) for high resolution recording comes with the curse of developing faster characterization strategies for concurrent acquisition of multi-channel electrode integrities over a wide frequency spectrum. To circumvent the latency associated with the current multiplexed technique for impedance acquisition, it is common practice to resort to the single frequency impedance measurement (i.e. $Z_{1\text{kHz}}$). This, however, does not offer sufficient spectral impedance information crucial for determining the capacity of electrodes at withstanding slow and fast-changing stimuli and recordings. In this work, we present *HermEIS*, a novel approach that leverages single cycle in-phase and quadrature signal integrations for reducing the massive data throughput characteristic of such high density acquisition systems. As an initial proof-of-concept, we demonstrate over 6 decades of impedance bandwidth ($5 \times 10^{-2} - 5 \times 10^4$ Hz) in a parallel 4-channel potentiostatic setup composed of a custom PCB with off-the-shelf electronics working in tandem with an FPGA.**

Index Terms—**neural interfaces, brain-machine interfaces, electrode characterization, impedance spectroscopy, bioinstrumentation**

I. Introduction

Ever since Santiago Ramón y Cajal's *neuron doctrine*, which posited the nervous system as a conglomeration of discrete neurons, scientists and engineers continue to push the resolution of neural microelectrode arrays (MEAs) beyond single neuron dimensions (i.e. a few microns). Similar to CMOS imagers, higher electrode resolution allows us to perceive finer electrophysiology. Although there may exist other noninvasive interfacing modalities, direct electrochemical interfacing offers better temporal contrast to catch the rapidly propagating neural action potential. Finer electrode diameter and pitch are often accompanied with high MEA channel counts, which are advantageous in capturing the high-dimensional neural/ cortical processing of sensory information. Unfortunately, an increased channel density in a recording setup means that the digital processor has to drink from a fire hose of biosignals. Faster communication and processing are thus needed to enable rapid closed-loop control. The situation is much dire in spectral electrode characterization methods, such as Electrochemical Impedance Spectroscopy (EIS), needed to guarantee electrode integrity. Neural MEAs interfacing with tissue form a Helmhotz double layer, i.e. a capacitive double layer formed by charge redistribution induced by the electrode-electrolyte complex. Ideally, charge must travel from electrode to tissue

(stimulation) and vice versa (recording) in either a capacitive non-faradaic manner or a reversible faradaic (redox) manner. This process is, however, limited by corrosion and glial cells formed over time. The capacitive nature of electrode/interface impedance requires that an investigator not only resolve for space and time but also for frequency. State-of-the-art MEAs have $> 10^4$ channel counts, e.g., Neuropixels 2.0 $(10, 240)$ [1], MaxOne/ MaxTwo (Maxwell Biosystems) $(26, 400)$ [2] and Dragas *et al.* [3] $(59, 760)$. It is common practice to circumvent the prolonged impedance acquisition associated with such high-density MEAs with mere measurements at 1 kHz, $Z_{1\text{kHz}}$. While this may offer coarse interface information, the nuances that wide spectral impedance offer is crucial to designing durable electrodes.

To obtain such rich spectral information, one may choose to apply several cycles per test frequency sufficient to resolve the magnitude and phase information by Fourier transformation. This is time-consuming. More so, present characterization systems (e.g. Gamry Instruments) handle multichannel characterization by multiplexing a cumbersome rack of potentiostats and thereby extends latency in data acquisition. In this study, we present *HermEIS*, a rapid EIS chatacterization approach (see Fig. 1A) based on in-phase and quadrature integrations where a single frequency cycle suffices. We adopted a parallel multichannel acquisition in a Field Programmable Gate Array (FPGA), limited only by universal serial bus (USB) transmission to the host PC. As a proof-of-concept, our demonstration involves an 4-channel Analog Front-End (AFE) implemented in a custom PCB working in tandem with the FPGA. The concepts presented here are however scalable to large-scale neural MEAs especially with the ever increasing speeds (> 10 Gbit/s) in PC-peripheral communication (e.g. USB 3x–4.x, PCIe 4.x–5x).

In a potentiostatic setup (i.e. voltage in, current out), EIS involves the measurement of impedance magnitude and phase responses via the application of sinusoidal potentials with frequencies within $10^{-3} - 10^5$ Hz and root-mean-square (rms) magnitudes typically below 50 mV to ensure current-voltage linearity [4], [5]; as such interfacial impedance are nonlinear in a large signal sense. The broad frequency spectrum mentioned above allows for a proper assessment of the dynamic range of electrode response. This is particularly important in guaranteeing the electrodes can capture the slowly changing subthreshold neural dynamics as well as the sharp neural depolarizations. The various frequency regimes of an EIS measurement indicate the quality of the electrode-electrolyte interface. While impedance response can be fitted to a number of equivalent circuits of the electrolyte-electrolyte interface,

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the Randles circuit is perhaps among the simplest yet plausible [6], [7]. It comprises the double layer capacitance, C_{dl} in parallel with Faradaic impedance, Z_F (composed of the redox kinetics resistance in series with the Warburg impedance, which accounts for the mass transport of the redox species), all in series with the uncompensated solution resistance, R_U. At both extremes, the interface impedance is dominated by R_U and $\Re\{Z_W\}$ at low frequency, and dominated by the reactances of C_{dl} and Z_F at high frequencies. Thus, an impedance response in the form of Nyquist or Bode plots offer a finer insight on the state of electrodes when placed *in vivo* or *in vitro*. This work shares similarities with lock-in amplifier approach, in the sense that only a single period is sufficient. The difference, however, is in the sole-dependence on quarter cycle integrations here without needing any form of modulation, while lock-in amplifiers and other classical single cycle fourier techniques require a multiplication with a reference square wave of unity amplitude and cosine/sine modulators respectively [8].

II. THEORY AND APPROACH

In a 3-electrode potentiostat setup, that is, the reference electrode (REF), counter electrode (CE), and working electrode (WE), the impedance $Z(\omega_i)$ is a function of the sinusoidal voltage, $V(\omega_i, t)$ applied on WE via REF and the WE current, $I(\omega_i, t)$ where ω_i is a user-defined frequency. Assuming linear time-invariance holds, the impedance response will either modulate amplitude V_1 or phase ϕ only. As such consider that $V(\omega_i, t)$ and $R_{out}I(\omega_i, t)$ are of the form,

$$V(\omega_i, t) = V_0 + V_1 \sin(\omega_i t + \phi) \quad (1)$$

where V_0 is an applied DC offset to set the operating point on the nonlinear IV curve and R_{out} is a suitably chosen output resistance to convert $I(\omega_i, t)$ into a voltage to match voltage-mode A/D conversion used for the reference voltage, $V^{(\mathrm{ref})}$. The goal is to decipher phase and magnitude change information and there are a number of ways to obtained that. The proposed method adopts the I/Q approach not by the typical correlation of the WE output with a separately generated complimentary sinusoid pair, but rather via appropriate quarter cycle signal integrations shown in eqs.2,3 over a period, $T = 2\pi/\omega_i$.

$$\mathcal{I}(\omega_i) = \int_0^{T/2} V(\omega_i, t)dt - \frac{1}{2}\int_0^T V(\omega_i, t)dt = \frac{2V_1}{\omega_i}\cos\phi \quad (2)$$

$$\mathcal{Q}(\omega_i) = \int_{T/4}^{3T/4} V(\omega_i, t)dt - \frac{1}{2}\int_0^T V(\omega_i, t)dt = -\frac{2V_1}{\omega_i}\sin\phi \quad (3)$$

Let $\mathcal{X}(\omega_i)$ be an intermediary signal such that;

$$\mathcal{X}(\omega_i) = \mathcal{I}(\omega_i) - j\mathcal{Q}(\omega_i) \quad (4)$$

Note that $\mathcal{X}^{(\mathrm{ref})}(\omega_i)$ takes the form $\mathcal{X}(\omega_i)$, while $\mathcal{X}^{(\mathrm{ch}_j)}(\omega_i)$ takes the form $-\mathcal{X}(\omega_i)$ to account for negative gain in the WE current readout amplification stage. The impedance response of a WE, ch_j, in an MEA of j channels can then be;

$$|Z^{(\mathrm{ch}j)}(\omega_i)| = R_{out} \cdot \left|\frac{\mathcal{X}^{(\mathrm{ref})}(\omega_i)}{\mathcal{X}^{(\mathrm{ch}j)}(\omega_i)}\right| \quad (5)$$

$$\angle Z^{(\mathrm{ch}j)}(\omega_i) = \angle\mathcal{X}^{(\mathrm{ref})}(\omega_i) - \angle\mathcal{X}^{(\mathrm{ch}j)}(\omega_i) \quad (6)$$

A discrete-time (DT) signal perspective on the above-mentioned is necessary for a digital implementation. In this case, the user-defined frequency Ω_i is posed as a function of the maximum ADC sampling frequency, f_s in the form $\Omega_i = 2\pi f_i/f_s$, By sampling theorem, $\Omega_i \in (0, \pi)$, thus $|f_i/f_s| < 0.5$ and $f_{max} = f_s/2$. The DT version of eq.1 shown in eq.7 is generated by direct digital synthesis (DDS) based on a clock frequency $f_{dds,clk}$.

$$V[\Omega_i, n] = V_0 + V_1 \sin(\Omega_i n + \phi) \quad (7)$$

To ensure periodicity and minimize approximation errors in the quarter cycle integrations, an adaptive sampling frequency, f_s' as a function of the f_i is adopted and is defined over $f_i \in [f_{max}^{-1}, f_{max}]$. To get the most out of a given f_s, we adopted an adaptive sampling:

$$f_s'(f_i) = \begin{cases} \left\lfloor \frac{f_s}{f_i} \right\rfloor \cdot f_i & \text{if } \left\lfloor \frac{f_s}{f_i} \right\rfloor \bmod 4 = 0 \\ \left\lfloor \frac{f_s}{4f_i} \right\rfloor \cdot 4f_i & \text{elsewhere} \end{cases} \quad (8)$$

$$\forall f_i \in (0, \lfloor \tfrac{f_s}{4} \rfloor]]$$

where $\lfloor \cdot \rfloor$ is flooring operation. Another round of approximation (shown in eq.9) is performed to ensure that f_s' is an integer multiple of f_{clk}. k is the clock divider for achieving this.

$$k = \left\lfloor \frac{f_{clk}}{f_s'} \right\rfloor \quad (9)$$

This rounding operation ($\lfloor \cdot \rfloor$) introduces a marginal frequency, f_ϵ shift that is kept negligible by ensuring that $f_{clk} >> f_s'$. The effective sampling frequency, $\hat{f}_s$ is thus given by:

$$\hat{f}_s = kf_{clk} \pm \overbrace{\frac{f_s'}{f_{clk}}}^{f_\epsilon} \quad (10)$$

At this point, we adopt $\hat{\Omega}_i$ instead of Ω_i, where $\hat{\Omega}_i = 2\pi f_i/\hat{f}_s$. DT equivalents of eqs.2,3 with sampling period, $\Delta t_s = \hat{f}_s^{-1}$ and discrete time, n are shown in eqs.11,12 respectively.

$$\mathcal{I}[\hat{\Omega}_i] = \left(\sum_0^{T/2} V[\hat{\Omega}, n] - \frac{1}{2}\sum_0^T V[\hat{\Omega}_i, n]\right) \cdot \Delta t_s \quad (11)$$

$$\mathcal{Q}[\hat{\Omega}_i] = \left(\sum_{T/4}^{3T/4} V[\hat{\Omega}_i, n] - \frac{1}{2}\sum_0^T V[\hat{\Omega}_i, n]\right) \cdot \Delta t_s \quad (12)$$

III. IMPLEMENTATION

We implemented the above approach in an Opal Kelly (OK) XEM6310-LX150 FPGA working in tandem with an $4 + 1$-channel (i.e., 4 WEs and a REF) AFE implemented in a custom PCB with off-the-shelf electronics. The system is accompanied by a software controller in a form of python code with the OK Frontpanel API support. This allows for user-defined hardware initialization along with input/output (IO) data stream from the FPGA. The AFE was, however, designed for up to 8 channels, but only 5 were used based on maximum slice utilization in the FPGA (run at $f_{clk} = 50\mathrm{MHz}$ to meet timing).
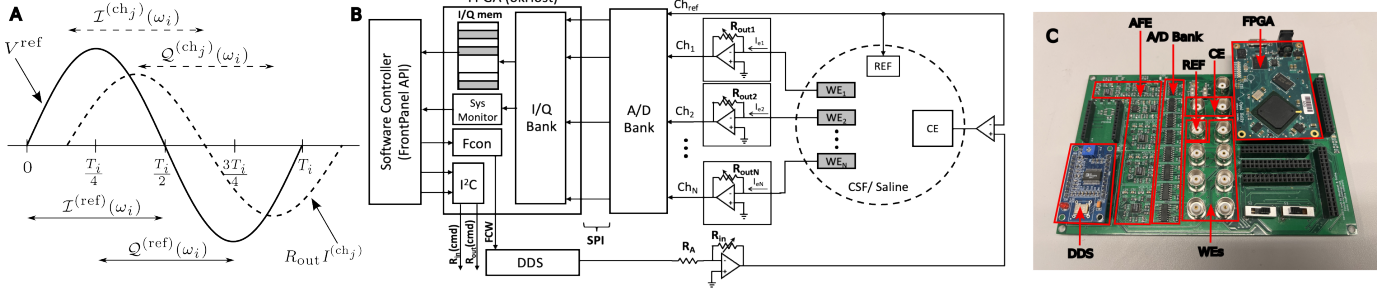
Fig. 1. **A**: An intuitive depiction of the integrative intervals yielding I/Q pairs for the reference and WE channels, both are subsequently used to obtain WE impedances. **B**: An overview of the hardware setup that combines Register Transfer Logic in an FPGA and analog front circuitry intended for multichannel *in vivo/ in vitro* measurements in a custom PCB shown in **C**.

A. Analog Front-End (AFE)

In our multichannel setup shown in Fig. 1B, all WEs share a REF and a CE. We implemented the 8-channel potentiostat using $2+8$ opAmp configuration, i.e., 2 opAmps are designated for the DC offset addition and setting V^{ref} respectively, and 8 opAmps (one per channel) for conveying the output currents. 3 LTC6082 (Analog Devices) Quad opAmp IC sufficed for this. The opamp supplies, i.e. $(V_{dd}, V_{ss}) = (3.3, -3)$V, come from an FPGA output and LTC1938-3 (Analog Devices) charge-pump inverter respectively. We used the 8 10-bit SAR MCP3008 (Microchip Technology) ADCs that allows a configurable sampling rate of up to 200 ksps sufficient for up to 50 kHz impedance characterization. Each ADC comes with 8 single-ended channels. For each ADC, we connected channel-0 of ADC_j to ch_j WE and populated the other ADC channels with the remaining WE channels in a ring manner. As such, parallel acquisition from all WEs is possible by broadcasting a single channel address to all ADCs. Alternatively, a pseudo-parallel acquisition of all 8 channels is possible with one ADC by multiplexing the channel addresses. However, this comes with a reduced sampling rate at $1/8$ factor. More so, temporal shifts in sequential sampling for this case must be accounted for. A combination of the parallel and pseudo-parallel modes stand to offer streaming from much higher channel counts. However, a commensurately high sampling rate is required. Here, we focus on the parallel mode and reserve the other mode for future study. Single-ended ADC inputs were used. This required elevating the measured potentials well above ground to allow the ADC to catch the full signal swing. An offset of $V_{dd}/2 \approx 1.65$V was applied here. We used the AD9850 (Analog Devices) DDS module for reference signal generation. This module comes with a 42 MHz low-pass, 5-pole elliptical filter at its DAC output and it is capable of up to 40 MHz output in the form $V^{\mathrm{ref(i)}} = 0.5 + 0.5\sin(2\pi f_i t)$. Alternatively, a numerically controlled oscillator can be synthesized in an FPGA with a sine Look-Up Table (LUT) along with an appropriate output digital-to-analog converter (DAC) and low-pass filter (LPF) if tighter system integration is desired. $V_0 = 0.5$V of $V^{\mathrm{ref(i)}}$ is set to 0 through an opamp-based inverting adder with an appropriate offset. The final reference voltage $V^{\mathrm{ref(o)}}$ can be amplitude modulated via a tunable R_{in} in the same amplification stage defined by $V^{\mathrm{ref(o)}} = -(R_{\mathrm{in}}/R_{\mathrm{A}})V^{\mathrm{ref(i)}}$ where $R_A = 100k\Omega$.

B. FPGA Implementation and Software Controller

For every f_i specified via an M-bit frequency control word (FCW) m based on a DDS clock, $f_{dds,clk} = 100$ MHz (given in Eq.13), the FPGA computes the appropriate $\hat{f}_s$ and retrieves a cycle-long stream of 10-bit sampled data via the serial peripheral interface (SPI) protocol at k count intervals.

$$m = \frac{2^M f_i}{f_{dds,clk}} \quad (13)$$

To minimize duplicate integrations, we express eq.11,12 in terms of quarter cycle integrations S_j as shown in eq. 15,16.

$$S_j = -\frac{r_j X_{\alpha,j}}{4m} + \sum_{n=\lfloor \frac{jT}{4} \rfloor}^{\lfloor \frac{(j+1)T}{4} \rfloor} X[n] - \frac{(4m - r_{j+1})X_{\alpha,j+1}}{4m} \quad (14)$$

where $r_j = j\frac{2^M \hat{f}_s}{f_{dds_clk}} \bmod 4m$, X is the 10-bit ADC data, $X_{\alpha,j} = \lfloor \frac{(j+1)T}{4} \rfloor$ and $j \in \{0,1,2,3\}$

$$\mathcal{I}[\hat{\Omega}] = (S_0 + S_1 - (S_2 + S_3))/2\hat{f}_s \quad (15)$$

$$\mathcal{Q}[\hat{\Omega}] = (S_1 + S_2 - (S_0 + S_3))/2\hat{f}_s \quad (16)$$

We compute $(\mathcal{I}, \mathcal{Q}) \cdot \hat{f}_s$ equivalent in the FPGA and defer the determination of magnitude and phase responses to the software controller which queries for this I/Q pair. We use 7-bit digital rheostats (MCP40D17, Microchip Technology) to for setting $R_{\mathrm{in}}, R_{\mathrm{out},j}$ defined by;

$$R_{\{\mathrm{in,out}\}} = R_{min} + (R_{max}N_{\mathrm{(in,out)}})/127 \quad (17)$$

where is $N \in [0, 127]$ is the 7-bit a user-defined command word set in the software controller and delivered by the FPGA via I^{2}C, and $R_{max} = 50k\Omega$ and $R_{min} = 0.002R_{max}$ (typical value reported in datasheet) being the maximum and minimum resistances respectively. This ensured the flexibility of finding appropriate resistor values that promote high SNR without clipping signals. We used a 32-bit signed fixed-point precision to achieve a 6-decade impedance spectra ($5 \times 10^{-2} - 5 \times 10^4$ Hz) computation, limited at the lower bound by DDS resolution ($f_{dds,clk}/2^{31}$) and the upper bound by sampling limit of $f_s/4$. A 32×10-bit buffer is instantiated in the FPGA for temporarily staging the 5 I/Q pairs. With the help of the software controller (in the form of a jupyter notebook) and a programmed FPGA, impedance acquisition process proceeds
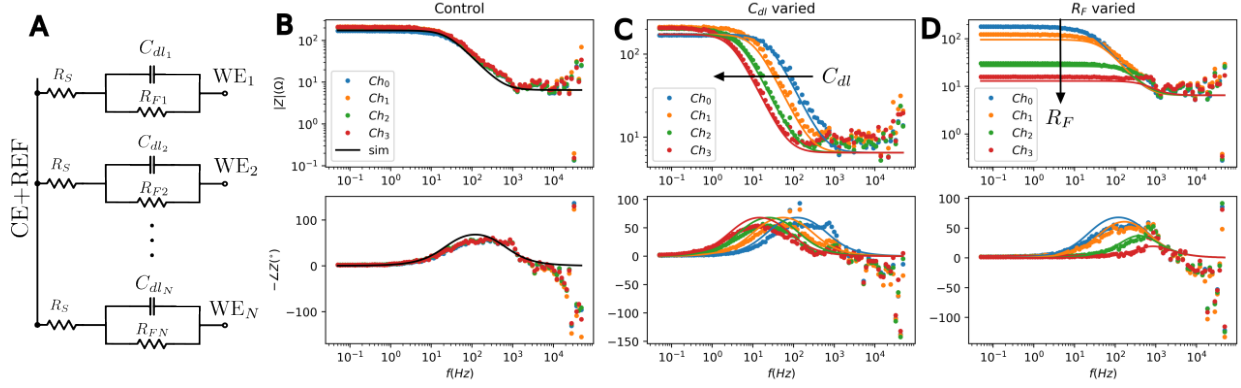
Fig. 2. Bode plots from parallel 4-channel impedance acquisition in 3 experimental protocols along with their simulated ground truth in solid lines – **B**: Control ($R_S = 3.9k\Omega$, $R_F = 100k\Omega$, $C_{dl} = 0.068\mu F$), **C**: Varying C_{dl}, $R_F = 100k\Omega$, $C_{dl} = \{0.068, 0.15, 0.33, 0.56\}\mu F$ for $\text{Ch}_{1,\cdots,4}$ respectively, **D**: Varying R_F, $C_{dl} = 0.068\mu F$, $R_F = \{100, 53.6, 12, 3.9\}k\Omega$ for $\text{Ch}_{1,\cdots,4}$ respectively. $\alpha = 1/600$ calibration factor applied in all.

as follows. The user specifies a list of frequency points to be computed and then loops through these points while grabbing I/Q pair data at every iteration. An iteration ends once the system monitor in the FPGA signals the completing of a signal cycle. This signaling occurs at the end of second cycle of I/Q generation. Two cycles instead of one allows an overwrite of any noise injection that occurs in the first cycle due to the switch in frequency, albeit scaling the acquisition time by a factor of 2. Regardless, this may still be significantly time relative to other fourier methods requiring several cycles per frequency to resolve a wide spectral range of impedance.

IV. RESULTS AND DISCUSSION

For test purposes, we modeled each electrode interface with a simplified Randles equivalent circuit composed of a series Resistance, R_S, connected to a parallel combination of resistance R_F (intended to model the Faradaic process) and capacitance C_{dl} (intended to model the interfacial capacitive double layer) in Fig 2. This exhibits high-pass filtering with a cut-off frequency, $\omega_C = 1/(R_F C_{dl})$ and an R_S offset as shown in eq. 18.

$$Z_o(\omega) = R_S + \frac{R_F}{1 + j\omega R_F C_{dl}} \quad (18)$$

A two-electrode configuration with CE and REF tied at one end of the impedance terminal and the other to a WE on a breadboard with jumper wires. Two test setups were explored – varying R_F and C_{dl} respectively. Arbitrary component values were chosen here. However, the intent was to depict how possible neural electrode-electrolyte interfacial impedance variations (arising from biotic and abiotic changes, e.g. corrosion and glial cell formation) can be concurrently captured over multiple electrode channels and as wide a spectrum as possible. Results for this can be seen in Fig 2. In the control setup, the following RC values are used – $R_s = 3.9k\Omega$, $R_F = 100k\Omega$, and $C_{dl} = 0.068\mu F$. In the R_F-varying experiment, $C_{dl} = 0.068\mu F$, $R_F = \{100, 53.6, 12, 3.9\}k\Omega$ for $\text{Ch}_{1,\cdots,4}$ respectively. While in the C_{dl}-varying experiment, $R_F = 100k\Omega$, $C_{dl} = \{0.068, 0.15, 0.33, 0.56\}\mu F$ for $\text{Ch}_{1,\cdots,4}$ respectively. $N_{\text{in}} = 10$ was used to set $V^{\text{ref(o)}} \approx 40$ mVpp

below the typical 50 mVpp limit for ensuring small signal linearity. $N_{\text{out}} = 100$ offers sufficient impedance SNR. The measured impedance is expressed as;

$$Z(\omega) = \alpha Z_o(\omega) \quad (19)$$

where α is a calibration factor accounting for component variations, possible non-linear IV relations arising from scaling V^{ref} and R_{out} scaling. We set $\alpha = 1/600$ based on empirical observations for the above-mentioned protocols. A spectral scan with 100 logspaced points over the $(5\times10^{-2} - 5\times10^4$ Hz) band took only 3min 40s. This comprises of $2\times$ periods for each frequency (with the largest period being 20s), and the software controller overhead. Wider deviations are apparent at higher frequency due to approaching sampling limits.

A. Scaling to More Channels

The concept presented is scalable to high density neural MEAs bottlenecked mainly by the PC-FPGA communication speeds. The OK-XEM6310 comes with a USB 3.0 capable of up to 38.1 MB/s transmission speeds for a block read length of 1024 bytes. Assuming a sufficiently large buffer for staging I/Q data in FPGA, an I/Q pair of 8 bytes (i.e. 2×32 bits) precision, could support almost 5×10^6 electrode channels which is well beyond the $59,760$ state-of-the-art MEA channel density [3]. Of course, with the accompanying increased slice utilization which a newer and more capable FPGA may meet. More so, analog integration by log-domain filtering could potential reduce the high computational resource requirements.

V. FUTURE WORK

Moving forward, validation in *in vitro* neural MEAs setups will be explored. This will be useful in capturing spectral shifts in impedance that arise due to aging and corrosive factors for various electrode materials. There exist opportunities to adopt nonlinear optimization methods to automatically find ideal R_{in} and R_{out} values in the calibration process. Ultimately, an integrated circuit approach will allow for compactness and low-resource I/Q pair generations as quarter cycle integrations could be performed with low-power analog subthreshold integrators. Code and supplementary made available at https://github.com/Adakwaboah/HermEIS_IQ.

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