Assessing Magnetic Attack on Commercial 40nm pMTJ STT-MRAM

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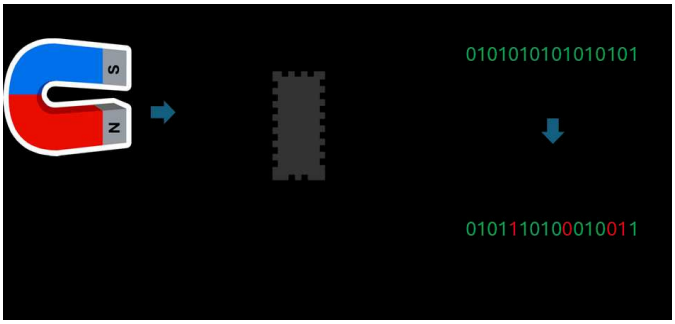
Abstract: In this paper, we experimentally evaluate the data integrity of commercial Spin-Transfer-Torque (STT) based Magnetic Random Access Memory (MRAM) under external magnetic fields. Our findings reveal that the standby immunity field for the tested device is around 180 mT, beyond which both read and write operations are significantly affected. Post-exposure retention analysis indicates that over 50% of bits become noisy after field exposure, though this can be corrected with an overwrite operation. We provide a physical explanation for the origin of these noisy bits. Our results have significant implications for the data integrity of STT-MRAM under magnetic field-based external attacks.

Keywords—STT-MRAM, Nonvolatile Memory, Magnetic attack, Reliability, Memory testing, MTJ.

I. Introduction

Spin-Transfer-Torque Magnetic Random Access Memory (STT-MRAM) is widely regarded as a promising candidate for universal memory technology with its nonvolatility, non-destructive readout capability, high operational speed, and high endurance [1]. With operational speed and memory architecture similar to Static Random Access Memory (SRAM), and density like Dynamic Random Access Memory (DRAM), and non-volatility like flash technology it stands out as a promising alternative to mainstream memories and showing the prosect of fulfilling the role of a universal memory. Consequently, the market share of STT-MRAM is rapidly increasing, with an expected growth of around 27% by 2031 [2]. This increasing demand indicates the use of STT-MRAM for a wide range of applications such as automation, space, and healthcare.

Despite having huge potential, it is crucial to explore the reliability and security aspects of STT-MRAM under various extreme environmental conditions. Previous studies have explored the potential and reliability issues of STT-MRAM through device-level characterization [3] and wafer level testing [4]. Several recent studies performed physical testing on MRAM. For example, Chakraborty et al. [5] examined the impact of magnetic field exposure on the read and write operations of a commercial-off-the-shelf (COTS) Toggle MRAM chip. They have found that external magnetic field on Toggle MRAM causes significant data corruption and increases read current during magnetic stress test. Similarly, Holst et al. conducted an experiment [6] using FPGA-based March testing on commercial Toggle MRAM to monitor the bit error rate and the influence of magnetic fields. Additionally, Tsiligiannis et al. [7] conducted reliability experiments on COTS Toggle MRAM under high energy neutron and alpha radiation conditions. They did not find any soft error or bit disturbance. In addition to experiment, several simulation studies [8], [9], [10] explored stability and error-correcting techniques for MRAM under extreme conditions.



Prior studies show that MRAM is highly sensitive to external magnetic fields, which poses a significant security vulnerability for magnetic memory. As shown in Fig. 1, data stored in the MRAM can be flipped by bringing a magnet near the memory chip. Even though previous reports performed extensive analysis on the magnetic field vulnerability of MRAM technology, most of these studies were conducted on in-plane Toggle MRAM chips. None of the previous experimental work examined the vulnerability of commercial perpendicular Magnetic Tunnel Junction (pMTJ) based STT-MRAM chips under magnetic attack. Since pMTJ-based MRAM surpasses in-plane MTJ in terms of scalability [11], a detailed study on magnetic attacks on physical pMTJ STT-MRAM is crucial.

In this study, we experimentally investigate the read, write, and retention performance of a commercial STT-MRAM chip subjected to varying magnetic field attacks. We also perform bit by bit analysis of the magnetic field induced data corruption. Our primary contributions are as follows:

- Conducted a comprehensive soft error characterization of the commercial STT-MRAM, determining the *standby immunity field ($F_{immunity}$)* for both write and read operations.

- Analyzed the impact of magnetic field exposure duration on data integrity of the STT-MRAM chip.
- Formulated a hypothesis and monitor the behavior of noisy bits in the STT-MRAM under both active magnetic field exposure and post-exposure conditions.
- Our analysis shows that the magnetic field induced failures are not permanent, and data can be successfully overwritten on the memory location after field exposure.

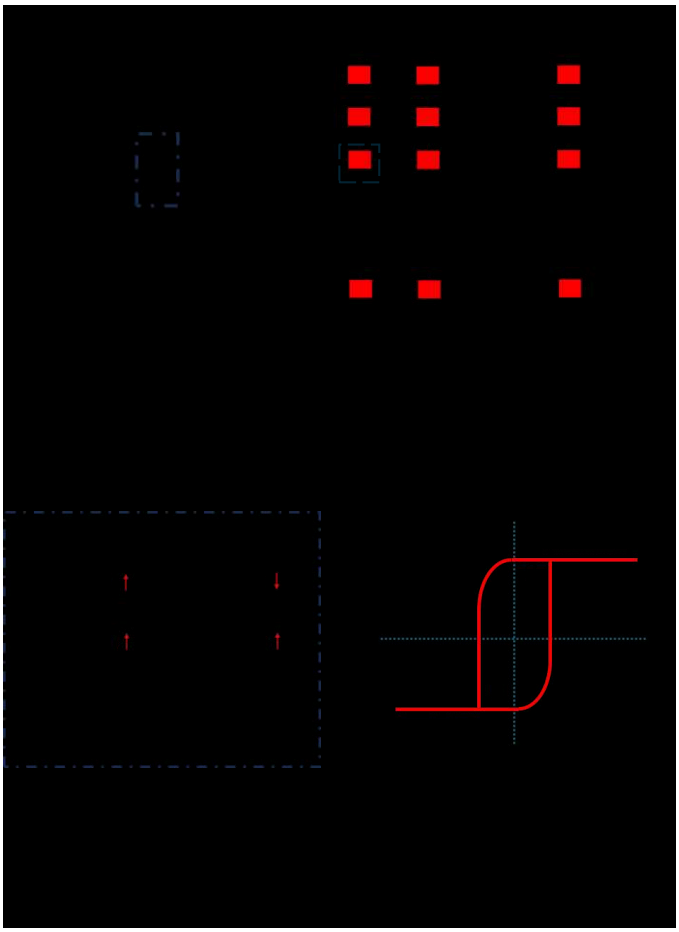
This paper is divided into five sections. Section II describes the background of the STT-MRAM. Section III discusses the Experimental setup for magnetic field exposure. Experimental results and analysis are shown in Section IV and the conclusions are provided in Section V.

II. Background of STT-MRAM

The basic cell structure of a STT-MRAM contains one transistor and one memory element (See Fig. 2(a)) and every STT-MRAM chip contains an array of memory cells as shown in Fig. 2(b). The core component of MRAM, the Magnetic Tunnel Junction (MTJ), relying on magnetic anisotropy energy to store information [12]. The structure of memory cell is made up of two synthetic ferromagnetic materials layers with a nonmagnetic insulating tunnel barrier in between (shown in Fig. 2(c)). The magnetic orientation of the reference layer is fixed, and when current flows through the MTJ and transistor, it induces spin transfer torque, programming the free layer of the MTJ. The free layer magnetization direction can be changed either by applying magnetic field higher than coercive field or injecting spin-polarize current through the MTJ.

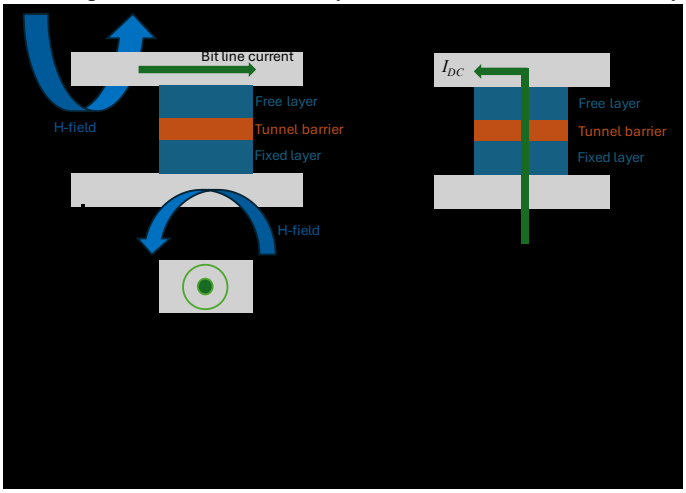
The switching is operated by adjusting magnetic field, shown in Fig. 2(d), and depending on the direction (parallel or anti-parallel) of two ferromagnetic layers. The difference in their resistance is decided by the Tunnel Magneto Resistance (TMR). For a better performing device it is expected that TMR is as high as possible because it will ensure the robust barrier between the two bit states. However, the value of TMR highly depends on the material property of the insulating layer. It is reported that MgO based barrier layer can achieve TMR around 200% [13]. Any operation on a bit in a STT-MRAM chip is accomplished by using the word line (WL) to turn on and off the nMOS transistor. The state of the MTJ is determined by the current flow between the Bit Line (BL) and Source Line (SL), which is influenced by the MTJ's resistance. The sensing circuit detects the current to identify the MTJ state. Notably, the read current through the MTJ is significantly lower than the write current.

Significant technological advancements have made MRAM increasingly suitable for next-generation memory applications, leading to the development of two main types: toggle-MRAM (Fig. 3(a)) and STT-MRAM (Fig. 3(b)). These types differ in architecture and programming mechanisms. Toggle-MRAM uses a cross-point architecture, where current flowing along its bit and digit lines generates a magnetic field that performs write operation by deciding magnetization direction of free layer. In contrast, STT-MRAM operates through current-driven switching of its free layer, where a large current (I_{DC}) passes through the MTJ and transistor. This current induces spin-transfer torque to program the free layer magnet. While STT-MRAM is mainly current-driven, an external fixed magnetic field can also polarize the current. As the second generation of MRAM, STT-MRAM offers higher density and greater versatility than toggle-MRAM, making it more practical for a wide range of applications.



III. Experimental Setup and Test Flow

The experiment presented in this paper aims to provide insight into realistic magnetic field interference on MRAM and understand the soft error characteristics during both read and write operations. For this study, we used a 4Mb commercially



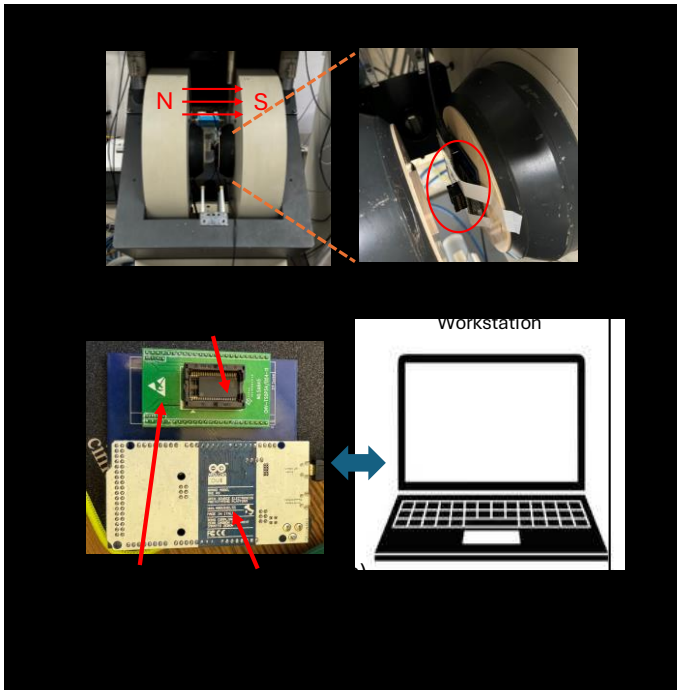
available perpendicular MTJ (pMTJ) STT-MRAM, manufactured by Avalanche, with a 40nm technology node. The parameters for the STT-MRAM chip used are shown in Table I.

TABEL I: STT-MRAM Chip Specifications [14]

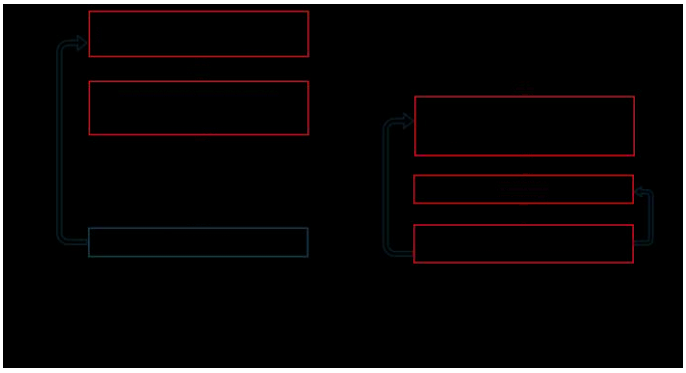
Parameter	Value
Operating Voltage	2.70 V - 3.60 V
Density	4Mb
Word size	16 bits
Techonology	40nn pMTJ STT-MRAM
Read and Write cycle time	35 ns
Read and Write current	20 mA

Our setup included a custom-designed board with a TSOP-48 socket to hold the STT-MRAM chips. The socket was connected to an Arduino Due microcontroller through a custom design printed circuit board (PCB). The Arduino microcontroller was further linked to the workstation for data transfer through USB port. For the field, we have used Bruker ELEXSYS ESR-500 continuous wave electron paramagnetic resonance spectrometer [15], which offers a well controllable and precise magnetic field. The direction of the field is applied perpendicularly to the top surface of memory chip as shown in Fig. 4(a).

To evaluate the read performance of the memory chip under an active magnetic field, we employed a step-by-step measurement approach, as shown in Fig. 5(a). Prior to activating the magnetic field, we wrote specific data patterns to the memory. Starting with an initial magnetic field of 50 mT, we performed read operations while the field was active. To assess data retention in STT-MRAM under active magnetic field, we collected data at 5-minute intervals, repeating the read operation 10 times. After completing the data collection for 50 mT, we incrementally increased the magnetic field strength, continuing observations up to 500 mT.



To understand the writing performance under an active magnetic field, we followed a similar experimental flow outlined in Fig. 5(b). The steps within the red outline box indicate when the magnetic field is active, while those in the black outline box indicate when the field is not active. Initially, we exposed the STT-MRAM to a 50 mT magnetic field and wrote an image data pattern to the memory while the field was active. After writing to each word, a read operation is performed to collect the data from all words and store it in a text file.



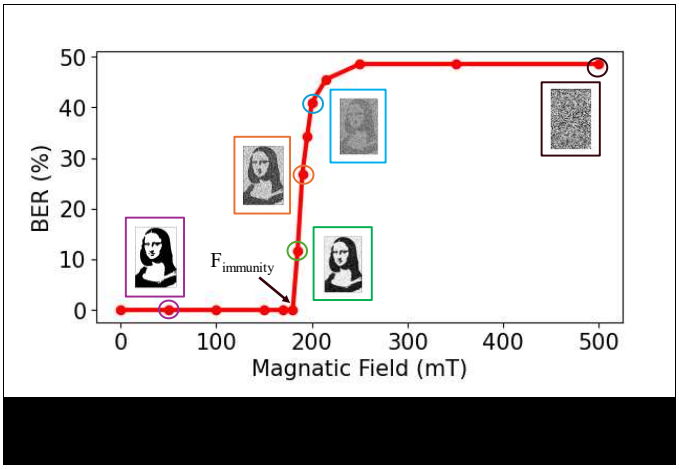
To ensure that the memory's pre-exposure condition remained consistent for each observation, we performed a refresh operation every time data was stored. We repeated this process for various magnetic fields, up to a maximum of 500 mT. For both read and write operation, quantifying the mismatch between the pre-expose and post-expose bit state, we measure the Bit Error Rate (BER) as follows:

$$\boldsymbol{BER}(\%) = \frac{\boldsymbol{\#\ of\ bits\ changes\ their\ state}}{\boldsymbol{Total\ \#\ bits\ in\ the\ Memory}} \times \mathbf{100} \quad (\mathbf{1})$$

IV. Result and Discussion

A. Magnetic Attack on STT-MRAM Read Operation

Fig. 6 illustrates the rate of data corruption in STT-MRAM memory under varying magnetic fields. Data corruption is quantified using the BER equation (Eq. (1)). The memory chip is exposed to an external magnetic field for 5 minutes, after



which data is read from the chip. The images at specific data points visually represent bit changes for each corresponding magnetic field. The BER trend shows a sharp transition at the standby immunity field ($F_{immunity}$), measured approximately at 180 mT. Beyond this point, a sharp increase in BER is observed for external fields up to 215 mT. The BER remains saturated at around 48% for external fields above 250 mT. Interestingly, the saturated image is neither completely black nor completely white; instead, it resembles a salt and pepper image with no recognizable features of the original Mona Lisa image.

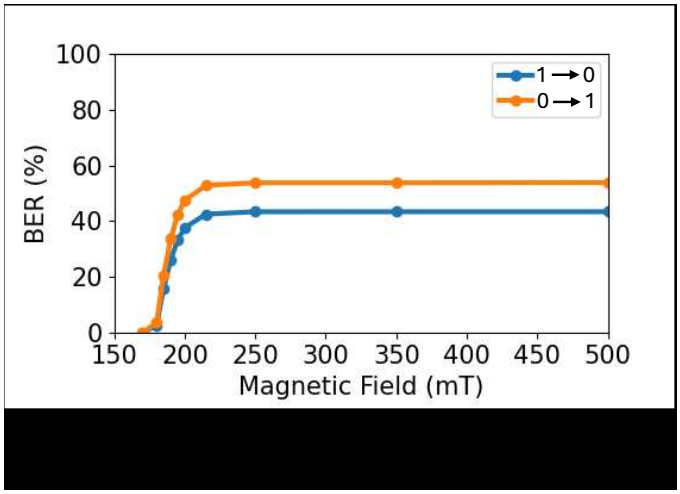
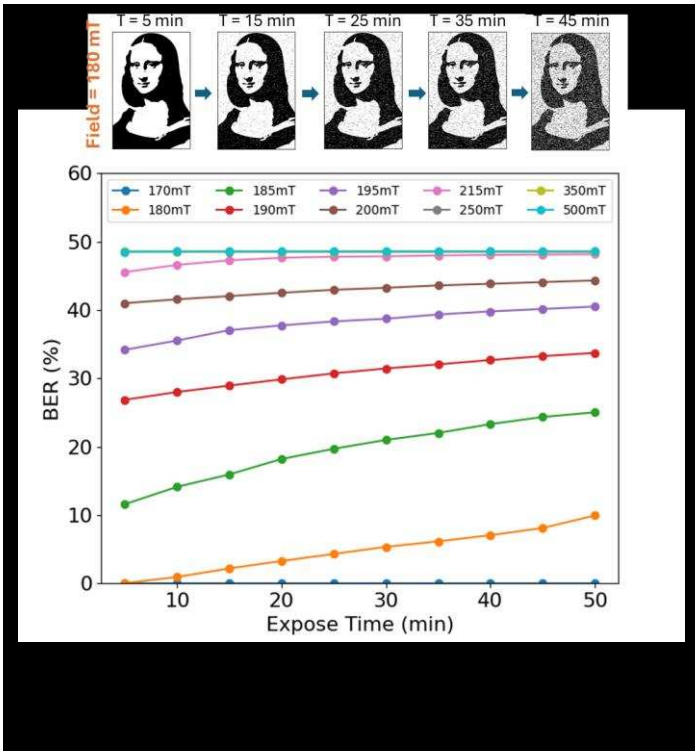


Fig. 7 presents a bit-by-bit analysis illustrating the bit-flip percentage arising from logical zero bits and one bits separately. Both logical transitions show increasing trends with the strengthening magnetic field. A dramatic increase in bit failures occurs as the field immunity point is reached at 180 mT. The transition from "0" to "1" is more dominant, surpassing the "1" to "0" changes. For instance, at 200 mT, the number of bits changing from "0" increased by about 10% more than those holding logic "1" and remained saturated. The switching of the MTJ's free layer is highly dependent on the direction of the applied magnetic field [5], suggesting an expected asymmetric bit-flip rate for logical zeros and ones. However, the comparable bit-flip rate measured in Fig. 7 indicates that the applied field may not completely align with the magnetization direction of the free layer. In this work, we applied a field perpendicular to the top surface of the chip. While one of the two logical states could be more affected depending on the field direction, we found that bits holding logic "0" were more sensitive to the magnetic field than those holding logic "1".

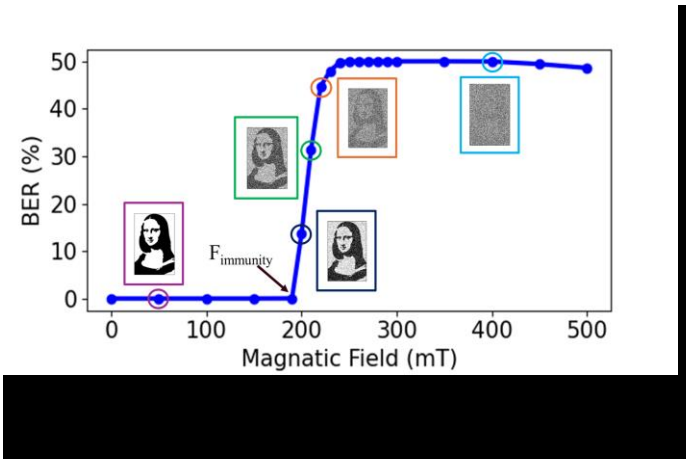
Fig. 8 shows the percentage of stored data corrupted with increasing exposure duration for different magnetic fields. The top images illustrate the gradual evolution of the corrupted image with time intervals under magnetic field of 180 mT. It is observed that increasing exposure duration leads to significant data corruption, especially after reaching the immunity field (180 mT). In other words data retention time in MRAM is significantly affected under magnetic field exposure with higher external field causing significant decrease in retention time. Note that the image corruption illustrated in Fig. 8 is the results of cumulative exposure time. Hence BER tends to saturate at higher exposure fields. The key takeaway from this figure is that continuous exposure to the magnetic field can increase errors in



STT-MRAM read operations, posing a significant security concern, especially for read-only memory used in IoT or automotive application.

B. *Magnetic Attack on STT-MRAM Write Operation*

[redacted] The overall trend in write errors for the STT-MRAM reveals no data corruption before reaching the standby immunity field ($F_{immunity}$) of 200 mT, indicating successful data writing to the memory. However, at 200 mT, the BER increases to approximately 13%. A slight field increase to 210 mT and 220 mT elevates the BER to about 31% and 46%, respectively, causing significant data distortion on the memory chip. Beyond 250 mT, the BER saturates and remains stable up to 500 mT. An interesting observation from Fig. 9 is that even a slight increase in the

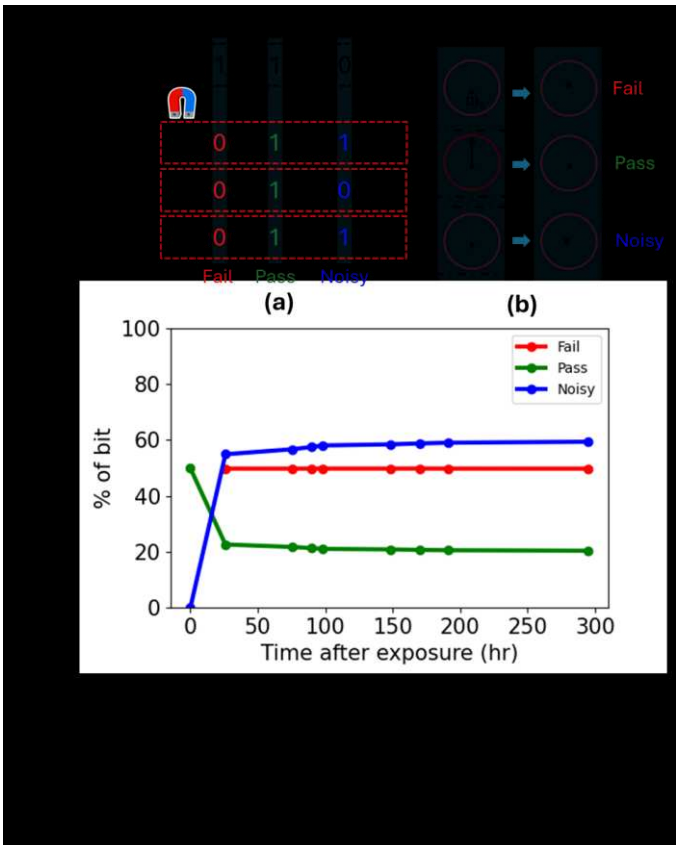


magnetic field beyond the standby immunity threshold leads to a significant spike in bit flips. This is likely attributed to the coercive field, which represents the barrier between two logical states (see Fig. 1(d)), influences the MTJ magnetization switching process [16]. Consequently, even minor magnetic field changes can induce substantial bit state transitions, which persist at higher fields.

C. Post Exposure Data Retentation of STT-MRAM

We evaluate the post-exposure failure characteristics of the STT-MRAM by operating it in the read-only mode for two weeks at room temperature. We periodically read the memory content during this time. The measurement procedure is illustrated in Fig. 10(a) where we classify three groups of bits. If a bit never changes its state from its pre-exposed value, we classify it as pass bit (green). If a bit changes its state at least twice during successive read operations, we classify them as noisy bits (blue). During each read operation if a bit value is different from its original value, we coin them as fail bits. Note that some of the noisy bits will be counted under fail bits during a particular read operation.

Fig. 10(c) shows the percentage of pass, fail and noisy bits with retention duration. Interestingly, we find that a significant portion of the bits become noisy after the field-exposure. We provide a hypothesis behind the increased number of noisy bits in Fig. 10(b). We illustrate the magnetization direction (m_z) of the free layer with arrow before and after field exposure. If the magnetization direction does not change after field exposure, the memory cell retains its correct logical value which is coined as pass bit. If m_z completely flips its direction, the bit value is read as steady fail bit. However, if the m_z changes to an intermediate point, the cell becomes noisy. Depending on the noise amplitude, the cell changes its state during subsequent read operation. Even though magnetic field exposure makes the exposed bits noisy, it is not a permanent effect. We have overwritten a new set of data on the exposed memory chip and the bits become stable again. So, we conclude that the field induced errors are soft-error, and we have not observed any hard errors (stuck-at zero or stuck-at one) for field exposure up to 500 mT on the chip under test.



V. Conclusion

In this study, we experimentally examined the susceptibility of STT-MRAM to soft errors under varying magnetic fields. Our findings show that the performance of commercially available STT-MRAM chips is highly sensitive to magnetic field exposure, specifically for field strength beyond 180 mT. Increased magnetic fields cause massive data corruption in both write and read operations. We also observed that the duration of exposure significantly affects read stability and retention errors. A substantial portion of memory bits became noisy after magnetic field exposure, though these errors were not permanent and could be corrected by rewriting the chip. Overall, our results indicate that external magnetic fields pose a potential security risk for STT-MRAM, underscoring the need to enhance its shielding capabilities.

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