A Novel Protection Design Process to Increase Microgrid Resilience

Mark Vygoder, *Graduate Student Member, IEEE*, Farzad Banihashemi, Jacob Gudex, *Graduate Student Member, IEEE*, Andrew Eggebeen, Giovanna Oriti, *Senior Member, IEEE*, and Robert M. Cuzner, *Senior Member, IEEE*

***Abstract*—Successful discrimination of, isolation from, and recovery against short-circuit electrical faults within microgrids having distributed energy resources (DERs) is challenging, as protection coordination must include not only the distribution equipment, but also control and low voltage ride-through settings of DERs. This is especially the case when grid resilience is improved by use of the microgrid to maintain services from DERs (localized to an installation) following utility grid outages. Under *islanded* configurations, continued reliability of power delivery is essential, even in the face of subsequent electrical faults. The main purpose of this paper is to propose a novel protection design process, and to demonstrate it on an islanded ac microgrid with parallel feeders. The contribution is a methodology for coordinated circuit breaker protection and ride-through settings, thereby maximizing the post-fault recoverability of an ac microgrid subject to faults in an islanded configuration. The aim is improve the microgrid resilience in islanded configurations. The protection and IEEE Standard 1547-2018 ride-through settings are validated in controller hardware-in-the-loop simulation, validating the proposed design process. Additionally, detailed implementation of ride-through enabling controls are discussed.**

***Index Terms*—Power system protection, microgrid, low voltage ride-through, IEEE standard 1547, distributed power generation.**

I. Introduction

ENERGY secure power distribution systems enable dependable power and energy delivery, even in the face of off-nominal events, such as short circuit electrical faults. Energy security can be broken down into three pillars: *resiliency, reliability, and efficiency* [1]. The United States (U.S.) government has set directives for improving grid resilience, while simultaneously decarbonizing energy generation. [2], [3], [4].

The quantification and definition of resilience continues to be an active area of research [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16]. Parallels to resilience metrics development can be drawn from the fields of computer architecture and Machine Learning (ML). For computer architecture, the debate on Reduced Instruction Set Computer (RISC) versus Complex Instruction Set Computer (CISC) architectures could not be fairly compared until a set of metrics for computational performance were agreed upon in the mid 1980s [17]. Similarly, bench-marking tools such as MLperf^{TM}were developed to assess performance of ML algorithms and high performance computing [18].

Furthermore, microgrids can help achieve goals of *both* improved resiliency and decarbonization by providing redundant operational configurations to maintain continuity of services and integration of renewable energy sources, respectively. Regarding the latter, since grid outages last for an unknown amount of time, the *islanded microgrid* (disconnected from the main utility grid) with distributed energy resources (DERs) servicing downstream loads is a default configuration where assurance of energy security is essential. The islanded microgrid may operate in multiple configurations, as defined by the operational states of the connected power and energy sources (the DERs) and diverse load connectivity. Since the microgrid and associated DERs comprise the source of supply, the paradigm of binary decision-making based upon only grid-connected versus island modes no longer applies [19].

This paper proposes a novel protection design process to increase microgrid resilience, and a methodology for configuration-coordinated circuit breaker protection and low voltage ride-through (LVRT) settings. The aim is to maximize the post-fault recoverability of an islanded ac microgrid, subject to a range of electrical short circuit fault types. The groundwork for this work is first laid by defining resilience for critical facilities, which require high levels of operational availability, and then addressing microgrid protection and DER fault ridethrough controls. The remainder of the paper develops the protection design process and then applies it to a case-study on an islanded ac microgrid with parallel feeders.

Manuscript received 15 August 2023; revised 29 January 2024; accepted 23 February 2024. Date of publication 13 March 2024; date of current version 22 July 2024. Paper 2023-PSEC-1162.R1, presented at the 2021 IEEE Energy Conversion Congress and Exposition, Vancouver, BC, Canada, Oct. 10–14, and approved for publication in the IEEE Transactions on Industry Applications by the Power Systems Engineering Committee of the IEEE Industry Applications Society [DOI: 10.1109/ECCE47101.2021.9595450]. This work was supported in part by the Naval Facilities Command (NAVFAC) Naval Shore Energy Technology Transition and Integration (NSETTI) Program, in part by National Science Foundation (NSF) under Grant 1939124, and in part by the Office of Naval Research (ONR) under Grant N00014-24-1-2070. *(Corresponding author: Mark Vygoder.)*

Mark Vygoder, Farzad Banihashemi, Jacob Gudex, Andrew Eggebeen, and Robert M. Cuzner are with the Department of Electrical Engineering, University of Wisconsin, Milwaukee, WI 53211 USA (e-mail: mvygoder@uwm.edu; banihas2@uwm.edu; jdgudex@uwm.edu; robcuzer@ieee.org; eggebee6@uwm.edu).

Giovanna Oriti is with the Department of Electrical and Computer Engineering, Naval Postgraduate School, Monterey, CA 93943 USA (e-mail: goriti@nps.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TIA.2024.3377171.

Digital Object Identifier 10.1109/TIA.2024.3377171

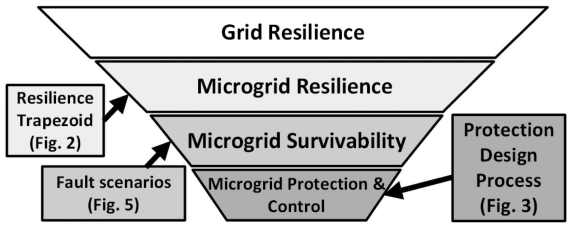


Fig. 1. Microgrid resilience funnel.

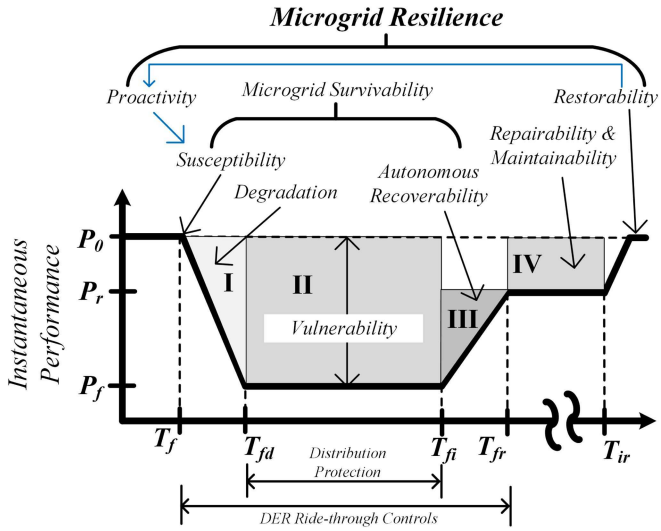


Fig. 2. Microgrid resilience and its attributes with respect to fault recovery.

A. Relating Microgrid Resilience Taxonomy to Fault Detection, Isolation, and Recovery

Fig. 1 shows a funnel to describe broad topic grid resilience, with progressively more niche topics of microgrid resilience, microgrid survivability, and microgrid protection & controls.

The scope of grid resilience looks at grid infrastructure to be resilience against adverse weather and operational resilience to repair the failed network [5], [6], [7], [8], [9], [10], [11], [12].

However, for microgrid applications, such a metric may not be as useful since the microgrid can operate in islanded-mode. Islanded operation of the microgrid is often used to support critical loads, so a power delivered based metric, such as instantaneous performance may be used. *Instantaneous performance* is the power delivered to system loads divided by the system's load demand at a given moment in time [13], [20].

A two-level trapezoidal shape is shown in Fig. 2. The shapes take inspiration from [6], [7], [13], [16], and shows a qualitative curve of resilience attributes over time in response to faults showing relationships between resilience attributes, instantaneous performance on the y-axis, and events during fault detection, isolation, and recovery process. The first trapezoid accounts for the microgrid's instantaneous performance during electrical fault or the mircogrid's *survivability*. Survivability can broken down into attributes susceptibility, vulnerability, recoverability [21], [22], [23], [24].

Susceptibility is the ability to avoid failures. For mobile applications, such as naval vessels or aircrafts, the vehicle's ability to maneuver to avoid threats comes into play, not solely the reliability of the equipment [21], [23], [24], [25], [26]. For land systems, the Electrical Power System (EPS) is typically in a fixed location, which simplifies the evaluation. An example of improving this attribute is moving overhead cabling underground, or moving equipment inside to avoid impact of adverse weather.

Vulnerability is the ability to respond to and isolate a fault. This attribute is applicable during the time period between when a fault is detected (T_{fd}) to when a fault is isolated (T_{fi}). This attribute could be affected by the protective scheme and distribution system complexity. Invulnerability can also be used as the complement of vulnerability. The greater the invulnerability of the system, the less the system's instantaneous performance will degrade under fault conditions (P_f).

Recoverability is the microgrid's ability to recover from a fault. This starts at fault isolation time (T_{fi}) and goes until the fault recovery time (T_{fr}) has elapsed, where the latter represents the time it takes for the voltage to return to within the nominal range after the fault is isolated from the system. Recoverability is assumed to be governed by autonomous actions in relatively short time-frames. The performance of the recovered system (P_r) is between nominal performance (P_0) and (P_f), as not all loads may be satisfied due to isolation of the faulty section of the system.

Actions such as manual closing of feeders and physical repairs to damaged parts of the EPS would fall under *Repairability and maintainability*. These actions can take hours or days to perform, where repairability and maintainability. These metrics are quantifiable in terms of time and capability attributes. For example, an overhead cable is easier to repair than an underground cable. The time it takes to repair the infrastructure (T_{ir}), fully restoring it to its pre-event performance (P_0) quantifies the system *restorability*.

With the data acquired as a consequence of prior fault detection, isolation and recovery response to events, proactive actions (*proactivity*) may be implemented to improve the susceptibility of the system against future faults.

Relating the attributes above to microgrid equipment performance, the distribution equipment is active between fault detection and fault isolation, while the DERs go into ride-through between fault inception and fault recovery. This time may be affected by adjusting protection settings on distribution equipment or LVRT settings on DERs. Alternatively, ride-through actions may be avoided with the addition of energy storage to supply the microgrid in post-fault recovery. Thus, design choices at the electrical protection and levels at which ride-through is triggered have direct links to microgrid survivability, and thus, the overall microgrid resilience.

B. Islanded Microgrid Protection and DER Fault Ride-Through Coordination Challenges

To understand the microgrid's instantaneous performance under fault detection, isolation, and recovery under islanded microgrid conditions, proper design and coordination of protection

settings for distribution equipment and LVRT settings for DERs must be performed [19].

However, designing the protection for an islanded microgrid may be complex due to [19], [27], [28]:

1) operation in both grid-connected and islanded mode;
2) possible ring or meshed EPS architectures with bi-directional power flow;
3) DERs connected at various locations within the EPS;
4) DER operational states (i.e. whether or not they are online) at the time of fault inception;
5) significant differences in fault currents characteristics between synchronous generator-based DERs, a combination of synchronous generator-based and inverter-based DERs, or just inverter-based DERs;
6) allocation of protective functionalities between distribution equipment and power conversion equipment.

Little guidance through standardized practices have been given to address this last point, since the mixing of power electronic-based DERs and conventional power systems into meshed microgrids is relatively new and requires acumen in both fields. DERs are required to meet ride-through and grid-supporting requirements per IEEE Standard 1547-2018 [29] when in grid-connected mode.

According to intentional islanding-mode, under Section VIII-B of [29], DERs "shall trip" when subject to undervoltage (UV) and underfrequency (UF) as defined in Sections VI-D and VI-E, respectively. However in [29], ride-through requirements only for grid abnormalities are addressed. Abnormalities that can occur during islanded configuration are not covered by this standard. With only mandatory "shall trip" settings and absence of guidance on LVRT settings, DERs in islanded mode may go offline (trip) due to internal low voltage protections during load transients or they may trip prematurely during faults before the protection scheme can isolate the faulty branch. Premature tripping of DERs may significantly change the momentary generation capacity and may overload remaining connected DERs, leading to cascading failures and possible system blackout. Alternatively, without any trip settings, DERs may continue to operate under abnormal conditions, which can lead to DER equipment damage and other safety issues.

Recent works present protection schemes of islanded ac microgrids in the presence of inverter-based DERs [30], [31], [32], [33], but have not taken LVRT capabilities into the account. [34] and [35] investigate LVRT controls for photovoltaic (PV) generation system, but for grid-connected systems. In [36] system recovery and LVRT capability are both investigated for a grid-connected PV system, which has different requirements than an islanded microgrid. [37] presents a protection scheme and coordination settings considering LVRT through capability of the inverter-based DGs, but applied to a radial microgrid, as opposed to a ring bus.

Detailed survivability investigations of synchronous generator-based DERs under load transient and transition to islanded mode were performed in [38], [39], [40]. An example of microgrid survivability can be seen in [41], [42]. This work addressed overloading issues caused by transient loads steps of mixed synchronous generator-and inverter-based DERs, leading to voltage collapse of the microgrid. The work proposed controls and protection settings to fix this particular issue. This work focuses on the microgrid survivability in the presence of short-circuit electrical faults.

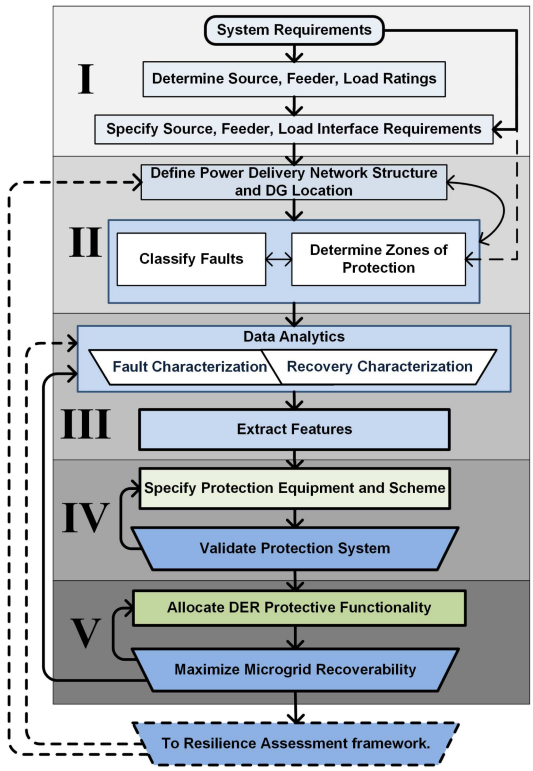


Fig. 3. Microgrid protection design process.

Lagos et. al highlight the issue of coordination coordination of protection design and LVRT setting in [19]. The researchers show how inverter-based DERs can cause issues with protection coordination under different operational scenarios of the microgrid and how, even with the ride-though settings compliant to standards, if not correctly coordinated with the protection scheme, LVRT or frequency ride-through may cause DERs to disconnect, even though the DERs are within safe area of operation, and can lead to system collapse. They also review different microgrid protection strategies and demonstrate an adaptive protection scheme through Controller Hardware-in-the-Loop (CHiL) simulation. However, the details of LVRT controls implementation and microgrid recovery were outside the scope of [19].

C. Novel Contribution and Paper Organization

The authors of this manuscript demonstrate the iterative microgrid protection design process shown in Fig. 3 [43]. This process is intended to help researchers and practicing engineering more efficiently design protection coordination systems, including the impacts of high levels of DER penetration and variations in grid-connected and islanded configurations. The process in [43] was demonstrated on a case-study of an islanded

ac microgrid with a ring bus structure, with a mix of synchronous generator-and inverter-based DERs.

The authors highlight that coordination between power distribution protective-relaying settings and inverter-based DER LVRT setting must be considered to maximize the recovery of the microgrid, as both impose limitations on each other. DERs must ride-through the fault-isolation time of the protection scheme and, simultaneously, the protection scheme must isolate the fault within the DER's ability to ride-through, and recover from, the fault. The design process enables this coordination.

Additionally, recoverability from faults of an islanded ac microgrid with a ring bus structure, having both synchronous generator-based and inverter-based DERs is observed. Maximizing the DERs that remain connected, after a fault condition is isolated, the recoverability and (P_r) of the microgrid is improved. Therefore, following the novel protection design process improves recoverability, as quantified by post-recovery instantaneous performance, improving microgrid resilience over.

This manuscript extends the work presented in [43], by validating the case-study in real-time CHiL simulation, and providing additional details on enabling DER controls for LVRT.

The contributions of this paper are as follows:

1) Demonstration of a microgrid protection design process which can be applied to any microgrid system. The process accounts for protection settings of distribution equipment and LVRT settings of power conversion equipment.
2) A detailed explanation of controls required to successfully implement IEEE Standard 1547-2018 LVRT controls. This includes higher-level state machine-based logic, LVRT specific state machine, feedback control, and PI implementation, all of which are required to enable ride-through, and recovery from, low voltage transients and outage events
3) Simulation results that detail each step of the protection design and selection of LVRT settings.
4) Validation of offline simulation results through real-time CHiL simulation, including a detailed explanation of CHiL implementation of directional overcurrent relays on an FPGA-based CHiL system.
5) Providing larger context as to how fault isolation protection and recovery controls affect microgrid resilience.

The authors present the step-by-step process in Section II to design a microgrid's protection scheme. This section also introduces an example of industrial EPS as a case-study. Section III presents a fault characterization of the microgrid, which will be used in Section IV to design and coordinate directional relay settings for the ring bus. Then, Section V implements category III LVRT from IEEE Standard 1547-2018 [29] with momentary cessation in the PV farm's controls to maximize the DERs connected during system recovery. Section VI discusses and shows CHiL implementation of the protective settings and controls derived in the Sections IV and V, validating the design process.

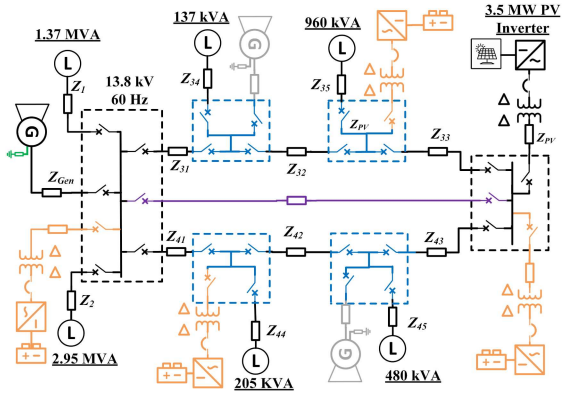


Fig. 4. Configuration options for Islanded AC Microgrid.

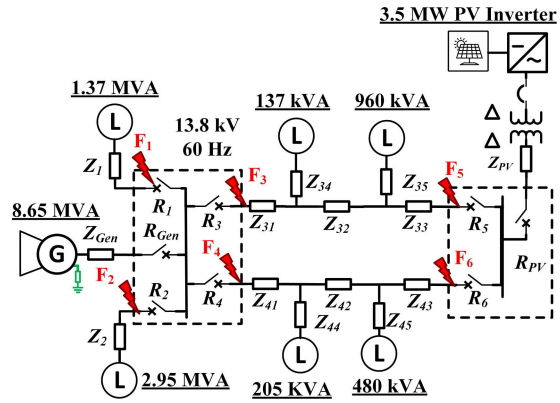


Fig. 5. Present Islanded AC Microgrid.

II. Microgrid and the Protection Design Process

Fig. 3 shows the process for systematically designing microgrid protection and is made in an effort to streamline protective design for complex microgrids. This iterative process was first proposed in [44], and modified for microgrid resilience.

Fig. 4 shows the islanded micogrid under consideration. The black lines represents the existing microgrid of an industrial facility with critical loads. The facility is seeking to improve the resilience of their microgrid in islanded mode, and assess possible infrastructure improvements such as: additional switchgear to improve fault discrimination capability around the ring bus (blue lines), a redundant pathway between the centralized gensets (left generator in Fig. 4) and the PV farm (purple lines), distributed energy storage systems (BESS) (orange lines), and distributed genset locations (top and bottom generators in Fig. 4 in gray). Specific rating for the distributed BESS and gensets will be in future work. However, first, the performance of the existing microgrid's protection and ride-through settings must be coordinated to enable future bench-marking of the present microgrid and for future improvements with respect to against resilience attributes listed in Section I-A.

The diagram in Fig. 5 shows the ac microgrid topology and fault locations, which is the result of execution of steps I and II (from Fig. 3), and through discussions with the industrial partner.

TABLE I
DOC AND DEF RELAY SETTINGS

Relay	I rated (A)	DOC TMS	DEF TMS
RGen	363	0.019	0.08
RPV	159	0.007	N/A
R1	74	inst.	inst.
R2	167	inst.	inst.
R3	159	0.015	0.04
R4	159	0.015	0.04
R5	159	0.00175	0.001
R6	159	0.00175	0.001

TABLE II
CATEGORY III VOLTAGE RIDE-THROUGH REQUIREMENTS (TABLE 16 IN [29])

Voltage Range (p.u.)	Operating Mode / Response	Minimum ride-through time (s) (design criteria)
$V > 1.20$	Cease to energize	N/A
$1.10 < V \leq 1.2$	Momentary Cessation	12
$0.88 < V \leq 1.10$	Continuous operation	Infinite
$0.77 < V \leq 0.88$	Mandatory Operation	20
$0.50 < V \leq 0.70$	Mandatory Operation	10
$V < 0.5$	Momentary Cessation	1

For the purposes of this study, the present microgrid contains four 2.16 MVA / 1.70 MW diesel gensets, totaling 8.65 MVA / 6.83 MW in the centralized location. The facility can implement load-shedding during islanded-mode, to reduce the total load to 6.1 MVA, about 70% of the genset's capacity, if necessary. The loads vary in power factor ratings from 0.85 to 0.95, and were sized using historical data. Cable lengths were determined from the facility one-line diagrams and physical layout and are tabulated in Table V in the Appendix. Recently, the facility has installed a 3.5 MW solar PV farm to reduce energy costs, which is located 3.5 km away from the diesel gensets.

III. FAULT CHARACTERIZATION

To properly assess the microgrid during fault transients (steps III and IV) and post-fault states (step V), inertial dynamics, fault dynamics, and fault recovery enabling controls of synchronous generator and inverter-based DERs must be included. The diesel genset model contains engine delays, mechanical inertial dynamics, governor controls, IEEE DC1A exciter with automatic voltage regulator (AVR), and 5th-order salient-pole dq model of the synchronous machine. The PV inverter is modeled as 2-level 3-phase voltage source inverter (VSI) with LCL filter with resistive damping and grid interfacing delta-delta transformer. All the DERs utilize state machine-based control structures to ensure sequential operation of grid connection, ramping up/ramping down, ride-through, and participation in fault recovery efforts. The circuit breakers are also equipped with state machines, which simulate opening/closing actuation. The opening time of the breakers is set to three 60 Hz cycles + 20%, or 60 ms.

The model is simulated in Matlab/Simulink with the SimPowerSystems^{TM} blockset. The SimPowerSystems blockset synchronous machine does not have an accessible neutral point, so a zig-zag transformer was added to the output of the machine, forming a low impedance grounded system, both to provide a path for, and to limit, the ground fault current. Parameters for the genset and PV inverter can found in the Appendix.

Fault characterization is performed on the microgrid by applying Line-to-Line (LL) and Line-to-Ground (LG) faults at the locations shown in Fig. 5 without any protective features active. This implies 12 simulation runs to characterize the fault response of the microgrid at all the location, and further simulation runs will be needed to test and validate protection and ride-through settings for steps IV and V in Fig. 3. This leads to conflicting simulation requirements of:

1) small time-steps;
2) detailed DERs to capture control responses and filter dynamics;
3) potentially many DERs locations and microgrid configurations;
4) long run-times due to slow internal dynamics of synchronous machines;
5) many iterations to perform validation and verification throughout the design process.

To accelerate the simulation process and address these conflicting requirements, the model was compiled and executed on an OPAL-RT 5600 industrial pc in simulation-mode (non-real-time). The platform is controlled through a Python API to iterate through possible fault locations and types, and is also used to validate settings determined in Sections IV and V. For this work, LG faults were applied to phase a, and LL faults were applied to phase a and b.

Fig. 6 shows the per-unit (p.u.) rms currents measured at each relay location for LL faults at locations F4 and F6, and is plotted on inverse-time curves. Only phase b rms current (i_b) is plotted, since both phase a and b currents are similar. Likewise, Fig. 7 shows the rms of $3i_0$, where i_0 is the zero sequence current, measured at each relay location for LG faults. The generator relay (RGen) p.u. is the current rating of the generator, and the p.u. of the relays on the ring bus (R3-R6) and the PV relay (RPV) are the current rating of the ring bus/PV farm. i_0 was not plotted for RPV, as the transformer blocks the flow of zero sequence current. The curves are slightly offset for visibility.

The fault currents are dominated by the sub-transient and transient dynamics of the generator, while the PV farm contributes a little, almost negligible, fault current to the microgrid during LL faults. The fault current at F4 only flows from the left side of the ring bus through RGen and R4, while fault current at F6 flows in both directions, through the RGen-R4 path and through the RGen-R3-R5-R6 path. The cabling between the top and bottom parts of the ring bus are of similar but not exactly the same distances. This is why the fault current magnitudes at F6 through R3 and R4 are close but not exactly the same.

Because the fault current flows from two directions, directional sensing will be required for the protection scheme. Directional sensing is performed by monitoring an unfaulted voltage and one current measurement. For example, for a LL fault between phase a and b, the angle for forward direction (ϕ_f) was determined by comparing v_c and i_{ba} ($i_b - i_a$). For

TABLE III
VOLTAGE RIDE-THROUGH REQUIREMENTS FOR CONSECUTIVE TEMPORARY VOLTAGE DISTURBANCES (TABLE 17 IN [29])

Category	Max. number of ride-through disturbance sets	Min. time between successive disturbances (s)	Time window for new count of disturbance sets (min)
I	2	20	60
II	2	10	60
III	3	5	20

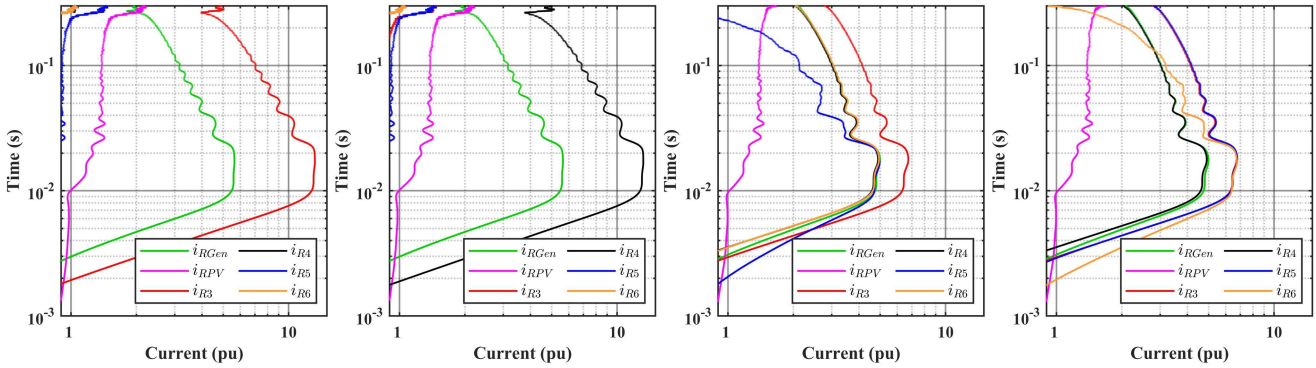


Fig. 6. Fault characterization showing Inverse-time curves for rms i_b current at locations (a) F3, (b) F4, (c) F5, and (d) F6.

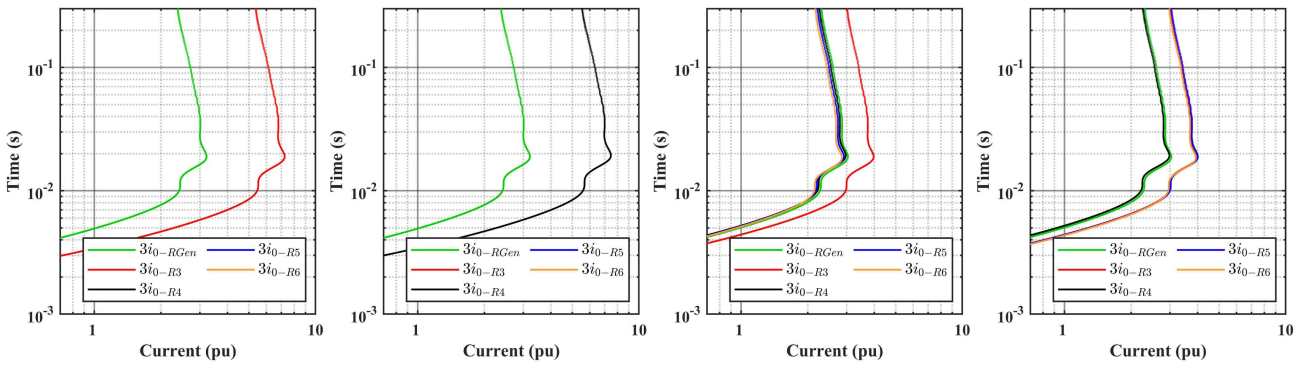


Fig. 7. Fault characterization showing Inverse-time curves for rms of $3i_0$ current at locations (a) F3, (b) F4, (c) F5, and (d) F6.

TABLE IV
COEFFICIENT OF POLYNOMIAL CURVE FIT

Coefficient	Value	Coefficient	Value
p_1	1.127e-06	p_4	–5.281e-03
p_2	–4.374e-05	p_5	0.02481
p_3	6.712e-04	p_6	0.9806

a LG fault occurring on phase a, the angle is determined by comparing v_{bc} and i_a. The forward zone of the relay is then $\phi_f \pm 90°$.

The reverse zone of the relay (ϕ_r) is 180° offset from ϕ_f. Fig. 8(a) shows characterization for LL faults, which will be used for Directional Over-current (DOC) relays. Fig. 8(b) characterizes the phase angle for LG faults to be used by Directional Earth Fault (DEF) relays. The forward zone is set to $0° \pm 90°$ for DOC relays and $-60° \pm 90°$ for DEF relays.

Lastly, inverter-based DERs can only ride-through to the extent to which the phased-locked loop (PLL) can maintain synchronization with the positive sequence voltage. Fig. 9(a) shows the voltage collapsing during a LL fault at F6. Positive sequence voltage was extracted in the stationary reference frame ($v^+_{\alpha\beta}$) using multiple second-order generalized integrators (MSOGI) presented in [45], and shown in Fig. 9(b). As $v^+_{\alpha\beta}$ approaches zero, the PLL no longer maintains synchronization, as no positive sequence voltage is present to synchronize with. The loss of synchronization is shown in Fig. 9(c) by the frequency going outside normal bounds around 310 ms after the fault.

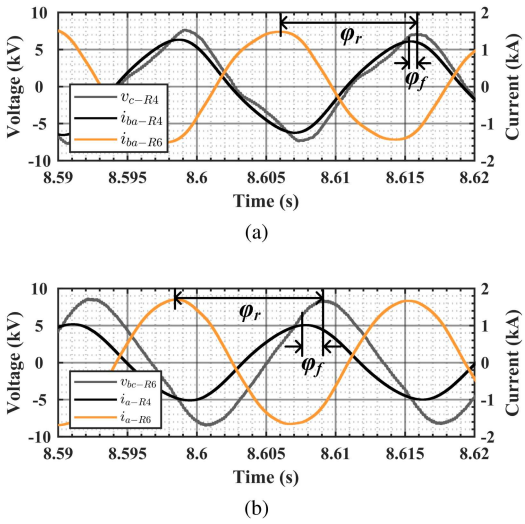


Fig. 8. Phase angle characterization for (a) LL and (b) LG faults at F6 location.

IV. Protective Relay Design

Following the fault transient characterization, the protection design can be performed (step IV). IEC 60255 standard inverse (SI) curves were used for current-time calculations for the DOC and DEF relay settings, where the SI curves are governed by [32]:

$$t = TMS\frac{0.14}{(I/I_s)^{0.02}-1} \tag{1}$$

where TMS is Time Multiplier Setting, I is the rms current in p.u., and I_s is the pick up current in p.u.

The curves where adjusted to account for the 60 ms opening time of the breaks. The forward direction assumes current is flowing from left to right of the microgrid. R3 and R4 are set to operate in the forward direction, and R5 and R6 are set to operate in the reverse direction. As the magnitudes of fault current at F3 and F4 were similar, the settings of R3 and R4 are assumed to be the same, and similarly with R5 and R6. However, as there is only one source fault current that can flow through parallel branches, some subtleties need to be considered in the coordination of relay settings. If the settings of R4 and R6 are set at the same levels and a fault occurs at F6, then not only will R4 and R6 trip, but also R3 will trip due to the secondary fault current path of RGen-R3-R5-R6. R5 would not trip, as the fault current at F6 would be in the forward direction. Additionally, if a fault occurred at F5, not only R3 and R5 trip, but also R4. Because of this, settings for R3/R4 were increased sufficiently to allow for R5/R6 to trip, the breakers to open, with some additional margin, as the rms calculation takes half to one cycle to update.

For faults at F3/F4, R3/R4 would trip, causing the fault current to flow around the ring bus through the opposite branch, subsequently tripping R5/R6. Lastly, RGen is set above R3/R4 to ensure it does not trip while the breakers of F3/F4 are opening.

Fig. 10 shows the logic implemented for DOC and DEF relays to account for magnitude and direction. The final settings are tabulated in Table I. The pickup current for DEF was set to 0.15 p.u. of rated current, as sufficient zero sequence current is only present under fault conditions. The pick up currents for DOC relays were all set to 1.15 p.u.

Figs. 11 and 12 show fault currents overlayed with the relay's time-trip curves and the relay's trip signals for each fault location for LL and LG faults, respectively. The relay's trip signal go high after the trip conditions are met, and are color coded to match the relay measurements and time-trip curves. As can be seen in the figures, both the protection settings and the direction conditions correspond to the correct set of relays to trip, according to associated fault location and fault type.

For example, Fig. 11(d) shows the R6 trip signal going high shortly after the fault current intersects the time-trip curve for LL fault at F6. Then after the breaker opens, the current stops flowing through R3-R5-R6 path and the current increases in the R4 path, causing the R4 relay to correctly trip. Fig. 11(c) shows the same behavior but with the R5/R3 relays at F5. Likewise, similar behavior is seen in Fig. 11(a) and Fig. 11(b), but with the R3/R4 relays tripping first, then R5/R6 relays. Similar behavior occurs for LG faults throughout Fig. 12.

V. Low Voltage Ride-Through Settings

With the protection setting implemented, LVRT settings can be selected and tested (step V). Fig. 13 shows the RMS voltage in p.u. for the genset and PV while the protection scheme is isolating the fault, and is plotted against IEEE Standard 1547-2018 lower limit lines. RMS was shown to be accurate compared to other peak detection methods in the presence of harmonics, specifically when used for the voltage abnormalities in IEEE Standard 1547-2018 [46]. The voltage response is shown for an LL fault at F4, since LL faults have the lower transient voltages and faults at F3/F4 have longer relay trip times.

A. Discussion on IEEE Standard 1547-2018

The assumption that the DERs must trip if the voltage falls below the limit is understandable from an initial read-through of IEEE Standard 1547-2018 [29], but careful understanding of the terminology and examination of the footnotes are required. Category (Cat.) I and category II ride-through have lower limits lines of 0.5 p.u. and 0.3 p.u., respectively. The standard recommends "Cease to Energize" if voltage falls below the lower limit. Category III (Table II) also has a lower limit line of 0.5 pu, but recommends momentary cessation (mc) with a minimum ride-through time of 1 s. "Cease to Energize" can be misleading as "*This does not necessarily imply disconnection, isolation, or a trip of the DER. This may include momentary cessation or trip*," while momentary cessation is to "*Temporarily cease to energize an EPS,... with the capability of immediate Restore Output of operation when the applicable voltages and the system frequency return to within defined ranges*." [29].

Because the voltage levels dip below the limit lines for all three categories, momentary cessation should be considered. Momentary cessation is not possible for the genset as the fault current from the genset is used for the fault location, and the system would go dark. Momentary cessation is possible for the PV farm as it does not contribute to fault current used for fault location, but is not required. However, it seems wasteful for the

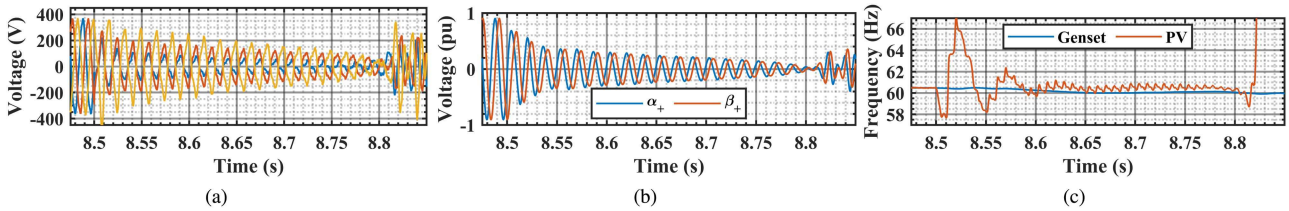


Fig. 9. LL fault at F6: (a) PV v_{abc}, (b) $v^{+}_{\alpha\beta}$, and (c) frequency.

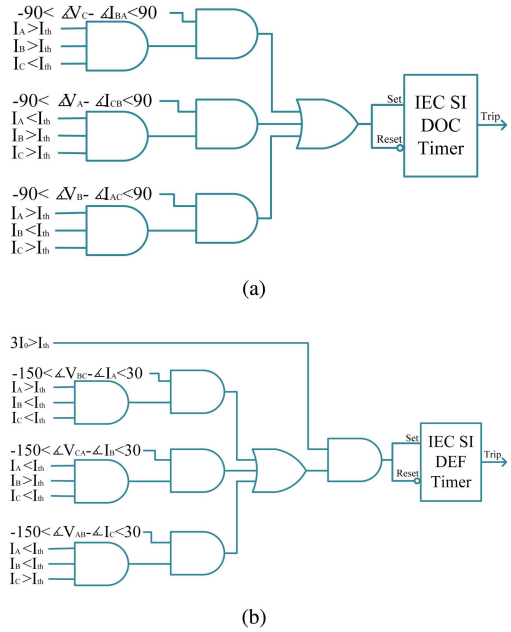


Fig. 10. Relay trip logic: (a) DOC and (b) DEF.

PV farm to continue to output power into a fault without benefit to the system. Also, momentary cessation would reduce thermal stress on the power electronics during overcurrent condition induced during the fault.

For the PV farm, momentary cessation would imply temporary stop to gating of the power electronic system, which can easily be implied. The allowable time for momentary cessation is not specified, and for this work is assumed to be the time listed in category III minimum ride-through time for 1 s, but can be extended if needed.

B. Enabling Controls and State Machines

To enable the momentary cessation functionality for the VSI, a series of state machines and control logic were implemented to ensure proper operation under LVRT. Fig. 14 shows a top-level view of different state machines, and their interaction with the grid-following controller. The controller consists of a system state machine, ramping state machine, VSI grid-following controls (Fig. 16), LVRT state machines (Fig. 15), and fault manager. The controller also has supporting signal processing functions such as RMS in the power meter, MSOGI-based PLL [45] to extract the positive sequence voltage and remain synchronized fault conditions fault conditions, sine pulse-width modulation (SPWM) with 3 rd harmonic injection, and dq/inverse dq transforms.

The system state machine contains states of OFFLINE, STANDY, ONLINE, and FAULT. The system state machine is initialized by the ac-side circuit breaker closing, and transitions from STANDY to ONLINE when the user starts the VSI. The ramping state machine contains states of OFFLINE, RAMPING UP, RAMPED UP, RAMPING DOWN, and RIDE-THROUGH. Once the system state machine is ONLINE, the ramping state machine transitions from OFFLINE to RAMPING UP. This state ramps up the command reference to the PI controls (in this case i_d^*) until its rated value (1 p.u.), and then transitions to RAMPED UP.

Additionally, an enable signal is sent to the PI controller and to the SPWM subsystems. This enable signal is high in RAMPING UP, RAMPED UP, RAMPING DOWN states and low in OFFLINE and RIDE-THROUGH states. Within the inner-current loop controller, the enable signal is fed each individual PI controller.

The structure of the PI is shown in Fig. 17. An integrator breaks down into an accumulator that is multiplied by the update rate of the controller and the integration gain. The integrator has logic where if the upper or lower saturation limits of the PI controller output are reached, integration action will be disabled, but upon re-enabling, will resume the at the pre-disabled value, i.e., pausing integration until the controller output returns to unsaturated condition. Additionally, if the enable signal is low, the integration action will be disabled and the integral value will be cleared. So, upon re-enabling, the integral value will be zero.

The LVRT state machine is shown in Fig. 15. The enable signal from the ramping state machine also transitions the LVRT state machine from OFFLINE to ONLINE. IEEE Standard 1547-2018 specifies the lowestRMS voltage phase should be taken into account, so a state machine is implemented for each phase. The output flags from each phase's state machine are OR'ed as well.

In the presence of voltage abnormalities, the ONLINE state transitions to LVRT state. If the rms voltage goes below 0.5 p.u., the state machine transitions to MOMENTARY CESSATION (MC) state. In this state, the ride-through flag is raised and sent to the ramping state machine. This causes the ramping state machine to transition to RIDE-THROUGH state. The RIDE-THROUGH state changes the enable signal that goes to the SPWM and the inner current loop controller to low, which stops PWM signals and clearing out integration terms in PI controllers.

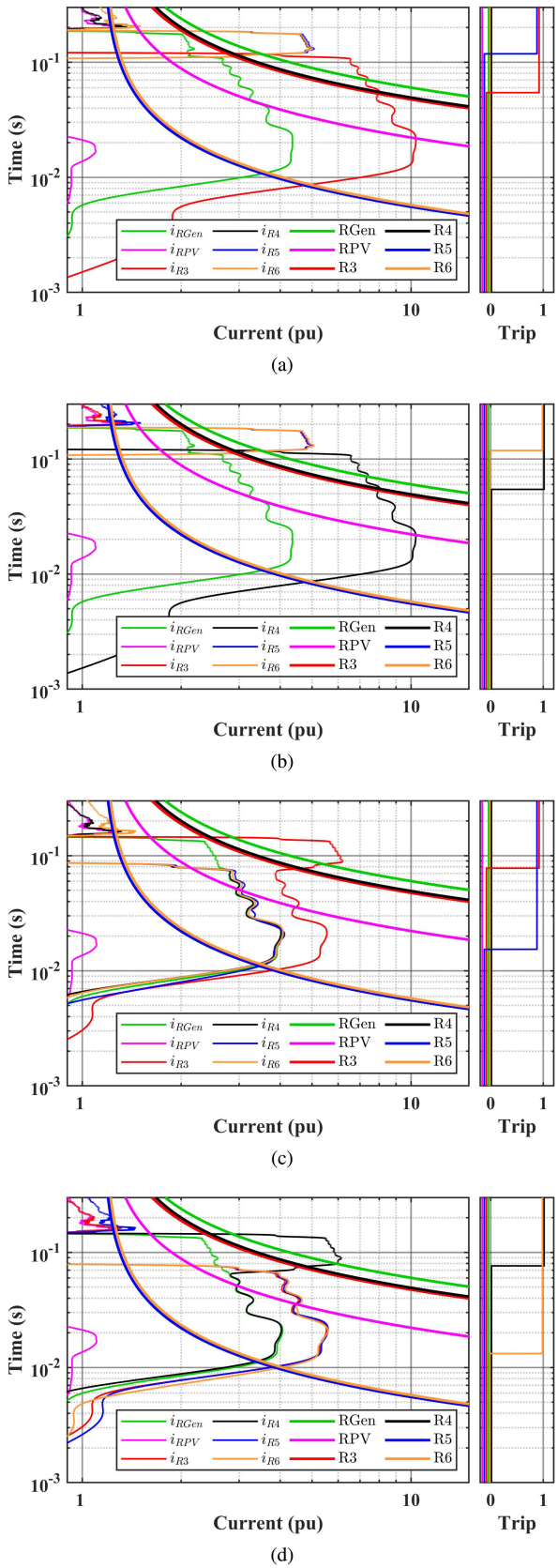


Fig. 11. Inverse-times curves of rms i_b current with DOC relay settings (left) and relay trip signals (right) at locations: (a) F3, (b) F4, (c) F5, and (d) F6.

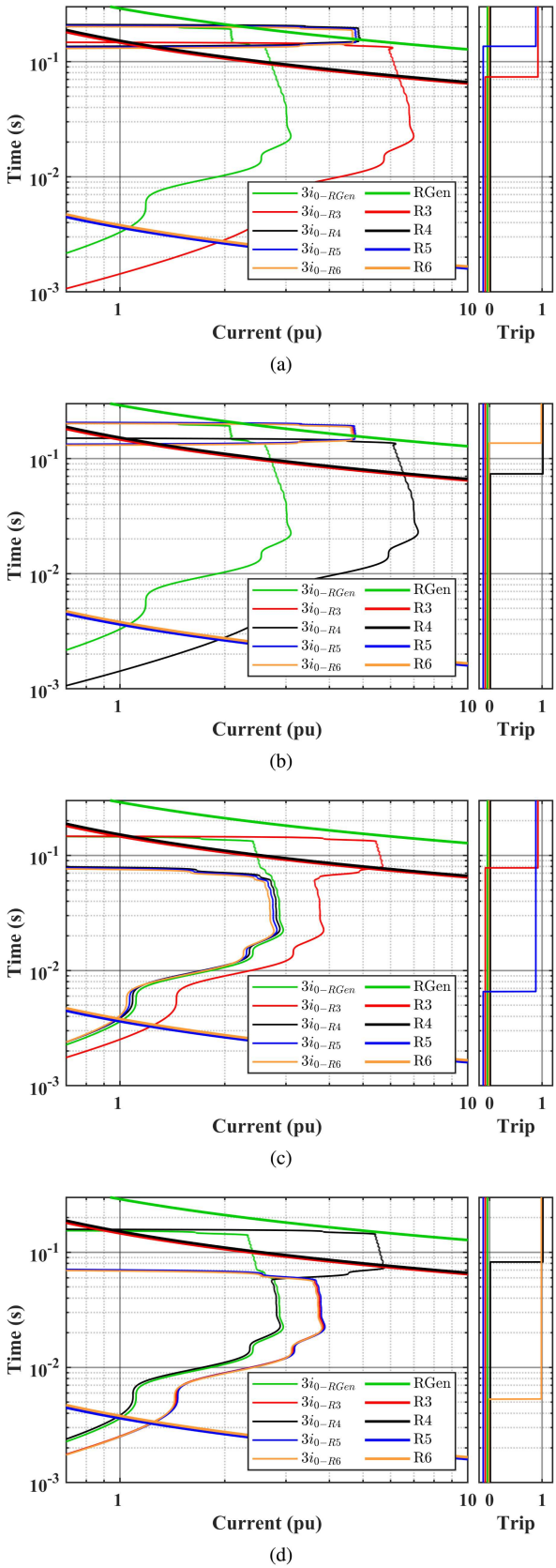


Fig. 12. Inverse-times curves of rms $3i_0$ current with DEF relay settings (left) and relay trip signals (right) at locations: (a) F3, (b) F4, (c) F5, and (d) F6.

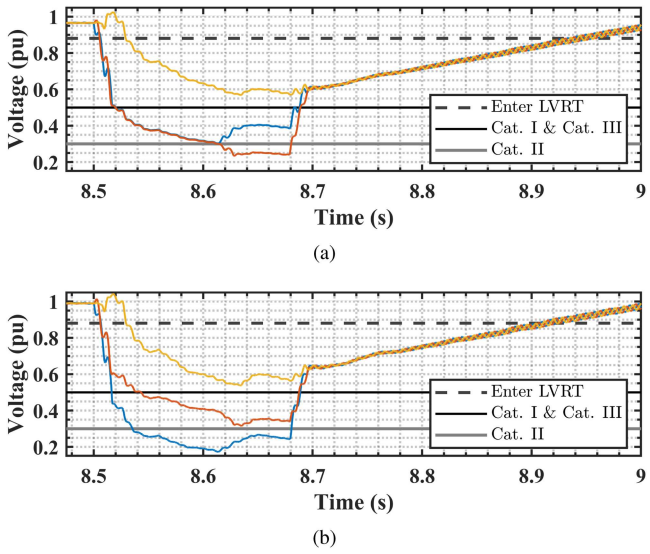


Fig. 13. RMS p.u. voltage during FDIR process against IEEE Standard 1547-2018 lower limits across all 3 categories for: (a) genset and (b) PV.

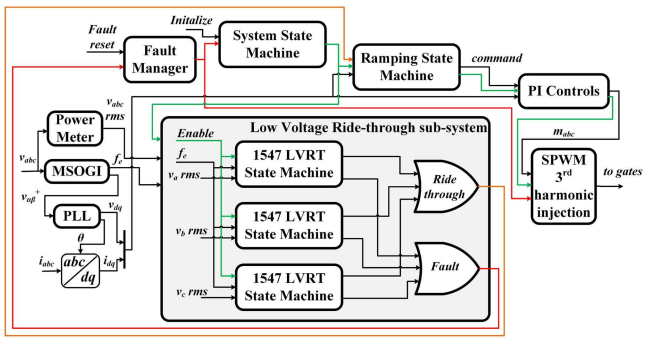


Fig. 14. Top-level control block diagram for grid-following VSI.

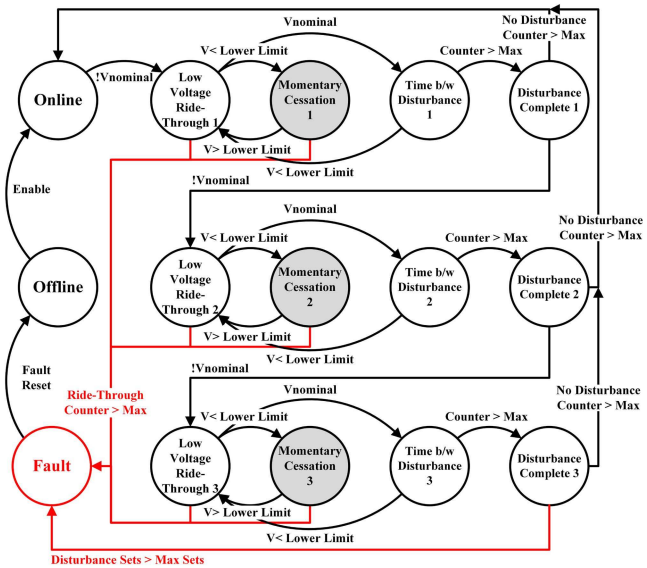


Fig. 15. IEEE Standard 1547-2018 Low Voltage ride-through state machine.

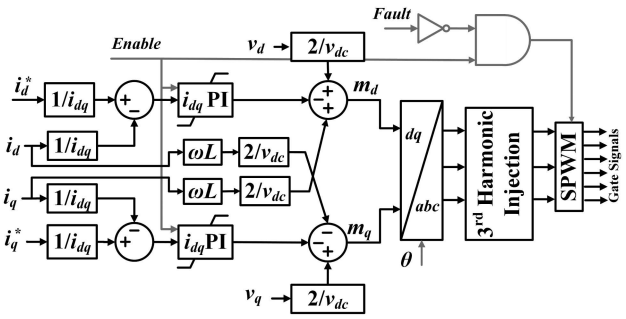


Fig. 16. VSI grid-following controls (inner current loop).

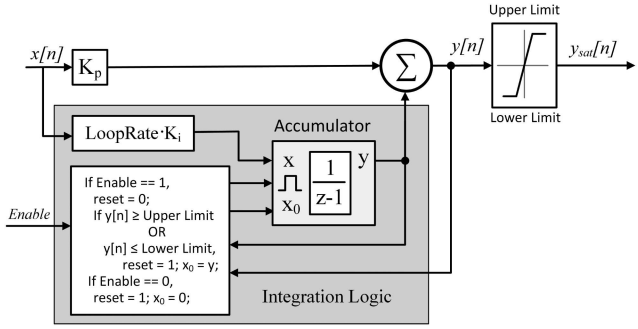


Fig. 17. PI with clamping integrator and enable reset.

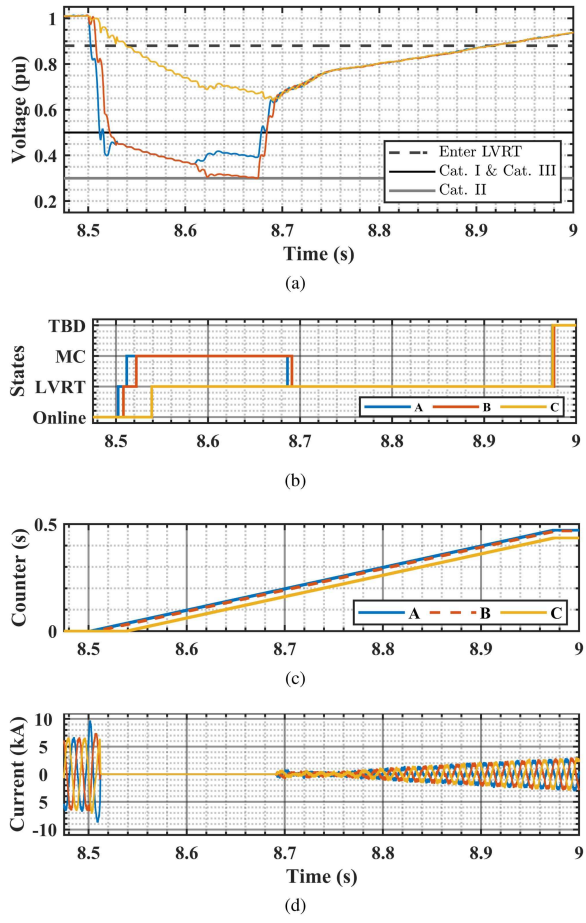


Fig. 18. PV category III LVRT state machine: (a) v_{abc} rms pu, (b) states, (c) counter, and (d) i_{abc}.

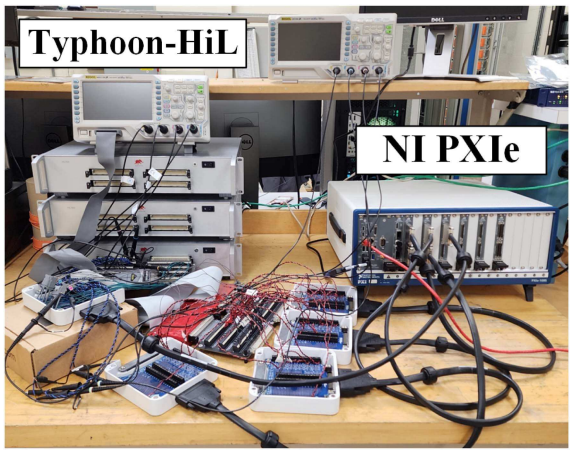


Fig. 19. CHiL setup.

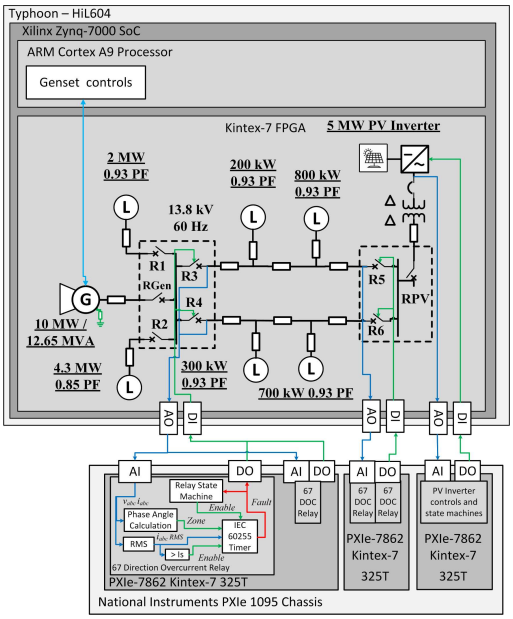


Fig. 20. Diagram of CHiL setup.

If the voltage returns above some threshold and frequency is within an acceptable range, set to 0.55 p.u. rms voltage and between 55 and 65 Hz, respectively, the LVRT state machine transitions from the MC state to the LVRT state. The ride-through flag becomes low, and the ramping state machine transitions from RIDE-THROUGH to RAMPING UP. The enable signals to SPWM and the inner current loop controls returns to high, and the VSI resumes outputting power. If the integrator terms within the PI controllers were not cleared during RIDE-THROUGH, upon return out of MC state, poor transient performance may be exhibited by the VSI due to accumulated errors without actuation.

The remaining structure of the LVRT state machine is governed by the requirements in Table 17 in (copied as Table III for conveniences) Section 6.4.2.5 of [29], which specifies requirements of *ride-through of consecutive voltage disturbances*. Some terms in this table should be defined. A *disturbance period* is defined by [29] as "*the range of time during which the applicable voltage or the system frequency is outside the continuous operation region.*" A *disturbances set* can be thought of as the set voltage abnormalities within one disturbance period. Column 2 in Table 17 list the maximum number of disturbances set allowed before disconnection, 3 for category III. Column 3 in Table 17 specifies the amount of time that should pass between successive disturbances for the ride-through time within a disturbance period to reset, 5 s for category III. A disturbance after this time would count as a new disturbance set. Lastly, Column 4 specifies the amount of needed between disturbances sets to reset the number of ride-through disturbances set. For category III, this is 20 minutes.

Thus, 3 counters are required, one for the time within a ride-through disturbance, one for the time between successive disturbance sets to determine the next disturbance set, and one for the time in nominal operation to determine a new count of disturbance sets.

Due to the consecutive disturbance requirement, the state TIME BETWEEN DISTURBANCE (TBD) was made as an intermediary state on the way to DISTURBANCE COMPLETE I. The state machine transitions from LVRT state to TBD state when the rms p.u. voltage returns within the normal range. In the TBD state, the ride-through disturbance time counter is paused and the time between disturbance set counter is started. If the voltage goes off-nominal while in the TBD state, the state machine will transition back to the LVRT state, the ride-through disturbance time counter will resume, and the time between disturbance set counter will be reset. If the voltage remains in nominal condition while in TBD state long enough for the time between disturbance set counter to reach 5 s, the LVRT state machine transitions to DISTURBANCE COMPLETE I, where the ride-through disturbance time counter and time between disturbance set counter are both reset. If 20 minutes are reached in nominal operation while in DISTURBANCE COMPLETE I, the state machines transitions back to ONLINE and the time in nominal operation counter is cleared. If a voltage abnormality is detected while in DISTURBANCE COMPLETE I, the state machine transitions to LVRT II state, and the process is continued.

C. Offline Simulation Results

Fig. 18 shows the PV performance using category III ride-through as the state machines for each phase cycle through different states in response to the voltage abnormality. The PV can be seen entering and leaving the Momentary Cessation state in Fig. 18(b) and the output current is reducing in Fig. 18(d) on the low voltage side of the transformer, while the protection system isolates an LL fault at F4. The remaining current is from the interaction between the microgrid's distribution system and the LCL filter. The protection system isolates the fault (T_{fi}) around 200 ms after fault inception and recovers from the fault (T_{fr}) around 480 ms.

VI. CHiL Implementation & Validation

Fig. 19 shows a picture of the CHiL setup and Fig. 20 shows a block diagram of the setup. The real-time emulation

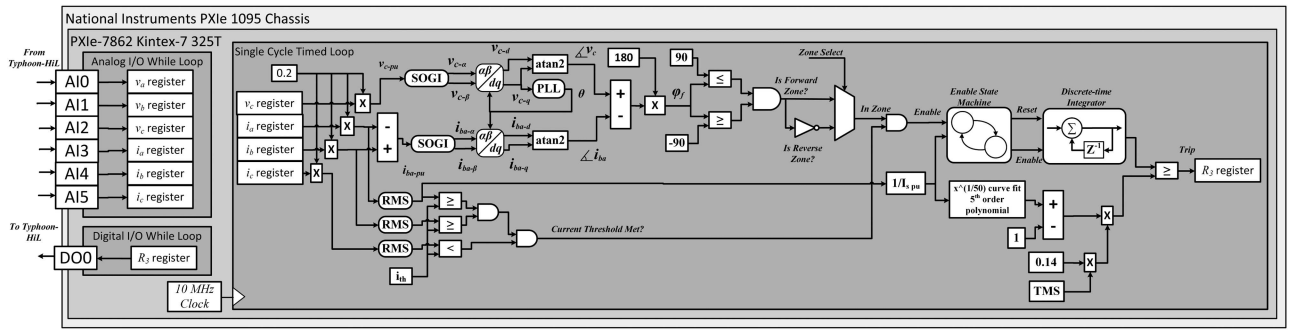


Fig. 21. Directional Overcurrent relay implementation in LabVIEW FPGA.

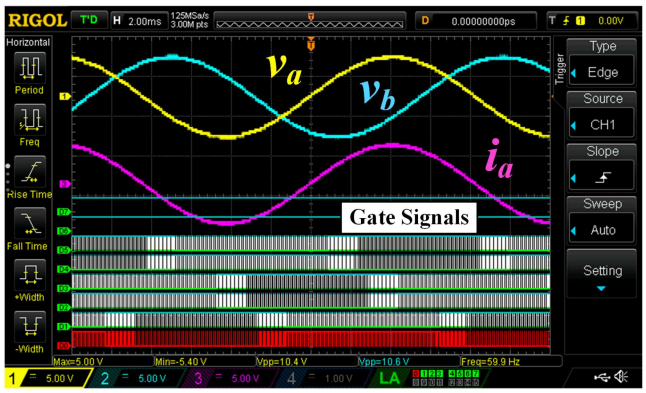


Fig. 22. Grid-following VSI in steady state in CHiL. Ch 1-3: v_{ab} and i_a, respectively, from VSI, 5 v = 1 p.u. Logic Analyzer (LA) signals show PWM gate signals to Typhoon-HiL.

of the islanded microgrid in Fig. 5 is executed on Typhoon-HiL 604. The logic for the DOC relays and grid-following controls for the VSI were implemented on National Instruments (NI) field programmable gate array (FPGA) based hardware. The PXIe-7862 modules contain Kintex-7 325t FPGAs and analog and digital I/O (PXIe standard for PCIe eXtensions for Instrumentation, where PCIe is Peripheral Component Interconnect Express). The modules are enclosed in PXIe-1095 chassis. The LabVIEW FPGA software is used to generate the HDL (hardware description language) code for the modules. Current and voltage measurements from the relays and VSI are fed from Typhoon-HiL to the NI FPGA modules. Digital signals for the circuit breaker and VSI switches are fed from the NI FPGA modules to Typhoon-HiL.

Fig. 21 shows the FPGA implementation of a DOC relay for LLab fault detection and coordination. Analog inputs are saved to registers, which are used for crossing clock domains between the analog input while loop, and the single-cycle timed loop (SCTL). SCTLs are used to ensure logic is compiled to make timing. The signals v_c and i_{ba} are fed to the single-phase SOGI to generate the quadrature components, $v_{c-\alpha\beta}$ and $i_{ba-\alpha\beta}$, respectively. The voltage $v_{c-\alpha\beta}$ is fed to a phase-locked loop (PLL) to generate v_{c-dq} and the phase angle, θ. The phase angle from the PLL is fed to the dq transform for $i_{ba-\alpha\beta}$ to generate i_{ba-dq}. v_{c-dq} and i_{ba-dq} are fed to ATAN2 (four quadrant arc tangent) functions to get the angles, $\angle v_c$ and $\angle i_{ba}$, respectively. Lastly, the phase angle ϕ_f is formed by subtracting $\angle i_{ba}$ from $\angle v_c$. The phase angle ϕ_f is the same phase angle used to determine forward and reverse zones in Fig. 10(a).

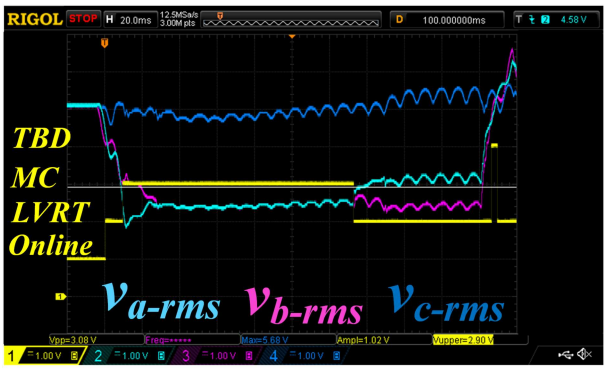
If the rms fault current thresholds are met and the phase angle is in the correct zone, a timer is activated. The IEC 60255 SI equation is a function of fault current and outputs the trip time (see (1)). If the timer is greater than the trip time calculated by (1), then the trip signal is high and a signal is sent to the breaker to open.

An unexpected implementation challenge for the DOC relay was implementing the 50th square root in the (1) for the IEC 60255 SI equation. Ultimately, a 5th-order curve fit was implemented. The form of the polynomial is shown in (2), and the coefficients are shown in Table IV.

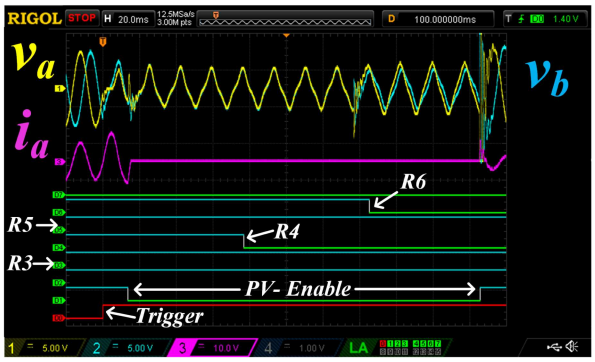
$$p_1x^5 + p_2x^4 + p_3x^3 + p_4x^2 + p_5x + p_6 \tag{2}$$

To validate the simulation results presented in Section V-C, LLab faults were applied at F4 and F5 at time t=0, while the microgrid was operating at steady state. The steady state pre-fault waveforms are shown in Fig. 22 for the grid-following VSI. The control system shown in Fig. 14 was implemented in LabVIEW FPGA for the VSI.

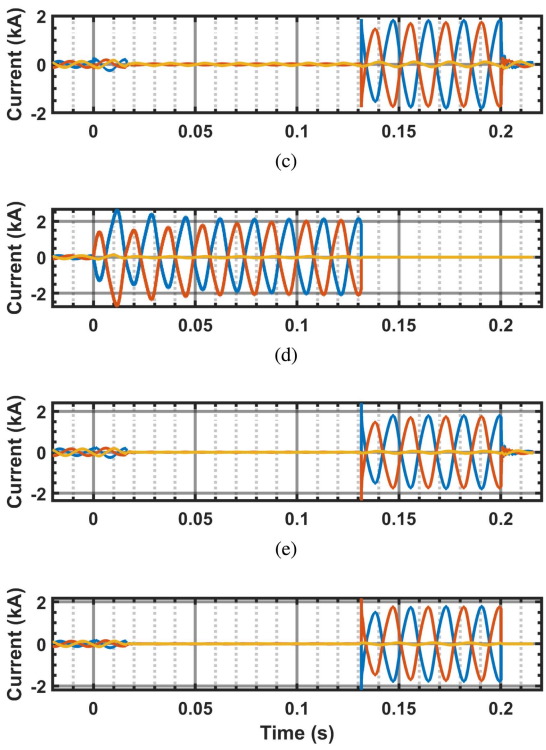
The waveforms after the LLab fault is applied for F4 and F5 locations are shown in Figs. 23 and 24, respectively. Fig. 23 demonstrates the fault detection, isolation of the fault branch, and voltage recovery of the system. Fig. 23(a) shows the rms voltages the controller is calculating and the LVRT state machine cycling through different states in response to the voltage transient. Fig. 23(b) shows the transient phase a and b voltage and phase current from the VSI. It also shows the different relay signals and the enable signal to the VSI. As the fault causes the system voltage to reduce, the LVRT state machine go to LVRT state. As the voltage reduces further, the LVRT state machine transitions to MC state, and PV gating is disabled. R4 and R6 relay signals can be seen coordinating in similar fashion to Fig. 11(b). The three phase current at R3–R6 were recorded at 100 k samples per seconds with Typhoon-HiL, and can be seen in Fig. 23(c), (d), (e), and (f). No current can be seen following between R4 and R6, showing that the correct branch was isolated. Once the R4 and R6 breakers open, the rms and transient voltages can be seen recovering, during which, the VSI can be seen re-enabled and able to supply output power. Note



(a)

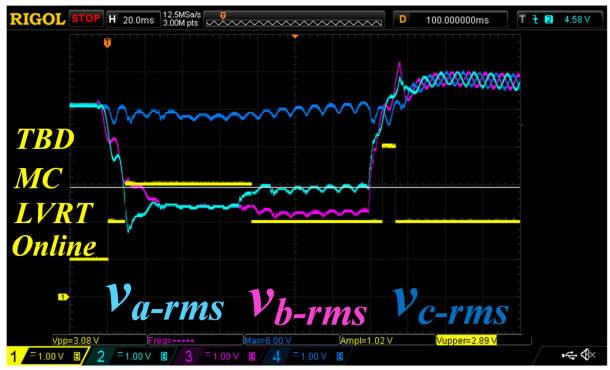


(b)

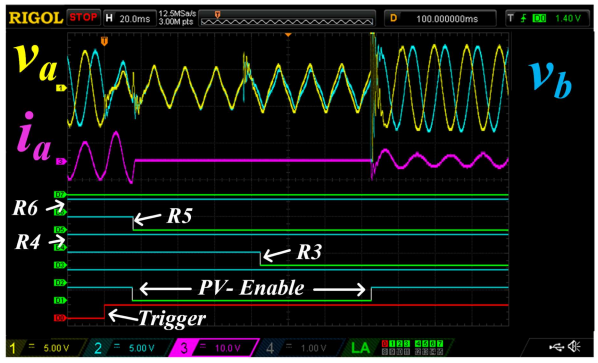


(c) (d) (e) (f)

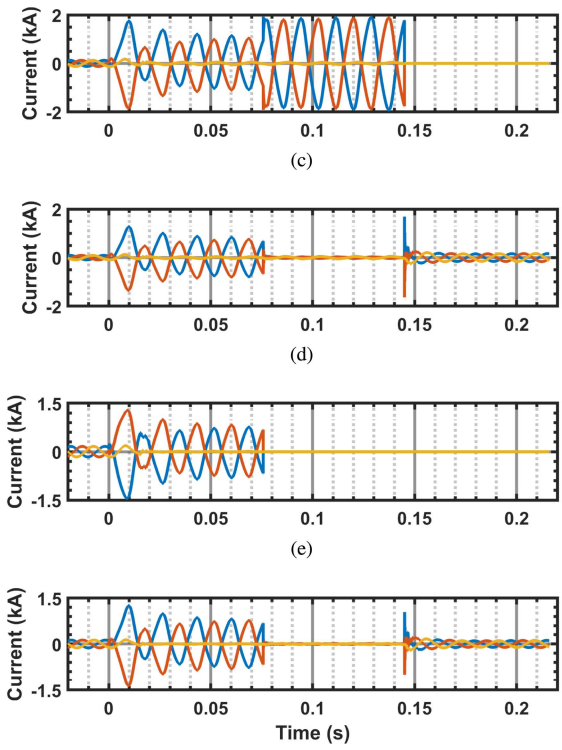
Fig. 23. Fault 4 LLab applied in CHiL system: (a) Measurements from the VSI controller Ch 1: LVRT State machine states for phase A. 1 v per state; Ch 2-4: v_{abc} rms at PV, respectively, 5 v = 1 p.u. (b) Ch 1-3: v_{ab} and i_a, respectively, from VSI, 5 v = 1 p.u. i_{abc} data-logged from Typhoon-HiL from (c) R3, (d) R4, (e) R5, and (f) R6.



(a)



(b)



(c) (d) (e) (f)

Fig. 24. Fault 4 LLab applied in CHiL system: (a) Measurements from the VSI controller Ch 1: LVRT State machine states phase A. 1 v per state; Ch 2-4: v_{abc} rms at PV, respectively, 5 v = 1 p.u. (b) Ch 1-3: v_{ab} and i_a, respectively, from VSI, 5 v = 1 p.u. i_{abc} data-logged from Typhoon-HiL from (c) R3, (d) R4, (e) R5, and (f) R6.

that although the phase A rms voltage is above the threshold to return to LVRT state after the R4 breaker opens, phase B is still below the threshold and thus in MC state, although not shown on the oscilloscope.

Similar results of successful fault detection, isolation, and recovery can be seen in Fig. 24 as a LLab is applied to the F5 location. Note that on voltage recovery, the system voltage goes above 1.2 p.u. This is likely due to the PI controller in the genset's AVR. For this reason the high voltage ride-through was increased to avoid the controller faulting. This is why the LVRT state machine transitions back to LVRT from TBD. Eventually, the system voltage does return to nominal conditions and the LVRT state machine transitions to TBD, and then to DISTURBANCE COMPLETE 1. Lastly, the TMS relay settings on R3/R4 had to be increased from 0.015 to 0.02 to achieve successful coordination. The increase in the TMS is most likely due to differences in the AVR controls between Typhoon and the offline MATLAB/Simulink model, where differences in the AVR controls affect the fault current levels.

VII. Conclusion and Future Work

This work introduces a novel step-by-step methodology to design and validate protection settings in distribution equipment and ride-through settings in DERs. The design process was demonstrated successfully on an islanded ac microgrid with a ring-bus structure with both inverter-based and synchronous generator-based DERs. The design process can also be applied to microgrid with different DERs and distribution systems, and in grid-connected systems.

OPAL-RT was used to improve simulation run-time of offline Matlab/Simulink models in steps III-V, as shown in Fig. 3. To further validate the settings, the microgrid model was executed in real-time CHiL simulation with Typhoon-HiL for the real-time microgrid emulation and NI-based FPGA hardware for the real-time controls for the DOC protection and the grid-following VSI. The details of protection coordination for the microgrid and the implementation and operation of enabling ride-through controls for inverter-based DERs were also discussed.

Additionally, this work shows that for islanded microgrids, where the voltage transients during faults can be significant, LVRT settings may need to be increased to category III ride-through and may need to include momentary cessation operation into the controls.

By having more DERs connected in post-fault recovery, as a result of proper coordination of protection and ride-through settings, microgrid recoverability is improved. This improvement is manifested by increased instantaneous performance after fault recovery (P_r), and will lead to reduced time to fully restore the system, thereby minimizing loss of EPS service.

This work has laid the groundwork for application of a novel protection design methodology to improve microgrid resilience by demonstrating the process and base-lining fault response performance using real-time simulations of the EPS and FPGA-based execution of protection mechanisms and feedback control on a CHiL platform.

By improving different attributes of microgrid survivability (susceptibility, vulnerability, autonomous recovery), we are directly improving overall resilience of the microgrid, i.e., how the microgrid responds to and recovers from off-nominal events. Thus, by ensuring recovery, we ensure a survivable, and therefore, a resilience microgrid to electrical faults. As a result, it is concluded that utilizing the proposed novel protection design methodology will improve the microgrid's resilience.

Future work will derive the key performance parameters and technical performance measures by which the baselined microgrid and future improvements can be definitively quantified. Possible improvements are those discussed in Section II:

- a redundant feeder between PV and genset switchgears;
- increasing number of switchgear to minimize the isolated branches;
- changing the number, location, and size of the gensets throughout the microgrid to be more decentralized and distributed;
- addition of BESS in the microgrid;
- more advance protection schemes like differential protection, adaptive protective, or emerging machine learning-based approaches;
- advanced control schemes, such as non-linear controls, that may improve fault recovery.

The protection design process methodology will help reduce design time for these prospective improvements, as each design must have proper coordinated protection and ride-through settings to enable evaluation. With proper settings, microgrid resilience attributes can be extracted.

Future work will bench-mark the architectural, protection, and control changes against the baseline microgrid, which enables traceability of technology insertion at the design-level to system-level resilience attributes. Different improvements in the microgrid will affect different aspects of microgrid survivability, and thus, resilience attributes. For example, improving detection time (t_f to t_{df}) of the protection equipment helps to reduce the time spend in a degraded state. Improving the controls of the DERs may help post-fault recovery time ($t_{fi}$to t_{fr}). Increasing the locations of switchgear can help to minimize which loads get disconnected, increasing (P_r), but may also increase circuit breaker coordination time to prevent premature tripping of upstream breakers (increasing t_f to t_{df}). Decentralizing the DER locations can help to improve the susceptibility by minimizing impact of loss of grid-forming capable DERs, but can increase protection coordination time from multiple fault current path and requiring more complex protection schemes. Ultimately, the microgrid stake-holders decide which improvement to pursue given budgetary constraints.

Appendix

Tables V and VI list out parameters used in the microgrid simulation.

TABLE V
CABLE IMPEDANCES

Symbol	R $[m\Omega]$	L $[\mu H]$	Symbol	R $[m\Omega]$	L $[\mu H]$
Z_{Gen}	8	12.6	Z_{34}	11	17
Z_{PV}	175	273	Z_{35}	54	84
Z_1	404	637	Z_{41}	487	763
Z_2	184	288	Z_{42}	211	331
Z_{31}	368	576	Z_{43}	175	274
Z_{32}	92	144	Z_{44}	16	25
Z_{33}	175	274a	Z_{45}	161	25

TABLE VI
GENSET AND PV INVERTER PARAMETERS

Parameter	Value
Genset	
Apparent power rating	8.65 MVA
Voltage	13.8 kV
Power factor	0.79
Electrical frequency	60 Hz
Pole pairs	4
Stator leakage reactance	0.0014 p.u.
Stator reactance	0.0144 p.u.
Stator resistance	1.81 p.u.
d-axis synchronous reactance	1.81 p.u.
q-axis synchronous reactance	1.76 p.u.
d-axis transient reactance	0.3 p.u.
d-axis subtransient reactance	0.23 p.u.
q-axis subtransient reactance	0.25 p.u.
d-axis open-circuit transient time-constant	1 s
d-axis open-circuit subtransient time-constant	0.07 s
q-axis open-circuit subtransient time-constant	0.03 s
Zero-sequence grounding resistance	0.41 p.u.
Zero-sequence grounding reactance	0.24 p.u.
PV Inverter	
Power rating	3.5 MW
Power factor	0.9
Voltage rating	480 V
Switching frequency	3125
Converter-side inductor	0.256 p.u.
Differential-mode capacitor	0.078 p.u.
Damping resistor	0.17 Ω
Grid-side inductor	0.077 p.u.
PV Interfacing-Transformer	
Apparent power rating	3.89 MVA
Primary-side voltage	13.8 kV
Secondary-side voltage	480 V
Impedance	0.06 p.u.

REFERENCES

[1] Naval Facilities Engineering Command, "P-602 Three Pillars of Energy Security (Reliability, Resilience, & Efficiency)," 2021. [Online]. Available: https://www.wbdg.org/FFC/NAVFAC/PPUBB/P-602 rev2.pdf

[2] U.S. Department of Energy, "DOE Climate Adaptation and Resilience Plan," 2022. [Online]. Available: https://www.energy.gov/sites/default/files/2022-03/DOEClimateAdaptationandResiliencePlan.pdf

[3] U.S. Department of Energy Office of Energy Policy and Systems Analysis, "Climate Change and the electricity sector guide for climate change resilience planning," U.S. Department of Energy, Washington, DC, USA, 2016.

[4] Office of the Under Secretary of Defense for Acquisition and Sustainment, "FY22 annual energy performance, resilience, and readiness report," Department of Defence, Tech. Rep. 5-9BB3EEF, 2023.

[5] M. Panteli, P. Mancarella, D. N. Trakas, E. Kyriakides, and N. D. Hatziargyriou, "Metrics and quantification of operational and infrastructure resilience in power systems," *IEEE Trans. Power Syst.*, vol. 32, no. 6, pp. 4732–4742, Nov. 2017.

[6] E. Hossain, S. Roy, N. Mohammad, N. Nawar, and D. R. Dipta, "Metrics and enhancement strategies for grid resilience and reliability during natural disasters," *Appl. Energy*, vol. 290, 2021, Art. no. 116709.

[7] Y. Chi, Y. Xu, C. Hu, and S. Feng, "A state-of-the-art literature survey of power distribution system resilience assessment," in *Proc. IEEE Power Energy Soc. Gen. Meeting*, 2018, pp. 1–5.

[8] A. Stankovic, "The definition and quantification of resilience," IEEE PES Ind. Tech. Support Task Force, Piscataway, NJ, USA, Tech. Rep. PES-TR65, 2018.

[9] E. D. Vugrin, A. R. Castillo, and C. A. Silva-Monroy, "Resilience metrics for the electric power system: A performance-based approach." Sandia Nat. Lab., Albuquerque, NM, USA, Tech. Rep. SAND2017-1493, 2017.

[10] E. L. Hotchkiss and A. Dane, "Resilience roadmap: A collaborative approach to multi-jurisdictional resilience planning," Nat. Renewable Energy Lab., Golden, CO, USA, Tech. Rep. NREL/TP-6A20-73509, 2019.

[11] R. Francis and B. Bekera, "A metric and frameworks for resilience analysis of engineered and infrastructure systems," *Rel. Eng. Syst. Saf.*, vol. 121, pp. 90–103, 2014.

[12] K. H. Anderson, E. L. Hotchkiss, L. Myers, and S. R. Stout, "Energy resilience assessment methodology," Nat. Renewable Energy Lab., Golden, CO, USA, Tech. Rep. NREL/TP-7A40-74983, 2019. [Online]. Available: https://www.osti.gov/biblio/1573210

[13] R. E. Giachetti, D. L. V. Bossuyt, W. W. Anderson, and G. Oriti, "Resilience and cost trade space for microgrids on islands," *IEEE Syst. J.*, vol. 16, no. 3, pp. 3939–3949, Sep. 2022.

[14] C. Peterson, D. Van Bossuyt, R. Giachetti, and G. Oriti, "Analyzing mission impact of military installations microgrid for resilience," *Systems*, vol. 9, 2021, Art. no. 69.

[15] S. Ericson, N. Grue, E. Hotchkiss, and M. Brown, "Applications of measuring and valuing resilience in energy systems," Nat. Renewable Energy Lab., Golden, CO, USA, Tech. Rep. NREL/TP-5R00-83841, 2023.

[16] M. Hamidieh and M. Ghassemi, "Microgrids and resilience: A review," *IEEE Access*, vol. 10, pp. 106059–106080, 2022.

[17] E. Blem, J. Menon, and K. Sankaralingam, "Power struggles: Revisiting the RISC vs. CISC debate on contemporary arm and x86 architectures," in *Proc. IEEE 19th Int. Symp. High Perform. Comput. Archit.*, 2013, pp. 1–12.

[18] S. Farrell et al., "MLPerf^{TM} HPC: A holistic benchmark suite for scientific machine learning on HPC systems," in *Proc. IEEE/ACM Workshop Mach. Learn. High Perform. Comput. Environ.*, 2021, pp. 33–45.

[19] D. Lagos, V. Papaspiliotopoulos, G. Korres, and N. Hatziargyriou, "Microgrid protection against internal faults: Challenges in islanded and interconnected operation," *IEEE Power Energy Mag.*, vol. 19, no. 3, pp. 20–35, May/Jun. 2021.

[20] M. Sabah, I. T. Ojo, and A. M. Cramer, "Evolution of operability-based performance metrics for assessment of mission performance," in *Proc. IEEE Electric Ship Technol. Symp.*, 2021, pp. 1–6.

[21] R. M. Reese, C. N. Calvano, and T. M. Hopkins, "Operationally oriented vulnerability requirements in the ship design process," *Nav. Engineers J.*, vol. 110, no. 1, pp. 19–34, 1998.

[22] W. W. Anderson Jr., "Resilience assessment of islanded renewable energy microgrids," Ph.D. dissertation Nav. Postgraduate School, Monterey, CA, USA, 2020.

[23] J. C. Walker, "Multi-attribute tradespace exploration for us navy surface ship survivability: A framework for balancing capability, survivability, and affordability," Ph.D. dissertation, Massachusetts Inst. Technol., Cambridge, MA, USA, 2016.

[24] M. G. Richards, A. M. Ross, D. E. Hastings, and D. H. Rhodes, "Empirical validation of design principles for survivable system architecture," in *Proc. IEEE 2nd Annu. Syst. Conf.*, 2008, pp. 1–8.

[25] G. L. Guzie, "Integrated survivability assessment," Survivability/Lethality Anal. Directorate, Army Res. Lab., Tech. Rep. ARLTR-3186, 2004.

[26] M. N. Dodge and R. F. McKelvey III, "Why the survivability onion should include reliability, availability, and maintainability (RAM)," Ph.D. dissertation, Naval Postgraduate School, Monterey, CA, USA, 2013.

[27] S. Beheshtaein, R. Cuzner, M. Savaghebi, and J. M. Guerrero, "Review on microgrids protection," *IET Gener. Transmiss. Distrib.*, vol. 13, no. 6, pp. 743–759, 2019.

[28] M. W. Altaf, M. T. Arif, S. N. Islam, and M. E. Haque, "Microgrid protection challenges and mitigation approaches-a comprehensive review," *IEEE Access*, vol. 10, pp. 38895–38922, 2022.

[29] *IEEE Standard Interconnection Interoperability Distrib. Energy Resour. With Assoc. Elect. Power Syst. Interfaces*, IEEE Standard 1547-2018 (Revision of IEEE Standard 1547-2003), 2018.

[30] S. Brahma, N. Pragallapati, and M. Nagpal, "Protection of islanded microgrid fed by inverters," in *Proc. IEEE Power Energy Soc. Gen. Meeting*, 2018, pp. 1–5.
[31] E. A. Mohamed, G. Magdy, G. Shabib, A. A. Elbaset, and Y. Mitani, "Digital coordination strategy of protection and frequency stability for an islanded microgrid," *IET Gener. Transmiss. Distrib.*, vol. 12, no. 15, pp. 3637–3646, 2018.
[32] F. Banihashemi, M. Vygoder, N. Hoeft, and R. Cuzner, "Earthing arrangements impacts on protection schemes for a commercial microgrid," in *Proc. IEEE 8th Int. Conf. Renewable Energy Res. Appl.*, 2019, pp. 413–421.
[33] A. A. Memon and K. Kauhaniemi, "An adaptive protection for radial AC microgrid using IEC 61850 communication standard: Algorithm proposal using offline simulations," *Energies*, vol. 13, no. 20, 2020, Art. no. 5316.
[34] A. Q. Al-Shetwi, M. Z. Sujod, and F. Blaabjerg, "Low voltage ride-through capability control for single-stage inverter-based grid-connected photovoltaic power plant," *Sol. Energy*, vol. 159, pp. 665–681, 2018.
[35] Y. He, M. Wang, Y. Jia, J. Zhao, and Z. Xu, "Low-voltage ride-through control for photovoltaic generation in the low-voltage distribution network," *IET Renewable Power Gener.*, vol. 14, no. 14, pp. 2727–2737, 2020.
[36] A. Mojallal and S. Lotfifard, "Enhancement of grid connected PV arrays fault ride through and post fault recovery performance," *IEEE Trans. Smart Grid*, vol. 10, no. 1, pp. 546–555, Jan. 2019.
[37] H. He et al., "Application of a SFCL for fault ride-through capability enhancement of DG in a microgrid system and relay protection coordination," *IEEE Trans. Appl. Supercond.*, vol. 26, no. 7, pp. 1–8, Oct. 2016.
[38] J. Choi, A. Khalsa, D. A. Klapp, S. Baktiono, and M. S. Illindala, "Survivability of prime-mover powered inverter-based distributed energy resources during microgrid islanding," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1214–1224, Mar./Apr. 2019.
[39] J. Choi, A. Khalsa, D. A. Klapp, M. S. Illindala, and K. Subramaniam, "Survivability of synchronous generator-based distributed energy resources for transient overload conditions in a microgrid," *IEEE Trans. Ind. Appl.*, vol. 54, no. 6, pp. 5717–5726, Nov./Dec. 2018.
[40] J. Choi and M. S. Illindala, "Effect of prime mover's characteristics on the survivability of a synchronous generator-based distributed energy resource during transient overload conditions," *IEEE Trans. Ind. Appl.*, vol. 56, no. 1, pp. 88–94, Jan./Feb. 2020.
[41] M. C. Pulcherio et al., "Evaluation of control methods to prevent collapse of a mixed-source microgrid," *IEEE Trans. Ind. Appl.*, vol. 52, no. 6, pp. 4566–4576, Nov./Dec. 2016.
[42] W. Du, R. H. Lasseter, and A. S. Khalsa, "Survivability of autonomous microgrid during overload events," *IEEE Trans. Smart Grid*, vol. 10, no. 4, pp. 3515–3524, Jul. 2019.
[43] M. Vygoder, F. Banihashemi, J. Gudex, R. M. Cuzner, and G. Oriti, "Coordination of protection and ride-through settings for islanded facility microgrids," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 1095–1102.
[44] R. M. Cuzner, S. Beheshtaein, and F. Banihashemi, *Microgrid Protection*, ser. Energy Engineering. Institution of Engineering and Technology, 2019, pp. 395–461. [Online]. Available: https://digital-library.theiet.org/content/books/10.1049/pbpo139e_ch12
[45] P. Rodríguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg, "Multiresonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 127–138, Jan. 2011.
[46] M. Vygoder, G. Oriti, J. Gudex, T. M. Tencate, A. L. Julian, and R. Cuzner, "Comparison of voltage abnormality detection methods for single-phase inverters to meet the requirements in IEEE standard 1547-2018," *IEEE Trans. Ind. Appl.*, vol. 57, no. 5, pp. 4981–4990, Sep./Oct. 2021.

Mark Vygoder (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering and physics and the M.S. degree in electrical engineering in 2017 and 2020, respectively, from the University of Wisconsin - Milwaukee, Milwaukee, WI, USA, where he is currently working toward the Doctoral degree. He is also a Graduate Research Assistant of electrical engineering with the University of Wisconsin - Milwaukee. His current goal is help humanity achieve zero carbon emissions. His research interests include hybrid AC-DC microgrids, power electronics-based distribution systems, and their controls and protection design.

Farzad Banihashemi received the master's degree from the University of Tehran, Tehran, Iran. He is currently working toward the Ph.D. degree in electrical engineering with the University of Wisconsin-Milwaukee (UWM), Milwaukee, WI, USA. He is also a Research Assistant of electrical engineering with the University of Wisconsin-Milwaukee (UWM). Prior to joining UWM, he had 6 years of hands-on experience in the industry in power and distribution systems control and protection. His research interests include the intersection of applied machine learning and AC systems, particularly in power and distribution systems. He aims to introduce a novel approach in the field by integrating cutting-edge machine learning techniques into traditional power system methodologies

Jacob Gudex (Graduate Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering in 2017 and 2019, respectively, from the University of Wisconsin - Milwaukee, Milwaukee, WI, USA, where he is currently working toward the Doctoral degree. He is also a Graduate Research Assistant of electrical engineering with the University of Wisconsin - Milwaukee. His research include real-time simulation of power electronics, power conversion, MVDC protection, system survivablilty metrics, and their application towards shipboard electrification and microgrids.

Andrew Eggebeen received the B.S. degree in computer engineering, the M.S. degree in computer science, and the Ph.D. degree in engineering from the University of Wisconsin-Milwaukee, Milwaukee, WI, USA in 2013, 2015, and 2023, respectively. From 2002 to 2018, he was a Software and Firmware Engineering in various roles include the development of telecommunication equipment for hostage negotiation and crisis response teams. He also taught various course, such as computer architecture, computer networks, embedded C, and assembly programming during graduate school. His research interests include digital twins, machine learning, and computer science applications towards sustainable energy systems.

Giovanna Oriti (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the University of Catania, Catania, Italy, in 1997. She was a Research Intern with the University of Wisconsin-Madison, Madison, WI, USA, then with United Technology Research Center. In 2008, she joined the Faculty of the Electrical and Computer Engineering Department, Naval Postgraduate School, Monterey, CA, USA, where she is currently a tenured Professor. She holds one U.S. Patent and has coauthored more than 70 papers. Her research interests include modeling and control of power electronic converters for electric ship systems, energy management, resilient military microgrids, power quality, renewable energy interface, and mitigation of electromagnetic interference.

Robert M. Cuzner (Senior Member, IEEE) received the B.S. degree in electrical and computer engineering from Brigham Young University, Provo, UT, USA, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Wisconsin-Madison, Madison, WI, USA. He is currently an Associate Professor with the Department of Electrical Engineering and Computer Science, University of Wisconsin-Milwaukee. He has more than 30 years of experience working in power generation, power conversion, and drive system controls and packaging for both Navy and industrial applications. He has authored more than 80 publications, and he holds four U.S. patents. His research interests include microgrid protection, power electronics for power distribution and drive systems, electromagnetic compatibility, and low- and medium-voltage power conversion system design and packaging.