Neural Network Trained Cold-plate Models for Modular Converter Exploration

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Abstract—Designing power electronics for medium voltage (MV) and applications, such as the Modular Multilevel Converter (MMC) MVac-MVdc converter for Multi-Terminal (MT) MVdc systems, requires a multidisciplinary approach to optimize a highly intricate system. One of the main challenges in this field is exploring various MMC implementations and evaluating them through appropriate metrics to determine the most effective approach. To address this challenge, this paper introduces a Virtual Prototyping Process (VPP) for Power Electronic Building Block (PEBB) based systems that leverages neural networktrained coldplate surrogate models. These coldplate surrogate model is useful in managing the complexity of a single thermal interface point connected to multiple coldplate-cooled elements within an MMC Sub-Module Drawer (SMD) to a systemlevel thermal management system. This approach enables the correlation of the intrinsic power capability of point of source to point of load Power Trains as a function of coolant approach and thermal management system capability to facilitate solutuion space exploration. This exploration is conducted in an evolutionary environment (within the VPP) that balances competing objectives like power density, efficiency, specific power and specific cost. The shipboard Integrated Power and Energy System (IPES) application is used as a use-case example.

Index Terms—Surrogate Model, Power Electronic Building Block (PEBB), Neural Network, Cold Plate

I. INTRODUCTION

The modular architecture of the Modular Multilevel Converter (MMC) is appealing for ac-dc conversion in Multi-Terminal (MT) MVdc and HVdc systems because it allows for scale-able solutions over a wide range of design variables,

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such as MVdc/HVdc voltage level, utilizing common components, such as a Power Electronic Building Block (PEBB), to achieve economies of scale. The PEBB may represent a power conversion system-building component for equipment manufacturers to contribute to a wide range of applications or a point of new technology insertion to future developments. For example, the Department of Energy and Office of Naval Research have invested heavily in the development of PEBBs utilizing 10kV rated SiC MOSFET multi-chip dual modules [1], [2]. The value, or fitness, of a solution is often assessed in terms of Measures of Performance (MOPs) that have meaning at the building block level, such as power density (ρ , e.g. $\frac{MW}{m^3}$), specific power (γ e.g. $\frac{kW}{kg}$), efficiency (η , %) reliability and specific cost (σ , e.g. $\frac{MW}{USD}$). However, to ensure that these MOPs are meaningful to the end-use application other factors must be taken into account. A concrete example is the Multi-Terminal (MT) MVdc service for the Integrated Power and Energy System (IPES) for future naval ship electrification [3]. Real estate for power conversion hardware is constrained along space/weight allocations for both the IPES and for freshwater cooling thermal management, which must also service loads and sources.

A *Power Train*, which provides a power conversion path between points of MVac power generation interface and MVac load usage is shown in Fig. 2. The MMC is a promising topology for such a system, however, because of the amount of power that must be processed through this path, a maximum intrinsic power P_{oi} must be achieved given the limitations of the ship thermal management system. Solution space exploration is defined by a set of converter level design space variables, $x_V \subseteq x_S$, where x_V defines the ship system design

space, including the inlet water temperature, T_A and mass flow rate, mfr (in $\frac{kg}{s}$). Generally, as $T_A \wedge mfr$ are increased, P_{oi} increase, and as P_{oi} increases, MOPs such as ρ , γ and η will increase.

The work of this paper follows the process defined by a Model Based Systems Engineering (MBSE) Integration Framework shown in Fig. 3 applied to the Power Train of Fig 2, Full-Bridge (FB-MMC) based ac-dc converter and dc-ac converters, utilizing the PEBB of [1], interfacing through a common, inter-zonal 12kV MVdc bus. The ac-dc converter utilizes conventional MMC PWM control and can arrest current discharge if a MVdc short circuit fault occurs. Such an approach requires an additional capacitor bank within the the SMD, as shown in Fig. 1a. The dc-ac converter utilizes Single Cycle Control (SCC), which does not require the additional capacitor bank (Fig. 1b) [4].

This process centers around a VPP [5] that searches for a $P_{oi}(T_A, mfr)$ that maintains active power semiconductors at their maximum junction temperature for every combination of $T_A \wedge mfr \in x_V$, through use of a Non-dominated Sorting Genetic Algorithm (NSGA-II). The VPP accounts for dimensional and mass impacts on PEPDS building block design and construction practicalities through cuboid allocations in xyz space around the PEBB (P) and Inductor Assembly (IA), shown in Fig. 1. These Drawer-level allocations are assigned to the following functionalities: (1.) maintenance and vibration travel space, α_{Da} , (2.) basic or reinforced insulation clearances, α_{Dd} (3.) thermal management, $\alpha_{D\bar{o}}$, frame structure and enclosures α_{Df} , and busses and bus-interconnects α_{Dc} .

The steps associated with Fig. 3, are summarized as follows: (1.) Derivation of a thermal-physical (TP) equivalent model of the coldplate; (2.) Incorporation of the TP into an electrothermal-physical (ETP) equivalent model of the full Power Train with SMDs into VPP and extraction of coldplate solution sets from the VPP outcomes; (3.) Development and training of the coldplate surrogate models for the PEBB and inductor assembly (IA) using neural networks; (4.) Validating of the coldplate surrogate models in VPP. Development of SMD metamodels that present ETP parameters, characteristics and behavior of the SMDs that scale with x_V against constraints $r_V \subseteq r_S$ (these metamodels represent only the solutions on the Pareto front); (5.) Size, Weight, Area and Power versus Coolant (SWAaP-C) studies where the SMDs are integrated into a Power and Energy Corridor, described in [6], leading to identification of thermal management solution support of P_{oi} . The focus of this paper is to provide the details on (2.)-(4.).

II. PEBB OVERVIEW

The novelty of this MBSE approach is that it maintains traceability of all IPES level decisions through design space variables, x_V , sub-sets of the ship system level design space variables, x_S , or technology insertion variables. Regarding the latter, x_V will include PEBB types, power conversion topological implementations, control and thermal management approaches, and protection philosophy (e.g. breaker-based vs. breaker-less protection). The process is designed to enforce

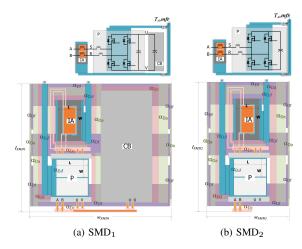


Fig. 1: Sub-Module Drawer circuits and their compilations

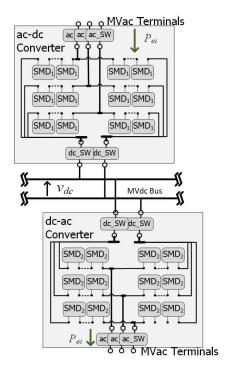


Fig. 2: MT-MVdc System

transparency between design space variable inputs (x_V) and performance measure outcomes (MOPs and TPMs).

The PEBB type used is the PEBB6000, utilizing 10kV SiC MOSFETs in an H-bridge configuration. This PEBB supports modular topologies like the FB-MMC for MVac-MVdc power conversion, with MVdc-side current limiting capability [1]. The PEBB data, refered to in Fig. 3 utilizes the information from [1] and as a datasheet to develop a virtual twin representation of the PEBBs in the context of the MVac-MVdc and MVdc-MVac converters comprising the Power Train, with the exception of the heat sink. Instead, the heat sink of the design of [1] is replaced by indirect water-cooled

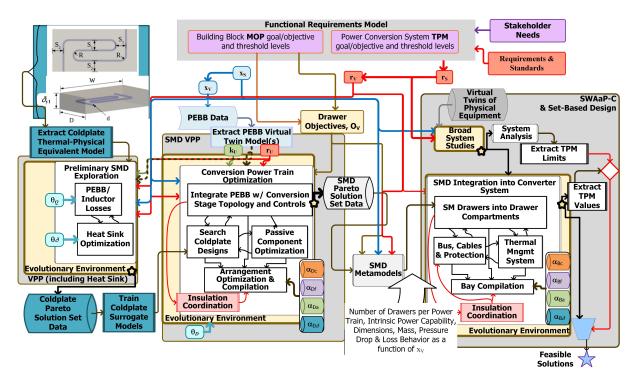


Fig. 3: Integration Framework

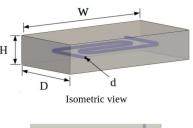
coldplate, which means that power semiconductor modules are mounted on the coldplate surface. The sub-module inductor also has coldplates mounted on two coil and two core surfaces, as will be described. All codlpates are mounted through high thermal conductivity interfaces. This approach can ensure predictable sink temperatures on all coldplate cooled surfaces. It will be necessary for the coldplate coolant water to be de-ionized so that they can float with respect to ground and for clearance spaces to be maintained between coldplates and Drawer chassis.

III. THERMAL ANALYSIS AND COLD-PLATE MODEL

A. Theory and Analysis

Liquid cooling systems effectively manage heat in power electronic devices, critical for applications like industrial automation, electrical ships, electric vehicles, and renewable energy. They excel in thermal management by removing heat from high-temperature areas more effectively than air cooling, despite being more complex and costly [7].

Fig. 4 shows a scheme of the cold plate design considered in the present study. The plate geometry consists of a hexahedron defined by the external lengths W, D, and H. The internal pipe shape is defined by the diameter d, the spans S_1 (between pipe center lines) and S_2 (between pipe center lines and plate edges), and also the bend radius R. Regarding the modeling of the cold plate, the flowchart in Fig. 5 demonstrates the various processes carried out. Since values for W, D, H, R and d are assumed, S_1 and S_2 are calculated by Eq. 1. However, if the condition $S_2 \geq d/2$ is not satisfied, the design is infeasible as the pipe exceeds the area limits of the plate. In this case,



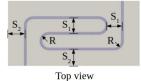


Fig. 4: Scheme for the cold plate and internal pipe.

the value of R is iteratively reduced to fit the pipe within the plate. It is worth noting that water was selected as the fluid and aluminum (UNS A91060) as the plate material. The relevant properties of the selected material are listed in Tab. I while water properties vary depending on the design. Therefore, water properties were obtained through CoolProp, which is a library that provides transport properties for a variety of substances [8], and the computational environment MATLAB [9] was applied to implement the modeling.

$$S_1 = 2R S_2 = \frac{D - 2S_1}{2}$$
 (1)

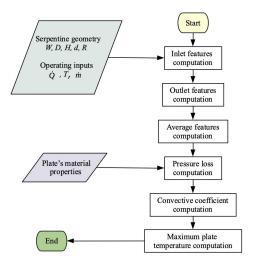


Fig. 5: Flowchart for the cold plate modeling

TABLE I: Plate material properties.

Feature	Value
Density (ρ_p)	$2705 \ kg/m^3$
Allowable stress (S_A)	$10.9 \cdot 10^{6} \ Pa$
Molar mass	$26.98 \ kg/kmol$
Specific heat	$935.6 \ J/kg \cdot K$
Thermal conductivity	$224.5 \ W/m \cdot K$
Roughness	$0.03 \cdot 10^{-3} \ m$

The pipe pressure loss (Δp) was calculated with Eq. 2, where f is the Darcy friction factor, K_{90} and K_{180} are the minor loss coefficient respectively for 90° and 180° pipe bends [10], \dot{m} is the mass flow rate and ρ is the fluid density. The friction factor (f) was calculated through Eq. 3, where Re is the number of Reynolds and the factors A and B are calculated based on Re, d and roughness (ε) according to [11].

$$\Delta p = \left[f \frac{l}{d} + n_{90} K_{90} + n_{180} K_{180} \right] \frac{8\dot{m}^2}{\pi^2 d^4 \rho} \tag{2}$$

$$f = 8 \left[\left(\frac{8}{Re} \right)^{12} + (A+B)^{-1.5} \right]^{\frac{1}{12}}$$
 (3)

Notice that ρ , as well as the other fluid properties, depends on the temperature and was taken as a constant at the average temperature (T_{avg}) given in Eq. 4. The inlet temperature (T_i) was given and the outlet temperature (T_o) was calculated by the energy balance in Eq. 5, where h_i and h_o are the specific enthalpies at the pipe inlet and outlet, respectively.

$$T_{avg} = \frac{T_i + T_o}{2} \tag{4}$$

$$\dot{Q} = \dot{m}(h_o - h_i)$$
, having $h_o = f(T_o)$ and $h_i = f(T_i)$ (5)

The maximum temperature over the plate was approached by Eq. 6, where \dot{q} is the average heat flux over the hot face of the plate, and κ_p is the thermal conductivity of the plate

material. The distance between the pipe bend and the corner of the plate (r_2) was calculated by Eq. 7, and the temperature at the internal surface of the pipe (T_s) was achieved through Eq. 8. In the latter equation, \dot{Q} is the heat transfer rate crossing the hot face of the plate, which is the same as reaching the serpentine pipe, s is the pipe heat transfer area, and h is the average internal convective coefficient acquired through Eq. 9.

$$T_{max} = \frac{\dot{q} \cdot r_2^2 \ln\left(\frac{r_2}{R}\right)}{2\pi \cdot d \cdot \kappa_p} + T_s \tag{6}$$

$$r_2 = [2(S_2 + R)^2]^{0.5} (7)$$

$$T_s = \frac{\dot{Q}}{h \cdot s} + T_{avg} \tag{8}$$

$$h = \frac{Nu \cdot \kappa}{d} \tag{9}$$

The symbol κ stands for the thermal conductivity of the fluid while Nu is the Nusselt number, which was computed through convection correlations. Depending on the Prandtl and Reynolds number values, as well as the flow regime (laminar or turbulent), different formulations were applied to calculate Nu [12]. Then, the heat Resistance Sink to Ambient (RSA) was calculated by Eq. 10.

$$RSA = \frac{T_{max} - T_A}{\dot{Q}} \tag{10}$$

The intrinsic power of each SMD is fundamentally constrained by the PEBB power semiconductor junction temperature, making efficient heat dissipation from the devices crucial for achieving maximum power output. As illustrated in Fig. 6, the heat resistance of each device is modeled in parallel with the heat resistance of its corresponding diode. This configuration ensures that the thermal characteristics of each component are accurately represented, allowing for a comprehensive analysis of the thermal behavior within the system. Each half-bridge configuration includes both upper and lower branches, with their combined resistances ultimately leading to the RSA (resistance to ambient) and ambient temperature.

The PEBB employs two half-bridge structure (for each side of the H-bridge) and utilizes two series cold plates to manage heat dissipation. The cold plates are strategically positioned to maximize heat transfer and minimize thermal resistance. The intrinsic power is limited by the hot-spot temperature of devices in the second cold plate which is fed by first cold plate, highlighting the importance of effective thermal management in the design. The thermal behavior of these devices is critical, as excessive temperatures can lead to reduced efficiency and potential failure. Fig. 6 shows PEBB thermal circuit equivalent. Fig. 6 illustrates the PEBB Thermal Circuit Equivalent. R_{jc_T} is the junction-to-case thermal resistor for the transistor, and R_{jc_D} is the junction-to-case thermal resistor for the diode, which is zero for SiC MOSFETs and applicable only when using IGBTs. In this figure T_s represents the surface

temperature of PEBB, while T_c is the temperature of each device. The RSA represents the thermal resistance of sink to ambient, which is the cold plate thermal resistance equivalent and is calculated using Eq. 10. Based on Fig. 6, the thermal

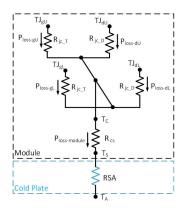


Fig. 6: PEBB Thermal Circuit Equivalent.

rise in temperatures due to heat generated by the devices, affecting the surface temperatures of PEBB and the cold plate, is as follows:

$$\Delta_{Tjc_qU} = P_{\text{loss_qU}} \cdot R_{jc_T},$$

$$\Delta_{Tjc_dU} = P_{\text{loss_dU}} \cdot R_{cj_D},$$

$$\Delta_{Tjc_U_max} = \max(\Delta_{Tjc_qU}, \Delta_{Tjc_dU}),$$

$$\Delta_{Tjc_qL} = P_{\text{loss_qL}} \cdot R_{jc_T},$$

$$\Delta_{Tjc_dL} = P_{\text{loss_dL}} \cdot R_{cj_D},$$

$$\Delta_{Tjc_L_max} = \max(\Delta_{Tjc_qL}, \Delta_{Tjc_dL}),$$

$$\Delta_{Tjc_max} = \max(\Delta_{Tjc_U_max}, \Delta_{Tjc_L_max}),$$
(11)

and as a result:

$$T_{S_qU_max} = T_{j\max_derated} - P_{loss_qU} \cdot R_{jc_T} - (P_{loss_Module}) \cdot R_{cs},$$

$$T_{S_dU_max} = T_{j\max_derated} - P_{loss_dU} \cdot R_{jc_T} - (P_{loss_Module}) \cdot R_{cs},$$

$$T_{S_U_max} = \min(T_{S_qU_max}, T_{S_dU_max}),$$

$$T_{S_qL_max} = T_{j\max_derated} - P_{loss_qL} \cdot R_{jc_T} - (P_{loss_Module}) \cdot R_{cs},$$

$$T_{S_dL_max} = T_{j\max_derated} - P_{loss_dL} \cdot R_{jc_T} - (P_{loss_Module}) \cdot R_{cs},$$

$$T_{S_dL_max} = \min(T_{S_qL_max}, T_{S_dL_max})$$

$$T_{S_L_max} = \min(T_{S_qL_max}, T_{S_dL_max})$$

so, the maximum temperature of PEBB surface is:

$$T_{\text{S_max}} = \min(T_{s_U_\text{max}}, T_{s_L_\text{max}}) \tag{13}$$

as a result:

$$T_{jmax_check} = \Delta_{Tjc_max} + (P_{loss_Module}) \cdot R_{cs} + T_{S_max}$$
 (14)

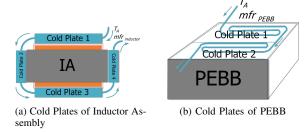


Fig. 7: Arrangement of cold plates of inductor and PEBB

As the thermal condition limits the maximum intrinsic power of the SMD, Eq. 15 in NSGA-II has been considered as a thermal constraint to find the Pareto front of the design.

$$T_{\rm Jmax_derated} + \Delta T_{\rm max} \le T_{\rm Jmax_Check} \le T_{\rm Jmax_derated} + \Delta T_{\rm max}$$
(15)

The $T_{\rm imax}$ of SiC MOSFET is 175 °C, and a derating factor of 0.9 has been considered, so $T_{\text{imax_derated}}$ is 155 °C. In addition, in Eq. (15), $\Delta T_{\rm max} = \pm 5\,^{\circ}{\rm C}$. Similarly, the inductor setup includes four cold plates arranged in a Coil - Core - Coil -Core configuration. Two of these cold plates are in contact with the coil and winding, while the other two are in contact with the cores. This arrangement ensures that heat is efficiently dissipated from both the coil and the cores, maintaining optimal operating temperatures throughout the inductor. The intrinsic power of the drawer is determined by the hot-spot temperatures in either the inductor or the PEBB, depending on the respective losses of the PEBB and the inductor. This interdependence between components underscores the complexity of thermal management in high-power systems. Fig.7 shows the arrangement of cold plates of inductor assembly and PEBB.

To summarize, efficient dissipation of heat thoroughly through cold plates in both the PEBB and inductor is essential for maximizing the intrinsic power output. The hot-spots in these components serve as the primary limiting factors, influenced by the heat resistances and arrangement of the cold plates. By maintaining effective thermal management, it is possible to enhance the performance and reliability of the system, ensuring that it operates within safe temperature limits. The use of cold plates and strategic thermal design are critical elements in achieving optimal performance in high-power electronic systems.

B. Cold-Plate Surrogate Model

Overview: Heat sinks are vital for dissipating heat in power electronic systems, affecting junction temperatures, power density, and overall reliability. Efficient design is crucial, and surrogate models can enhance this process by approximating complex thermal behaviors with less computational effort.

Process of Cold Plate Optimization: Optimization begins by creating a dataset through high-fidelity simulations, varying parameters like geometry, material properties, airflow, and power dissipation. Theoretical cold plate analysis, detailed in

Section 2, aids in generating this dataset, which trains a neural network model for accurate thermal performance predictions.

Design space variables such as coolant approach, mass flow rate and water temperature are explored, connecting them to the intrincic power capability of the Power Train of Fig. 2. Additionally, pipe diameter and cold plate dimensions for PEBB and inductors serve as genes and intermediate variables in the NSGA-II optimization algorithm. These variables balance thermal resistance, pressure drop, and cooling efficiency to identify optimal designs.

Neural Network (NN) models capture complex, nonlinear relationships through interconnected layers of nodes (neurons) processing inputs. The NN model is trained from data produced by the VPP, utilizing TP equivalent models for the coldplate (Fig. 6). Training adjusts connection weights to minimize prediction errors, handling large, multidimensional datasets effectively. The trained model is integrated into an optimization framework to find the best cold plate design, aiming for high power density and efficiency. Objectives include minimizing junction temperature and maximizing heat dissipation, with validation through high-fidelity simulations.

Advantages of Using Neural Network Models for Cold Plate Optimization: Neural network models excel in handling nonlinear relationships between parameters and thermal performance, creating accurate surrogate models essential for reliable optimization. They manage large datasets with many features, adapting to various cold plate and cooling technologies. Efficient in evaluating numerous configurations, these models significantly reduce computational time and resources, making the optimization process more cost-effective.

C. Neural Network Modeling for Cold Plate Design

Neural networks have significantly influenced engineering by enabling the modeling of complex, nonlinear relationships that traditional methods struggle to handle. They are widely used in areas such as predictive maintenance, system optimization, and real-time monitoring due to their ability to process large datasets and identify intricate patterns.

Neural networks (NNs) have revolutionized electrical engineering [13]–[18]. They optimize grid operations [15], fault diagnosis [16], and stability assessment [17], [18], and enhance signal processing [14], control systems [18] and controller design for electrical power system [19].

In this study, a NN model was developed to simulate the thermal behavior of a cold plate, specifically predicting pressure drop and thermal resistance (RSA) from the cold plate to ambient conditions. The model used input parameters including mass flow rate, water temperature, cold plate dimensions, and tube diameter. Our approach started with data pre-processing, focusing on standardizing input features and target outputs through z-score normalization to improve model training effectiveness. The dataset was then split into training (80%) and testing (20%) subsets to evaluate how well the model could generalize.

The NN architecture consisted of multiple fully connected layers with Rectified Linear Units (ReLU) activation functions,

designed to capture the complex nonlinear dynamics in the data. Training used the Adam optimizer with a customized learning rate schedule to ensure efficient convergence, aided by GPU acceleration for faster computations. Post-training evaluation included calculating Mean Squared Error (MSE) on the test dataset to measure prediction accuracy. Visual comparisons between predicted and actual outputs further validated the model's performance. The trained model and normalization parameters were saved for future analysis and application.

In practical application, the trained NN model was employed to design optimized cold plates for both the inductor and PEBB. This involved configuring four series-connected cold plates for the inductor—two for the core and two for the coil—as well as two series-connected cold plates for the PEBB. This approach ensured efficient thermal management by accurately predicting pressure drop and RSA under varying operational conditions.

In Fig. 8, the inputs and outputs of the model are depicted. Due to the use of series-connected cold plates, the output of the first cold plate serves as the input to the next one.

IV. RESULTS

Fig. 8 illustrates the algorithm employed in this paper to achieve and validate surrogate model of cold plate. The optimization goal of this study extends to factors like power, power density, and efficiency, guiding the decision-making process in design selection. Furthermore, the study explores the Virtual Prototyping Process (VPP) for thermal management, where digital models of physical components are created. This ensures that the ship system's thermal support capacity influences power train ratings, rather than relying solely on individual design exercises. This paper investigates the use of NSGAii (Non-dominated Sorting Genetic Algorithm II) to discover optimal designs. These designs are then employed to train the NN model, serving as a surrogate for cold plate designs used in both inductors and PEBBs, ultimately enhancing system efficiency.

In thermal management, liquid coolant and cold plates are crucial, particularly in PEBB and inductor applications. Cold plates are arranged in series for PEBBs and inductors, enhancing cooling efficiency. NSGA-II constraints include evaluating pressure drop in each branch and optimizing cold plate design. Dynamic coolant flow rate adjustment is vital for optimizing thermal performance. In the pursuit of scalable designs, the study examines various design parameters within cold plate design. Factors like mass flow rate, coolant water temperature, and tube diameter are carefully considered to optimize thermal performance and efficiency. This holistic approach ensures the development of effective thermal management solutions while paving the way for future advancements in the field. Since the optimization objective in this study aims to achieve an optimal system from multiple perspectives, the response of the optimization algorithm will be in the form of a Pareto solution set. The algorithm operates by exploring a wide range of genes, including dimensions and specifications of

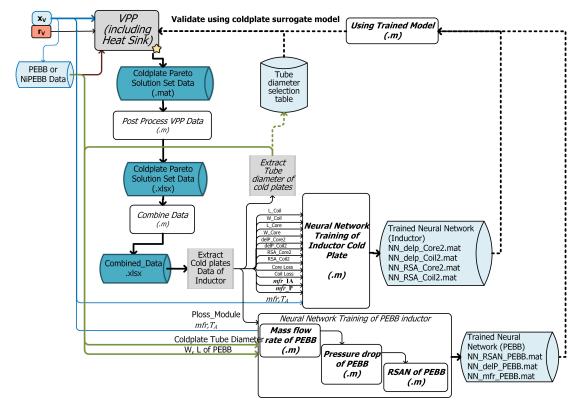


Fig. 8: Flowchart of Process

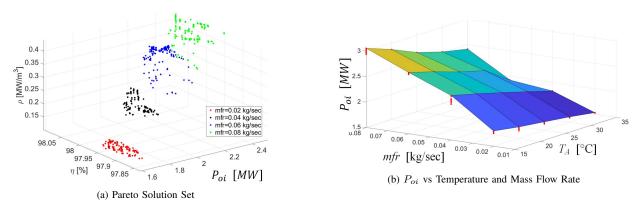


Fig. 9: Outputs from the Virtual Prototyping Process (VPP)

the inductor core and its windings, as well as air gaps, based on the input power level and the characteristics of PEBB. It selects the optimal inductor in a way that minimizes dead space and maximizes power density. Furthermore, throughout this process, the goal is to maximize output power while maintaining efficiency at its highest level.

In this study, the design space variables of cold plates consist of water temperature and mass flow rate, ranging from 15 to 35 degrees Celsius and from 0.02 to 0.08 kg/sec, respectively and the tube diameter is in the range of [0.25 0.5] inches as a gene. Fig. 9b shows power level variations with temperature and mass flow rate. Increasing temperature lowers

power, while higher mass flow rates enhance it, as depicted in the Pareto solution set in Fig. 9a. Each Pareto solution maximizes a specific objective component. Temperature and mass flow rate variations affect trends in maximum power, power density, and efficiency, as seen in the displayed surfaces. Fig. 10 compares outputs from the VPP with the NN-based surrogate model of coldplate.

This analysis offers valuable insights into the surrogate model's performance and reliability in simulating the thermal management system. Further evaluation will determine its accuracy and effectiveness in capturing system dynamics.

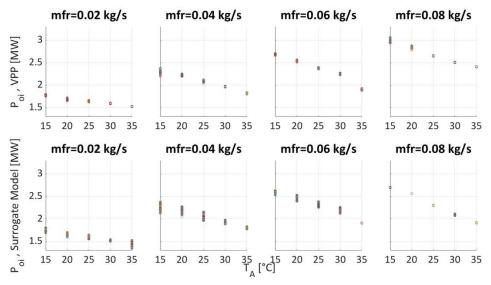


Fig. 10: VPP outputs vs. Surrogate Model outputs

V. CONCLUSIONS

This study presents a VPP integrating NN-based surrogate models for optimizing MMCs utilized in a shipboard MT-MVdc IPES. By employing surrogate models, a non-dominated Sorting Genetic Algorithm II (NSGA-II), utilized within the VPP, enabled the identification of Pareto-optimal solutions, balancing power density, efficiency and intrinsic power through output criteria, while maintaining a single point of thermal interface to SMD building blocks of an MMC-based system for two separate coldplate cooled components within those SMDs, the PEBB and a sub-module inductor.

Future research can enhance NN accuracy, expand dynamic operational capabilities, and integrate advanced controls to explore a wide range of PEBB-based power conversion strategies within multi-converter systems.

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