

Analysis of SRAM PUF Integrity Under Ionizing Radiation: Effects of Stored Data and Technology Node

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Abstract—Power-up states of static random access memory (SRAM) chips are routinely used to derive their physical unclonable functions (PUFs). Radiation effects on the integrity of SRAM PUFs have recently gained significant attention. This article demonstrates experimentally that the data stored in SRAM during irradiation impact the integrity of SRAM PUFs. Next, the SRAM-PUFs derived from chips manufactured using smaller technology nodes appear to be more robust to the effects of radiation. Consequently, the selection of a family of SRAM chips and their predeployment characterization to inform how SRAM cells should be primed during irradiation can help improve the integrity of SRAM PUFs.

Index Terms—Ionizing radiation, physical unclonable function (PUF), static random access memory (SRAM).

I. INTRODUCTION

PHYSICAL unclonable functions (PUFs) are an important hardware security primitive that can be used for device-specific key generation and device authentication. The power-up state of static random access memory (SRAM) is routinely used for generating PUF [1], [2]. SRAM power-up state is a random bit stream that is unique for a particular memory chip. Its uniqueness is closely tied to the manufacturing process variations. SRAM PUFs are commonly used in commercial electronic systems because of the ubiquitousness of SRAM memories [3], [4], [5], [6]. SRAM PUFs are also of interest in space applications and electronic systems operating in radiation-prone environments (e.g., nuclear energy).

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Radiation effects on PUFs have recently gained significant traction with the ever-growing satellite constellations and the requirement for radiation-hardened hardware security primitives. An array of recent research investigations [7], [8], [9], [10], [11] has delved into the radiation effects on PUF circuits. For example, Wang et al. [9] investigated X-Ray and proton radiation effects on 40-nm CMOS PUF circuits, named BD-PUF, that utilize the randomness of oxide breakdown (BD) positions in transistors to generate the PUF. Their results show that BD-PUF is robust under X-ray irradiation up to 2 Mrad (SiO₂), but it shows significant degradation at high-fluence proton irradiation, attributed primarily to a threshold-voltage (V_t) shift of the selector device. Similarly, Martin et al. [8] studied TID effects on delay-based CMOS ring-oscillator PUF. They observed significant degradation of PUF reliability, exceeding 10% intradie Hamming distance (HD) after 300 krad(Si) of irradiation. Sakib et al. [7] explored the TID effects on a PUF derived from NAND flash memory chips. The results unveiled a substantial decline in PUF accuracy after irradiation.

Additionally, there have been several studies on radiation effects on SRAM PUF. For example, Lawrence and his colleagues [10] explored the effects of X-ray and proton irradiation on SRAM PUFs using commercially available standalone SRAM memory chips. They observed significant degradation in the accuracy of SRAM PUFs after 100 krad(SiO₂) of irradiation. Similarly, Surendranathan et al. [12] studied the effects of Co-60 radiation on SRAM PUFs derived from commercial SRAM memory chips sourced from various manufacturers. They reported more than a 15% bit error rate after 100-krad(Si) irradiation. Cui et al. [13] studied the effects of very high dose [200 Mrad(Si)] irradiation on a 65-nm SRAM memory array. Interestingly, they found a reverse data pattern imprinting effect on the power-up characteristics of the array due to the bias-dependent threshold shift of cell transistors. Zhang et al. [11] proposed a stability improvement method for SRAM PUF using ionizing irradiation. They found that by irradiating the SRAM memory array to a moderate amount of TID of 40 krad(SiO₂), the intrachip HD can be improved significantly. Su et al. [14] proposed a novel SRAM cell design with eight transistors (8Ts) to enhance the reliability and radiation tolerance of SRAM PUF. Their approach involved the incorporation of two cascading pMOS transistors into

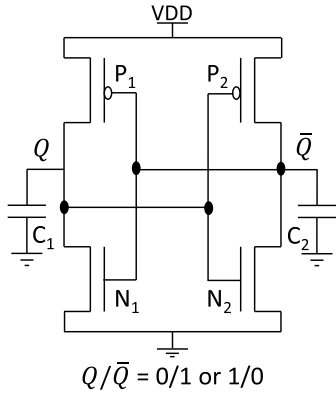


Fig. 1. Cross-coupled inverter pair in an SRAM cell with two possible stable states $Q/\bar{Q} = 0/1$ or $1/0$.

TABLE I
CONDITIONS FOR POWER-UP STATES

$Q/\bar{Q}$	NMOS mismatch	PMOS mismatch
0/1	$V_t^{N_1} < V_t^{N_2}$	$ V_t^{P_1} > V_t^{P_2} $
1/0	$V_t^{N_1} > V_t^{N_2}$	$ V_t^{P_1} < V_t^{P_2} $

the standard 6T cell configuration fabricated using 28-nm FDSOI process technology. This modification yielded superior radiation tolerance in comparison to the standard 6T design.

Although several prior studies have examined the TID effects on SRAM PUFs, questions regarding the impact of technology node on the TID response of SRAM PUFs remain unanswered. Similarly, a comprehensive analysis regarding the impact of data patterns held in memory during irradiation on the integrity of SRAM PUFs is missing in the published literature. In this article, we aim to address these open questions by conducting a series of thorough experiments.

This article investigates and analyzes three distinct aspects of TID effects on the integrity of PUFs. The first aspect involves examining the impact of the data stored in the SRAM memory array during gamma-ray irradiation on the subsequent integrity of the SRAM PUFs. The second aspect focuses on evaluating the relationship between the SRAM technology node and the extent of degradation in the SRAM PUF induced by TID. Lastly, the effects of postirradiation room temperature annealing on the SRAM PUF integrity are investigated.

II. BACKGROUND

An SRAM cell is composed of a cross-coupled CMOS inverter pair and two bitline access transistors. Fig. 1 shows the schematic of the cross-coupled inverter pair. The access transistors are turned off during power-up and are thus modeled as capacitors to capture power-up dynamic response. The cross-coupled inverter pair has two stable states, $Q/\bar{Q} = 0/1$ or $Q/\bar{Q} = 1/0$, as shown in Table I. After a power-up, the SRAM cell ends up in either of the states, depending on manufacturing

process variations. For example, $Q/\bar{Q} = 0/1$ will be the default power-up state if $V_t^{N_1} < V_t^{N_2}$, assuming V_t values of pMOS transistors are closely matched. Several factors including variations in W/L ratios can influence the power-up cell state alongside V_t . Since radiation effects do not alter the transistor geometry, we focus solely on V_t variation to explain radiation-induced changes in the power-up states. Since an SRAM chip contains an array of memory cells, the power-up state of these cells provides a random number that can be used for generating SRAM PUFs. If the power-up state is repeatedly captured on the same chip, it produces a similar random sequence of bits, albeit not identical, as some memory cells change their power-up state. We flag these mismatches as errors, and we quantify them by measuring the HD as follows:

$$HD = \frac{\# \text{HW}(\text{GoldPUF XOR AuthenticationPUF})}{\text{Total \# of PUF bits}} \quad (1)$$

where GoldPUF refers to the reference SRAM PUF and AuthenticationPUF refers to the PUF derived during the authentication process. The HW represents the Hamming weight. Thus, HD represents the number of mismatches between the GoldPUF and AuthenticationPUF relative to the total number of bits in the PUF, as shown in (1).

III. EXPERIMENTAL SETUP AND FLOW

The irradiation experiments were conducted at The Ohio State University Nuclear Reactor Laboratory, utilizing the underwater Gamma Irradiator [15]. The Co-60 source employed in the experiments provided a dose rate of 11.7 krad(Si)/h. The gamma irradiator consists of a vertically extending 6-in-diameter dry tube positioned within a light water pool. Twenty-five Co-60 pins were placed around the tube to ensure a uniform radiation field featuring gamma rays at energies of 1.173 and 1.332 MeV. The gamma irradiation process involved subjecting packaged TSOP (thin small outline package) devices to radiation, while the chips remained powered on. Commercial off-the-shelf (COTS) SRAM chips from Cypress, ISSI, and Alliance were utilized in the experiments. Details of the chips are given in Table II [16], [17].

To interface the SRAM chips with a workstation, we have used a custom-designed setup [12]. The setup includes an Arduino Due interfacing the workstation via the Universal Serial Bus (USB) and a TSOP-54 socket holding an SRAM chip. The Arduino firmware supports powering up/down of SRAM chips, reading the SRAM chips' power-up states, and writing selected data patterns into the SRAM chips. Powering off the SRAM chips is carried out through a pMOS switch by driving its gate voltage to 3.3 V for 5 s, while concurrently keeping data, address, and control pins of the SRAM chip at 0 V.

The experimental flow is as follows. We gather 101 power-up states and create a majority voting-based GoldPUF. Before irradiating the chips, we precharacterize each chip to obtain their baseline performance. We prime the chips with different data patterns and then irradiate them to analyze the effects of stored data during irradiation on power-up states. The chips remain powered on during irradiation for each dose step. We then retrieve the power-up states of the irradiated

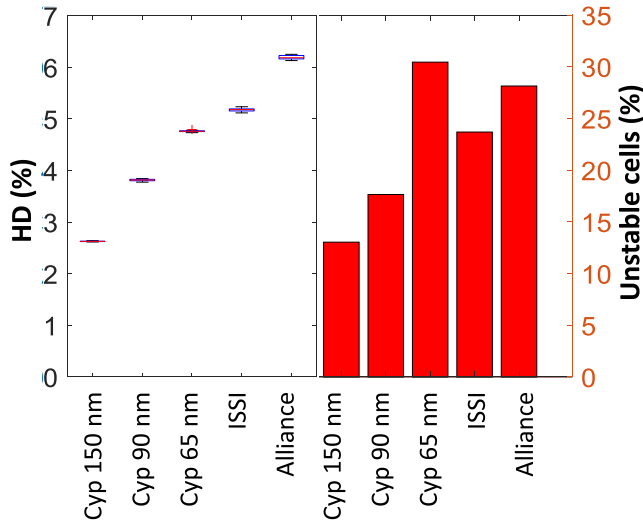


Fig. 2. Baseline HD% and unstable Cells% characterization of SRAM samples.

chip immediately after irradiation (within 5 min). We generate 25 different authentication PUFs from each chip using power on/off cycling. Each authentication SRAM PUF is compared to the corresponding GoldPUF to compute HD. We take the average of the 25 different HD values and plot it in the subsequent analysis. For the technology-node analysis, the procedure remains the same as above; however, the chips are exposed to irradiation in a powered-off state with all pins grounded.

IV. RESULTS AND DISCUSSION

A. Baseline Characterization Results

The baseline power-up states for different SRAM chips are characterized for the unirradiated condition. The corresponding HD% and unstable cells% are shown in Fig. 2. We define unstable cells as those that flip their state during consecutive PUF generations. The procedure to determine unstable cells is described in our previous publication [12]. The percentage of cells with power-up state at logic-1 is about 50% for all chips. We use 25 authentication PUFs to obtain the HD% and unstable cells%. Variation among the 25 PUFs is not significant as shown in the Box Whisker plot for HD%. We observe a monotonic increase in HD% for different Cypress SRAM chips, where chips manufactured using lower technology nodes have a higher HD%. We have also analyzed the PUFs generated from different locations of the chips and have found that the PUF metrics, such as HD% and unstable cell%, remain relatively stable across different regions of a given memory chip.

B. Effects of Stored Data on the Power-Up State

Fig. 3 shows the effects of priming SRAM chips with various data patterns during radiation exposure. We divide every chip into four quarters and then program every quarter with a different data pattern as follows: all-zero, all-one, GoldPUF, and inverted GoldPUF. Fig. 3(a) shows the HD% for

the 150-nm Cypress chip. We observe a monotonic increase in HD% with an increase in TID, regardless of the data stored. Interestingly, we observe a distinct difference in the slope of HD% increase as a function of the data pattern. The rate of increase in HD% with TID is significantly lower for the cells primed with the GoldPUF than for the cells primed with the inverted GoldPUF. The HD% of regions primed with the all-zero and all-one data pattern is identical, and they are approximately the average value of the HD% of the regions primed with the GoldPUF and inverted GoldPUF. Since the all-zero and all-one data pattern can be considered as a superposition of the GoldPUF and the inverted GoldPUF, their effects on PUF degradation show the averaging behavior. Fig. 3(b) shows the percentage of unstable cells as a function of TID. Holding the GoldPUF in SRAM during irradiation lowers the percentage of unstable bits, whereas holding the inverted GoldPUF increases the percentage of unstable bits. The results in Fig. 3(a) and (b) thus imply that it is advantageous to keep the Cypress SRAM memory in the typical power-up state, which is very similar to the GoldPUF, during irradiation to minimize PUF degradation due to TID effects. However, these trends are not universal for SRAM chips coming from different manufacturers.

Fig. 3(c) and (d) shows the HD% and unstable cells% for the ISSI chip, respectively. A notable contrast in behavior is evident between the Cypress and ISSI chips. In the case of the ISSI chips, the rate of increase in HD% is markedly lower when holding the inverted GoldPUF compared to holding the GoldPUF. In fact, we even observe a reduction in HD% for the ISSI chip holding the inverted GoldPUF after TID = 10 krad(Si). Hence, it proves advantageous to toggle the power-up state of the ISSI chip when it is in an idle state during irradiation to minimize TID effects on its PUF characteristics.

Fig. 3(e) and (f) shows the HD% and unstable cells% for the Alliance chip, respectively. Similar to the ISSI chip, we observe a lower rate of increase of HD% when holding the inverted GoldPUF during irradiation. Unlike the other chips, we find a saturation in HD% for regions holding the GoldPUF for TID > 50 krad(Si). Thus, we find a converging HD% for different data patterns for TID > 50 krad(Si).

Fig. 4 provides an elucidation for the disparate behavior exhibited by these chips. In our analysis, we leverage two key observations concerning the effects of TID on MOS structures. First, we find that TID induces a downshift in the threshold voltage of MOS transistors, leading to a decrease in the magnitude of V_t for nMOS transistors and an increase in the magnitude of V_t for pMOS transistors. This shift is observed assuming a positive V_t values for nMOS and negative V_t values for pMOS transistors. Second, we note that there is an asymmetry between the V_t shifts between nMOS/pMOS in the ON/OFF states [11], [13]. By taking these observations into account, we provide a plausible explanation for the dependency of SRAM PUF integrity on data patterns held during irradiation in the following paragraphs.

Fig. 4(a) elucidates the TID effects on Cypress SRAM chips. Consider an SRAM cell with a default power-up state set to “0” [see Fig. 4(a)], denoting $Q/\bar{Q} = 0/1$. Assume that its power-up state is determined by the mismatch between the

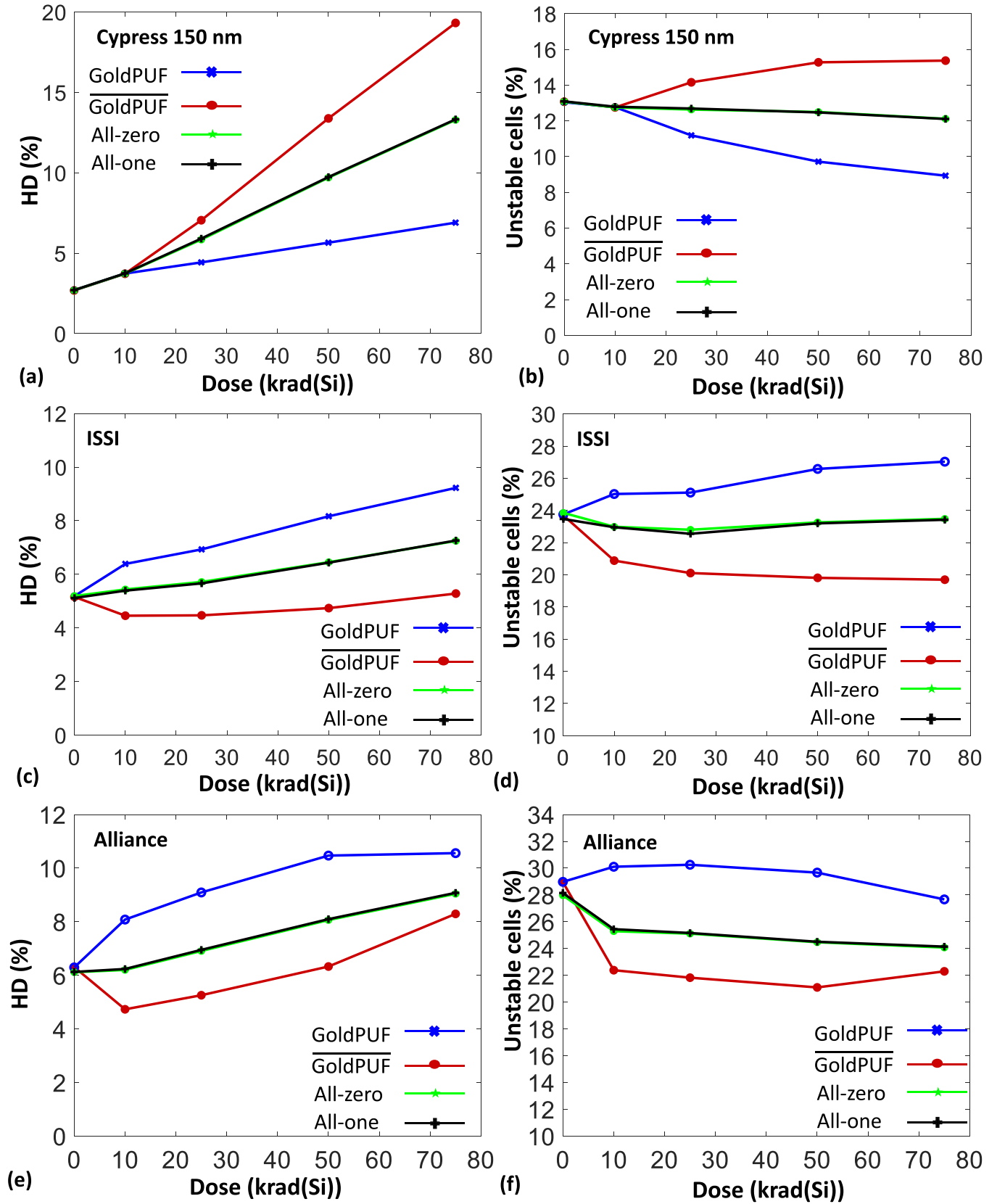


Fig. 3. Effects of data stored on HD% and unstable cells%. (a) Cypress HD%. (b) Cypress unstable cells%. (c) ISSI HD%. (d) ISSI unstable cells%. (e) Alliance HD%. (f) Alliance unstable cells%.

nMOS transistors. In this case, the threshold voltage relation $V_t^{N_1} < V_t^{N_2}$ will lead to power-up $Q/\bar{Q} = 0/1$. If the cell is irradiated in its default state (N_1 turned on and N_2 is off) as per [11], we can expect $\Delta V_t^{N_1} > \Delta V_t^{N_2}$, implying

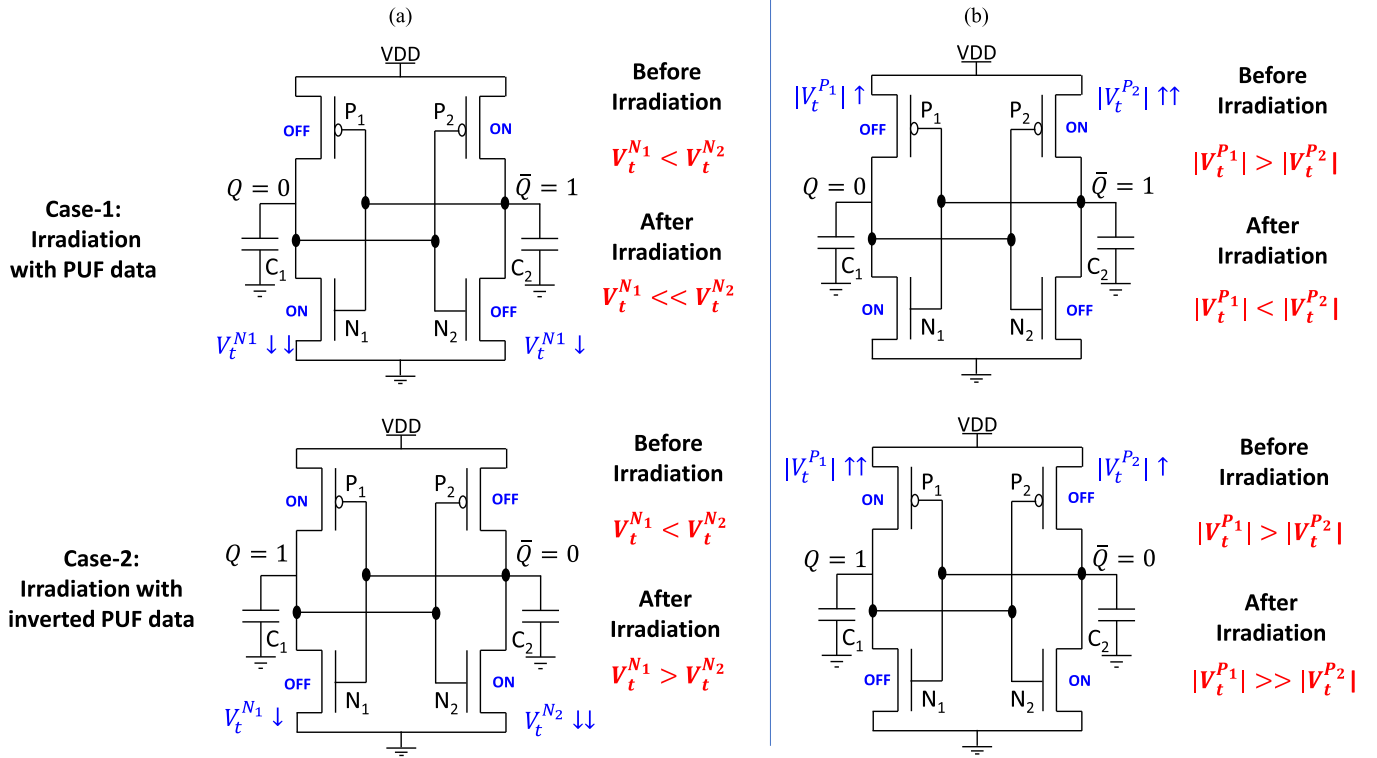


Fig. 4. Effects of data pattern on power-up state of irradiated SRAM cells. We assume two cases: (a) SRAM cell whose power-up state is dictated by mismatched nMOS transistors and (b) SRAM cell whose power-up state is dictated by mismatched pMOS transistors.

$V_t^{N1} \ll V_t^{N2}$ after irradiation (since on-nMOS experiences a larger threshold voltage shift than on-pMOS, i.e., nMOS dominant). This preserves the power-up state as explained in [11], reinforcing PUF stability. In contrast, if the cell is irradiated in its inverted PUF state (N_1 : off and N_2 : on), we can expect $\Delta V_t^{N2} > \Delta V_t^{N1}$, which may lead to $V_t^{N1} > V_t^{N2}$ after irradiation. This will flip the preferred power-up state leading to a higher HD%, as observed in Cypress chips.

The behavior of the ISSI and Alliance chips is explained in Fig. 4(b). In contrast to the Cypress chips, we assume that the Alliance and ISSI chip's postradiation power-up characteristics are predominantly determined by the pMOS transistors, as noted in [13]. In other words, for a preferred power-up state of $/\bar{Q} = 0/1$, if the cell is exposed in its PUF state (P_1 : off and P_2 : on), we can expect $|\Delta V_t^{P2}| > |\Delta V_t^{P1}|$, potentially leading to $|V_t^{P1}| < |V_t^{P2}|$ after irradiation. This would result in switch of the preferred power-up state of the cell, leading to a higher HD% after irradiation. Cui et al. [13] reached a similar conclusion regarding the explanation of reverse pattern imprinting after irradiation. In contrast, if the cell is exposed in its inverted state (P_1 : on and P_2 : off), we can expect $\Delta V_t^{P1} > \Delta V_t^{P2}$ resulting in $|V_t^{P1}| \gg |V_t^{P2}|$ after irradiation. This would preserve the power-up state. More importantly, this stabilizes the power-up state of memory cells that show unstable power-up characteristics. Hence, the HD% of the PUF will decrease after irradiation as observed for the ISSI and Alliance chips after TID = 10 krad (Si).

Based on the aforementioned explanation, we propose that TID effects cause an asymmetric V_t shifts between nMOS and pMOS transistors, as reported in [11] and [13].

Specifically, in the Cypress chip, the TID-induced threshold voltage reduction in the on nMOS transistor is more pronounced compared to the on pMOS transistor. Conversely, the ISSI and Alliance chips exhibit the opposite trend. Please note that the specific properties of individual transistors within the SRAM memory arrays are proprietary, preventing us from confirming our hypothesis. Nonetheless, our explanations and hypothesis offer a straightforward yet consistent framework for understanding the TID effects on the power-up characteristics of SRAM memory. In general, both nMOS and pMOS transistors' mismatch can simultaneously affect the power-up transients. Consequently, a more detailed modeling framework is required to predict the TID effects on SRAM PUF characteristics for a broader TID range [18].

C. Technology-Node Versus TID Effects on PUF

In this section, we compare the PUF response of different Cypress SRAM chips manufactured using 65-, 90-, and 150-nm technology nodes (see Table II for chip details). Fig. 5(a) and (b) shows the HD% and unstable cells% as a function of TID, respectively. We find that SRAM PUFs from smaller technology nodes show a higher HD% and unstable cells% before irradiation than the corresponding ones manufactured using larger technology nodes. This can be explained by a higher vulnerability of smaller node SRAM cells to thermal noise. The 65-nm chip shows the highest resilience to radiation (with the smallest slope) beyond 25 krad(Si). The 90-nm chip performs the second best with a gradual but less steep slope when compared to the 150-nm sample.

TABLE II
SUMMARY OF CHIP SPECIFICATION

	Cypress 150 nm	Cypress 90 nm	Cypress 65 nm	ISSI 110 nm	Alliance 200 nm
Part Number	CY7C1041CV33	CY7C1041DV33	CY7C1041G30	IS61WV25616BLL	AS7C34098A
Capacity	4 Mb	4 Mb	4 Mb	4 Mb	4 Mb
Input voltage	−0.5 V to 4.6 V	−0.3 V to 4.6 V	−0.5 V to 3.8 V	−0.3 V to 3.9 V	−0.5 V to 3.8 V
Word size	16 bits	16 bits	16 bits	16 bits	16 bits
Temperature	−40 °C to +85 °C	−40 °C to +85 °C	−40 °C to +85 °C	−40 °C to +85 °C	0 °C to +70 °C
Timing	10 ns	10 ns	10 ns	10 ns	10 ns

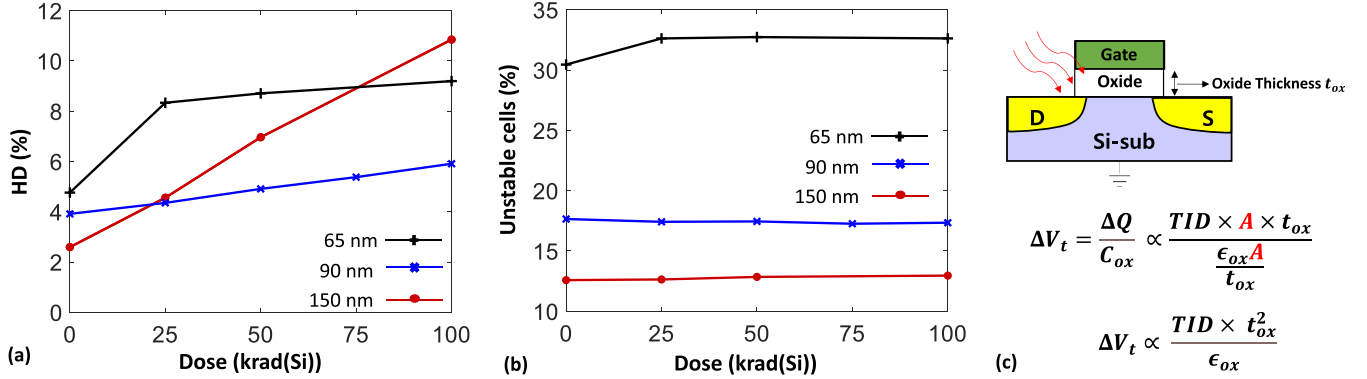


Fig. 5. TID effects on different technology nodes. (a) HD%. (b) Unstable cells%. (c) Threshold voltage change as a function of oxide thickness.

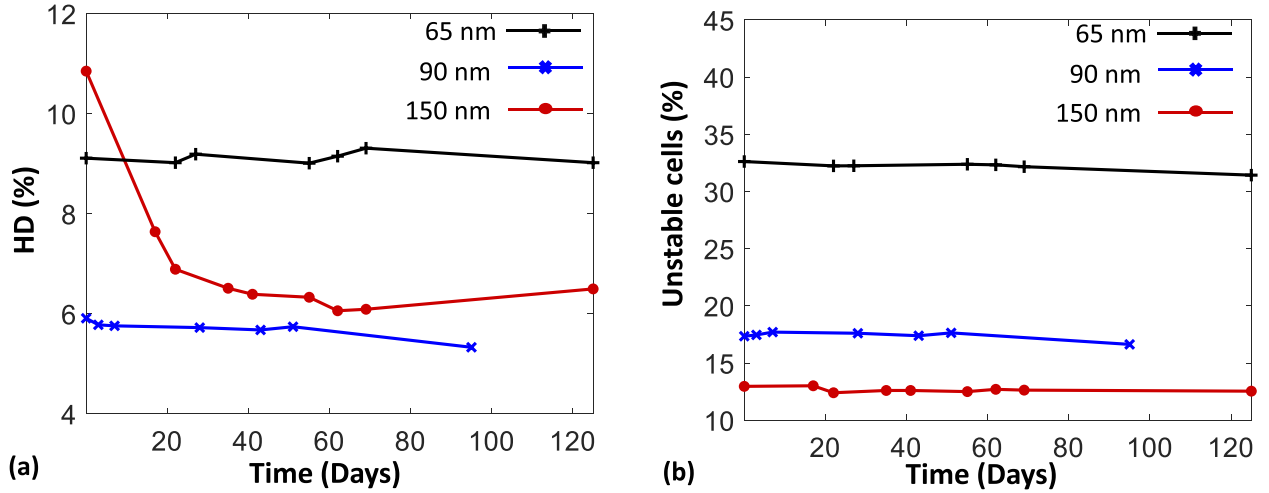


Fig. 6. Effects of room-temperature annealing on SRAM PUF. (a) HD (%) and (b) unstable cell (%) are plotted as a function of anneal duration. The chips were kept in the unpowered state with all pins grounded during annealing.

The 150 nm shows the highest increase in HD% overall. This result suggests that even though smaller cells are more susceptible to thermal noise, they may be less affected by TID. We can explain this through the equations in Fig. 5(c). We see that the TID-induced change in the threshold voltage (ΔV_t) depends on the square of the oxide thickness (t_{ox}), i.e., $\Delta V_t \propto t_{ox}^2$. The 65-nm chip will have the smallest gate oxide thickness, resulting in the gentle HD% slope after TID = 25 krad(Si). The 150-nm chip will have the thickest gate oxide layer resulting in the highest change in V_t values of its constituent transistors. Thus, the SRAM PUFs from 150-nm node

chips exhibit the highest HD% after a TID of 100 krad(Si). The 65-nm chip starts at the highest HD% and also a significantly higher unstable cells% compared to the 90-nm chip, possibly accounting for the steep rise in HD% between 0 and 25 krad(Si). Note that there could be more factors at play, for example, trap location (oxide versus oxide-interface traps), but these are believed to be less impactful in nanoscale devices [19]. From our analysis, it appears that the 90-nm technology node offers a good balance between TID resistance and initial HD%, suggesting its use could be more suitable for TID prone environment.

D. Room Temperature Anneal

In this study, we allow the irradiated chips from various technology nodes to anneal over time at room temperature. The chips are kept grounded during the anneal. From previous works, we can expect a decrease in the overall HD% due to small threshold voltage regression [18], [20], [21]. Fig. 6(a) and (b) shows the HD% and unstable cell% as a function of annealing time, respectively. Expectedly, the HD% decreases over time. However, even after an extended period of annealing, the HD% is significantly higher than the preirradiation baseline. The 150-nm chip that showed the highest increase in HD% also shows the highest degree of annealing. Despite a higher degree of annealing from the 150-nm sample, the 90-nm chip shows the best HD% performance for the same reasons discussed in Section IV-C. The unstable cells% remain relatively unchanged even after an extended period of time.

V. CONCLUSION

In summary, our key findings are as follows.

- 1) The data stored in the SRAM memory array during irradiation impact postirradiation power-up states. The cells containing either their default power-up state or the inverted power-up state are more immune to TID effects, contingent on their physical properties. For Cypress chips, holding the PUF state during irradiation proves effective in reducing PUF degradation, while in the case of ISSI and Alliance chips, holding the inverted PUF state proves advantageous.
- 2) Chips manufactured using smaller technology nodes (90 and 65 nm) seem to exhibit greater resilience to TID effects compared to those manufactured using larger technology nodes (150 nm). However, due to higher instability in power-up transients of cells in smaller technology nodes, striking a balance between baseline performance and radiation response is crucial.
- 3) A room temperature anneal of chips in the grounded state reduces the HD% of the irradiated chips, approaching its preirradiation level over a span of several months.

Armed with these insights, we can make more informed choices in the parts selection phase of the design of systems operating in space and other radiation-prone environments. Through meticulous prior characterization, we can proactively counteract the effects of TID on the integrity of SRAM PUFs by priming a specific location of the SRAM array reserved for PUF with the appropriate data patterns. These findings will help further solidify the use of SRAM PUFs in radiation-prone environments.

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