Subtractive Microfluidics in CMOS

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***Abstract*—**This paper introduces a microfluidics platform embedded within a silicon chip implemented in CMOS technology. The platform utilizes a one-step wet etching method to create fluidic channels by selectively removing CMOS back-end-of-line (BEOL) routing metals. We term our technique "subtractive" microfluidics, to complement those fabricated with additive manufacturing. Three types of structures are presented in a TSMC 180-nm CMOS chip: (1) passive microfluidics in the form of a micro-mixer and a 1:64 splitter, (2) fluidic channels with embedded ion-sensitive field-effect transistors (ISFETs) and Hall sensors, and (3) integrated on-chip impedance-sensing readout circuits including voltage drivers and a fully differential transimpedance amplifier (TIA). Sensors and transistors are functional pre- and post-etching with minimal changes in performance. Our CMOS subtractive microfluidics technique enables tight integration of fluidics and electronics, paving the way for future small-size, high-throughput lab-on-chip (LOC) devices.

I. Introduction

Integrating microelectronics with microfluidics, especially those implemented in silicon-based CMOS technology, has driven the next generation of *in vitro* diagnostics. This CMOS/microfluidics platform offers close interfaces between electronics and biological samples and tight integration of readout circuits with multi-channel microfluidics, both of which are crucial factors in achieving enhanced sensitivity and detection throughput. Importantly, conventionally bulky benchtop instruments are now being transformed into millimeter-sized form factors at low cost, making the deployment for Point-of-Care (PoC) applications feasible [1-2].

Conventional CMOS/microfluidics integration has typically followed a "modular" approach, where the CMOS electronics package and the microfluidics are prepared separately and then attached through in-house assembly [3-4]. However, such an approach suffers from significant misalignment between the microfluidics and the sensing transducers on the chip, especially when the transducer sizes are reduced or the microfluidic channel width shrinks. The full potential of CMOS parallel readout has not been fully realized.

This work proposes a novel CMOS/microfluidics system utilizing "subtractive" manufacturing. The idea is to use the metal routings from the standard back-end-of-line (BEOL) in the CMOS process as a sacrificial layer for the microfluidic channel after complete wet-etching-based removal (Fig. 1). This method allows for direct and tight integration of fluidic channels with readout and control circuits, mitigating the aforementioned misalignment issues. By taking advantage of the fine-line lithography in CMOS foundries, our approach easily promotes high channel counts and enables direct scaling of the microfluidics geometry toward sub-micron levels. In this paper, we discuss the issues encountered in the subtraction process, our corresponding solutions, and demonstrate the successful implementation of subtractive microfluidics in CMOS, including (1) a 1:64 fluidic splitter and a micro-mixer, (2) on-chip ion-sensitive field-effect transistors (ISFET) and Hall sensors, and (3) subtractive microfluidics with functional impedance sensing readout circuits. To the authors best knowledge, this is the first demonstration of subtractive microfluidics with CMOS active circuits.

II. Post-CMOS Process and System Assembly

A. Etching complex fluidic structures

Etching the metallization in CMOS to form fluidic channels with acidic etchants is a non-trivial process. The etch rate can be significantly reduced due to diffusion limits, especially when there are only two access ports: the inlet and the outlet. Previously, our group leveraged hydraulic pressure to promote turbulence and enhancing diffusion rates, which sped up the etch rate by 10× [5]. However, we also found that for complex microfluidic structures, such as the meander micro-mixer and fluidic splitters at high splitting ratios (N > 16), complete removal is nearly impossible, even with multiple days of incubation in the etchant at elevated temperatures. In this paper, we solve the issue by adding small "pad openings" along the fluidic channels to introduce more access ports (Fig. 2). To prevent fluid leakage from these ports, we further sealed these openings using PDMS microfluidics in the final system assembly as discussed in II.B. Fig. 3 shows successfully etched micro-mixer and 1:64 fluidic splitter designed in 180-nm CMOS with successful function demonstration. Note that these extra openings can create pockets to trap air. We dissolve these air bubbles into the medium by applying hydraulic pressure for 15 minutes.

We include on-chip resistive heaters (unsalicided polysilicon) to perform localized and controllable etchant heating. Our experiments show that our assembly (described in the next subsection) can achieve a chip temperature of 110°C at ~0.53W of electrical power (from IR camera). By keeping the temperature slightly higher than 65°C, the etchant activation temperature, full M6 removal of a single 400-µm long 6-µm wide channel takes ~18hr while the 1:64 fluidic requires 20hr.

B. System assembly

Fig. 4 illustrates the system assembly process. First, the CMOS die is embedded inside a PCB using biocompatible epoxy (Epo-Tek 302-3M). Next, the CMOS pads are wirebonded to the PCB, and the bonds are encapsulated with epoxy. During this step, a PDMS slab protects the CMOS surface to prevent overflow. Third, part of the CMOS chip is protected with Kapton tape, followed by the application of PDMS microfluidics for etchant delivery. Finally, a different

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PDMS microfluidics, molded from 50-µm thick SU-8 photoresist, are used for delivering biofluids.

III. Integrated ISFETs

The ISFETs are implemented using thick-oxide NMOS transistors with a W/L ratio of 1µm/350nm. Their gates are extended to M5, which is isolated from the fluidic channel layout in M6 using the default 1-µm thick oxide from the foundry. This dielectric layer also serves as a charge-sensing membrane. The sensor area is defined by the area of M5. Two ISFETs are implemented in the same fluidic channel with M5 areas of 6 µm × 12 µm and 6 µm × 24 µm, respectively. This area difference results in different coupling capacitances and, consequently, different attenuation factors formed by the capacitive dividers, as represented by the equivalent schematic in Fig. 5. Our analysis shows a worst-case attenuation factor of 0.55× compared to the ideal Nernst equation when sensing pH (59mV/pH sensitivity). The ISFETs' drain currents are measured with an off-chip transimpedance amplifier (TIA) using TI's OPA4354. The gate voltage is provided by a platinum (Pt) electrode (A-M Systems) in direct contact with the ionic solutions. The Pt potential is pulsed between 0 and 3V at 0.2 Hz to minimize the drifts through periodic resets. The nominal drain bias is set to 1.0V.

Fig. 6 shows the measurement results of microfluidics-embedded ISFETs at different pH levels from 4 to 10 using standard solutions from Hanna Instruments (HI5710-11PB). Two ISFETs are measured simultaneously, and their sensitivities are compared. The ISFET with a 2× larger M5 area demonstrated a 1.2× increase in sensitivity. Drift is indeed observed (Fig. 6(c)) but can be effectively canceled by performing a differential operation using a pair of ISFETs formed with NMOS and PMOS [10]. Fig. 6(d) shows the power spectral density (PSD) of the current noise at ISFET output. Our measurements show a flicker noise corner of 30 kHz, a combined contribution from both ISFETs and chemical noise.

IV. Integrated Hall Sensors

The Hall sensors are implemented using N-well resistors having a width of 5 µm. Two different layout styles are implemented for study purposes (Fig. 7(a)). To maximize sensitivity, the microfluidics for the Hall sensors are implemented in the lower M2 (width = 10 µm) instead of M6. Note that our etching technique can remove metal down to M1, as shown in Fig. 7(b). The Hall sensors are biased at 1.0V and the Hall voltages are measured using instrumentation amplifiers (TI's INA823) at a gain of 1000 V/V, followed by oscilloscope captures. A thin on-chip M2 wire is routed in proximity to the Hall sensor to electromagnetically modulate the magnetic fields locally for sensor calibration. Since the fluidic channel is located in M2 (thickness = 0.53 µm), the device requires the longest time to complete metal removal (> 3 days).

Fig. 8 shows the Hall sensors responses to different magnetic fields (0 ~ 5mT, generated by running DC currents in the on-chip routing in proximity to the Hall sensors) before and after metal etching. Consistent sensitivity is observed, but the etching process appears to introduce extra offset voltages. Fortunately, this offset voltage can be compensated through circuit techniques such as correlated double sampling (CDS). The successful embedding of Hall sensors opens the way for flow cytometry using magnetic beads or nanoparticles as labels.

V. Integrated Impedance Readout Circuits

Fig. 9 shows the schematic of the fully-differential impedance readout circuits. The most unique aspect of our design is the use of "vias" between M5 and M6 (Via56) to form liquid-interfacing electrodes, exposed by removing the M6 fluidic channel [5]. We have demonstrated in [5] that these via electrodes can achieve more stable recording compared with Ag/AgCl pseudo reference electrodes. To avoid over-etching, we monitor the electrode impedance in real-time with the on-chip impedance-sensing circuit and stop the etching once an "open" circuit is observed from the readout. Slight over-etching is inevitable, yet our measurements indicate that the electrode stability can still be maintained. Other circuits include two unity-gain buffers delivering a differential sinusoidal drive of 0.4 V_{pp} at 100 kHz to the electrodes and a resistive-feedback TIA with a current-reuse cascode amplifier (Fig. 10). The TIA consumes 0.4 mA from a 1.8-V supply and has a bandwidth of 1.2 MHz, set by the R (= 1 MΩ) and C (= 133 fF) in the feedback network. The measured input-referred noise current is 0.15 pA/$\sqrt{\text{Hz}}$. The buffer employs a two-stage architecture to maximize the voltage swing while consuming 0.25 mA of current each. The output is oversampled and demodulated off-chip numerically in Matlab.

Fig. 11 shows the photo of the subtractive microfluidics with on-chip impedance sensing circuits and its testing setup. Fig. 12 plots the measured impedances (|Z|@100kHz|) of saline buffers at different ionic strengths (from 1× to 5×). The results are repeatable across two additional devices, verifying functional circuits post-etching. The measurements indicate higher noise at high ionic strengths, showing that the major noise source in the system could be the chemical noise at the liquid-solid interface. Future applications include rapid detection of single bacteria cells in flow

VI. Conclusions

This paper presents the subtractive microfluidics concept in CMOS technology. We leverage the fine-line lithography capabilities offered by the semiconductor foundries and a single-step wet-etching process and embed microfluidic channels within a silicon chip in close proximity to the sensing electronics, showcasing the potential for tightly integrated, high-performance lab-on-chip devices. Table I. provides a comparison to the other prior works.

Acknowledgment

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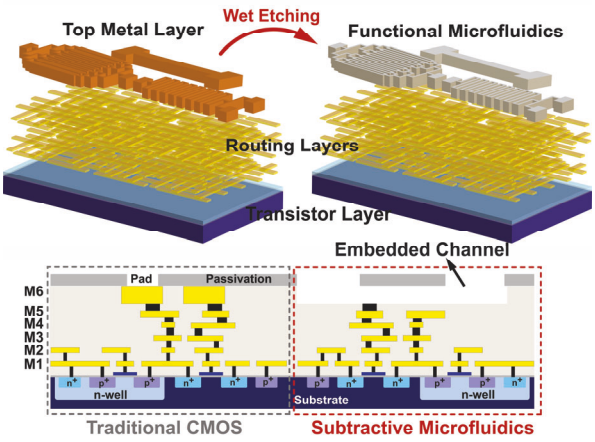

Fig. 1. CMOS subtractive microfluidics concept,

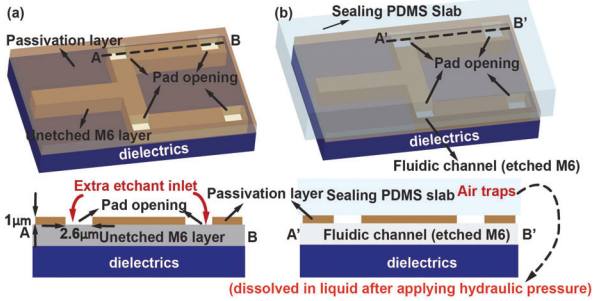

Fig. 2. (a) Distributed pad openings along top metal layers to increase the etching efficiency. (b) The open holes are sealed with PDMS. The trapped airs are dissolved in the solutions with the aid of hydraulic pressure.

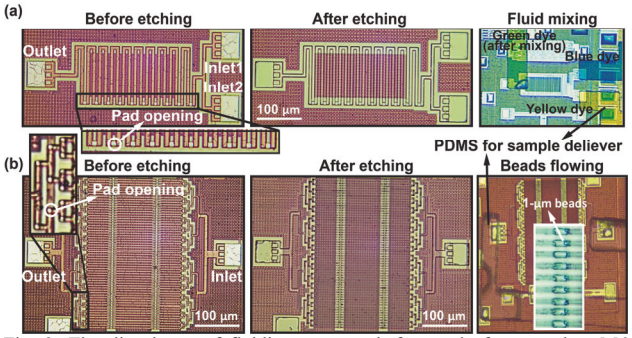

Fig. 3. The die photos of fluidic structures before and after complete M6 removal. (a) A micro-mixer mixes a blue and yellow dye solutions. (b) A 1:64 fluidics splitter for parallel sensing. The channels are loaded with 1-μm beads.

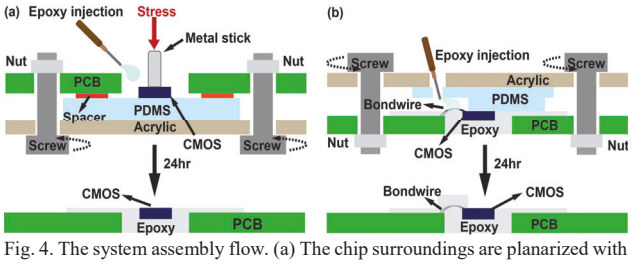

Fig. 4. The system assembly flow. (a) The chip surroundings are planarized with the aid of biocompatible epoxy and a PDMS slab. (b) Bonding wires protection.

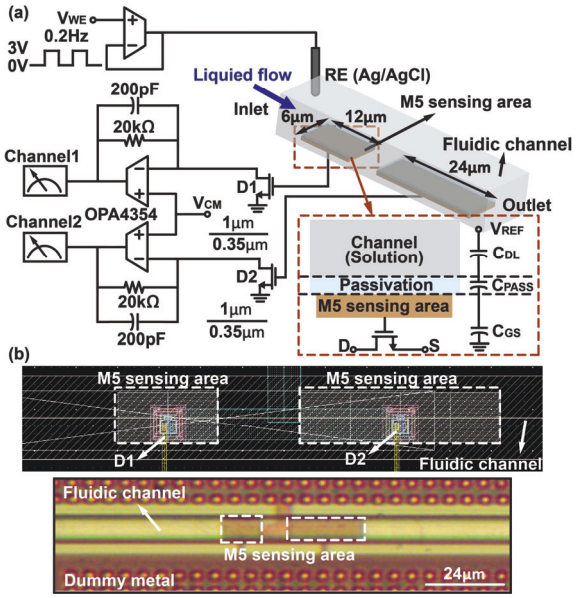

Fig. 5. Subtractive microfluidics with integrated ISFET sensors. (a) The schematic and the test setup. We use the inter-metal dielectric at the bottom of the M6 fluidic channel to perform charge sensing. An equivalent circuit model is provided. (b) The ISFET layout and the device micrograph.

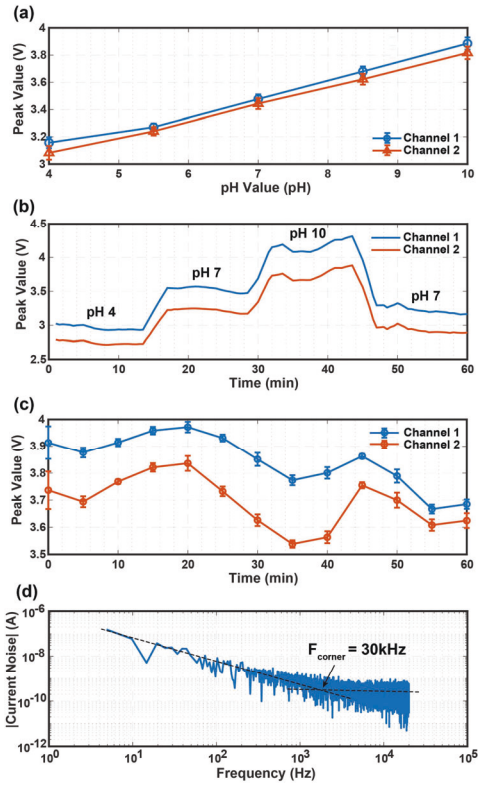

Fig. 6. (a)(b) Measured pH responses from the two ISFETs. (c) Long-term recording showing drifts that mandates differential ISFETs operation. (d) The noise current power spectral density referred to the ISFET output.

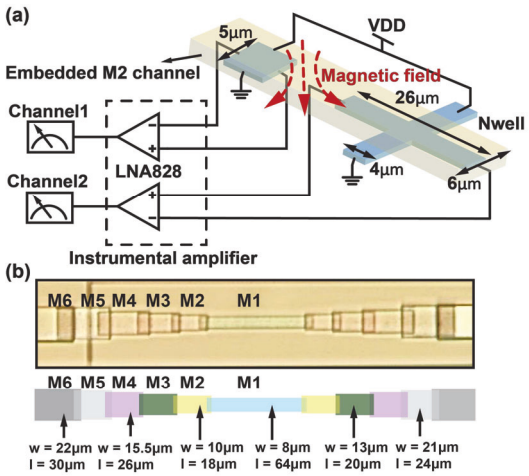

Fig. 7. (a) Hall effect sensing schematic. (b) Using a metal ladder, the lower metal layers can be successfully removed, creating a fluidic channel that is closer to the Hall sensors implemented with N-well resistors.

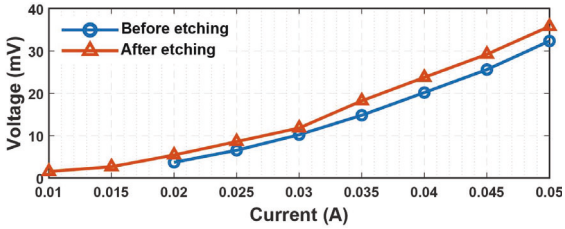

Fig. 8. Measured Hall sensor responses with respect to different magnetic fields. The fields are generated electromagnetically through DC current from adjacent wires. The measured sensitivity is ~8mV/mT.

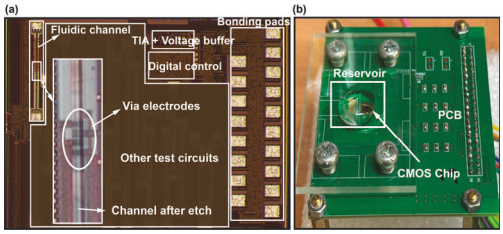

Fig. 11. (a) Chip die photo and the etched fluidics with via electrodes. (b) The measurement setup. A PDMS is used only for sample delivery.

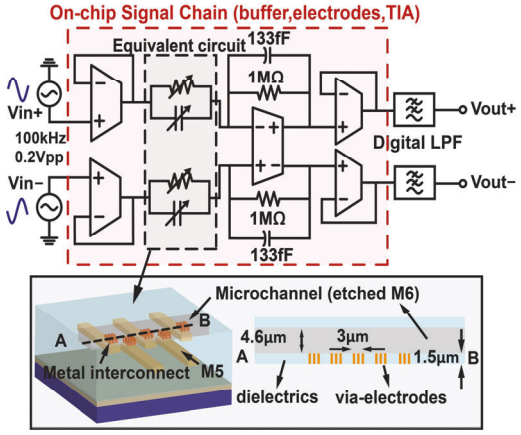

Fig. 9. Subtractive microfluidics with integrated impedance readout circuit. "Vias" for connecting M6 and M5 are used as sensing electrodes. A fully-differential readout is chosen to maximize power supply rejection ratio.

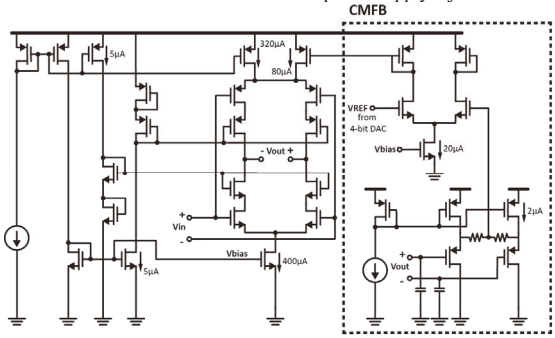

Fig. 10. The schematic of the amplifier in the TIA.

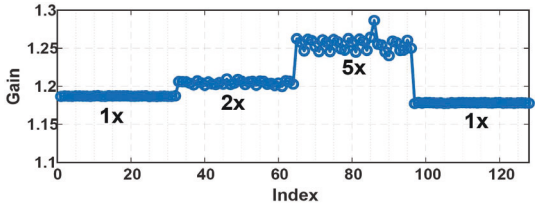

Fig. 12. Impedance sensing of saline buffers at different ionic strengths.

Table I. A comparison between different CMOS-microfluidics platforms.

	This work	[6]	[7]	[8]	[9]
Technology	**180-nm CMOS**	180-nm CMOS	250-nm BiCMOS	Wafer-level	65-nm CMOS
Fluidic channel cross-sectional dimension	**6 μm × 0.53m**	4.6 μm × 4.6 μm	375 μm × 700 μm	42 nm × 5 nm	60 μm × 60 μm
Microfluidics process	**BEOL wet etch (Top-down)**	BEOL wet etch (Top-down)	Wafer-bonding (Modulus)	Lithography (Bottom-up)	PDMS on PCB (Modulus)
Alignment requirement	**No**	No	Yes	Yes	Yes
Critical process steps	**1**	1	> 5	> 10	> 2
Integrated Sensors	**1. ISFET for pH sensing 2. Hall sensors 3. AC impedance sensing (100kHz) for liquid differentiation**	E. Coli DC Resistive-pulse sensing	Liquid differentiation using millimeter-wave dielectric spectroscopy	DNA manipulation	Label-free flow cytometry using microwave dielectric-spectroscopy
Integrated circuits	**Yes**	No	Yes	No	Yes