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Performance and Characterization of Additively Manufactured BST Varactor Enhanced by Photonic Thermal Processing

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Abstract: The demand for reconfigurable devices for emerging RF and microwave applications has been growing in recent years, with additive manufacturing and photonic thermal treatment presenting new possibilities to supplement conventional fabrication processes to meet this demand. In this paper, we present the realization and analysis of barium–strontium–titanate-($Ba_{0.5}Sr_{0.5}TiO_3$)-based ferroelectric variable capacitors (varactors), which are additively deposited on top of conventionally fabricated interdigitated capacitors and enhanced by photonic thermal processing. The ferroelectric solution with suspended BST nanoparticles is deposited on the device using an ambient spray pyrolysis method and is sintered at low temperatures using photonic thermal processing by leveraging the high surface-to-volume ratio of the BST nanoparticles. The deposited film is qualitatively characterized using SEM imaging and XRD measurements, while the varactor devices are quantitatively characterized by using high-frequency RF measurements from 300 MHz to 10 GHz under an applied DC bias voltage ranging from 0 V to 50 V. We observe a maximum tunability of 60.6% at 1 GHz under an applied electric field of 25 kV/mm (25 V/μm). These results show promise for the implementation of photonic thermal processing and additive manufacturing as a means to integrate reconfigurable ferroelectric varactors in flexible electronics or tightly packaged on-chip applications, where a limited thermal budget hinders the conventional thermal processing.

Keywords: barium–strontium–titanate (BST); interdigitated capacitors; additive manufacturing; spray pyrolysis; photonic sintering

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1. Introduction

Additive manufacturing (AM), also commonly referred to as 3D printing, has revolutionized the way we create complex structures and components and has become a major cornerstone in research and development in recent years. While the term 3D printing has become almost synonymous with fused deposition modelling (FDM), AM encompasses a large selection of technologies including a wide range of deposition techniques, such as micro dispensing, binder jetting, inkjet printing, aerosol jet, as well as the aforementioned FDM, just to name a few. However, it is also often seamlessly combined with other technologies and techniques, such as localized laser processing, in situ UV curing, micromilling, photonic thermal processing, etc., which are used for the fabrication of complex multidimensional structures and allow for the postprocessing of deposited materials and individual layers [1–5]. These technologies can not only be combined with each other to create new processes or improve upon existing ones, but can, and have been, integrated together with conventional fabrication technologies as part of hybrid co-designs, which leverage the strengths of each set of technologies to address challenges faced by conventional fabrication [2,4–7]. For example, this hybrid approach has allowed for the incorporation of integrated bypass capacitors into a wideband chip carrier to ensure a clean

and stable power source to an amplifier die [6] and the use of unconventional geometries, along with selective material deposition, to address thermal management when packaging amplifiers [7].

Such techniques have already been implemented in the fabrication of other perovskite materials for optoelectronics, where AM has paved the way for the design and fabrication of fully 3D structures for the purpose of improving tailoring to meet specific needs and systems, thus addressing the limitations of the planar structures of conventional fabrication [8–10]. This fabrication approach has allowed for greater versatility of design, with some of the main advantages including the ability to generate 3D structures and the design-to-manufacturing flexibility offered by many of these AM techniques. Among the numerous applications of AM in electronics, for the purpose of this work, the main focus is on reconfigurable devices, circuits, and systems, all of which can be realized through various mechanisms such as mechanical microfluidic actuation or by implementing materials such as ferroelectric, ferromagnetic, and meta-materials. The exact mechanism through which each category of material can be reconfigured, or tuned, varies greatly and so does their implementation into functional electronic devices [11–13].

This work focuses on ferroelectric materials for reconfigurable device applications, more specifically barium–strontium–titanate (BST), which has received extensive research attention due to its interesting properties. BST, as a ferroelectric material, has a Curie temperature that can be directly modified by changing the Ba:Sr ratio in its stoichiometry. It has both a high dielectric constant and piezoelectric properties, which can be tuned using an external electric field, and displays low dielectric loss tangential losses, all of which can be further tailored by changing the stoichiometry and introducing dopants [6,7,14–21], therefore making BST an attractive material for reconfigurable high-frequency applications. Prior research on BST has focused on the characterization and implementation of devices in various fields including optics, communications, and RF and microwave [6,7,15–21]. Besides its use for RF electronics, BST shows potential for other applications such as magnetic sensors. The most common way to achieve that is by iron (Fe) doping the BST to exhibit the desired multiferroic and magnetic properties. Both [22,23] examined the effect of Fe doping level on the average crystal size, the expansion of the BST unit cell, the ferroelectric, magnetic, and optical properties, and the dielectric constant and losses up to 1 MHz. Enriching BST's capabilities to allow the sensing of a magnetic field can lead to the employment of BST in a magnetic field sensor for various applications. In that sense, researchers have also been exploring the sensor applications of magnetic ceramics by using materials such as strontium hexaferrite. For instance, Safronov et al. [24] reproduced biological tissues using ferrogels containing micron-sized magnetic particles and developed a prototype magnetic field magnetoimpedance sensor. Another promising application to magnetic field sensing, demonstrated by Yang et al. [25], for detecting cardiac biomarker myoglobin (Mb) is conducted by using an integrated giant-magnetoimpedance (GMI)-based immunosensor.

Prior work has shown that, among various parameters, the crystalline structure of the deposited BST is a primary contributor, determining the effective dielectric permittivity and tunability. To ensure that the BST films are not in an amorphous state and realize the desired crystalline microstructure, BST films are deposited either at very high temperatures or at lower temperatures and then annealed. The most common annealing method reported in the literature involves the use of rapid thermal annealing (RTA) and high temperature furnace annealing at typical temperatures of 700–850 °C for up to multiple hours. These processing methods, while convenient, pose many limitations for flexible electronics, on-chip, and high-density packaged designs due to the thermal budget. Substantial research has been conducted to address these limitations, including the use of UV-wavelength radiation via excimer laser to improve the quality of low-temperature-deposited BST films and promote crystal grain growth [26–29]; however, laser annealing has a limited throughput due to spot size limitations, and these studies have required substrate temperatures in the range of 200–300 °C during either BST film deposition or annealing, making them

unsuitable for integration with the majority of thermoplastics commonly used in AM packaging and flexible electronics. In the case of AM or BST, some prior works have used inkjet printing on alumina substrates to allow for sintering at temperatures upward of 1150 °C to circumvent thermal budget limitations [30,31]. Ranasingha et al. [32] demonstrate the good performance of sinterless-aerosol-jet-deposited BST nanoparticles, but the performance still falls behind that of sintered BST [32]. This work, therefore, aims to fill a gap in the literature with respect to the low-temperature sintering of BST films with the aid of AM techniques. To realize additively manufactured BST films at low temperatures with a performance comparable to that of fully furnace-sintered films, we leverage the increased radiation absorption of nanoparticles that is due to their high surface-area-to-volume ratio combined with photonic sintering to sinter the surface BST coating without causing a significant temperature increase in both the substrate and the metallization layer underneath. This allows for greater flexibility when integrating ceramic films, which require thermal processing for the best performance, into flexible electronics, complex 3D structures, and high-density electronic packaging designs without a significant thermal budget limitation.

The two main design topologies used for the integration of ferroelectric materials in capacitive devices found in the literature are parallel plate implementations and interdigitated designs [16,33,34]. Parallel plate implementations consist of a metal–insulator–metal (MIM) topology where the ferroelectric material is sandwiched between two electrodes, whereas the interdigitated capacitor (IDC) design consists of a planar metallic structure with multiple overlapping fingers. The MIM topology has the advantage of allowing a large and more uniform electric field concentrated in the active ferroelectric layer; however, it comes with a more complex multilayer fabrication process, a greater dependance on the electrode quality, and is more prone to resonant resistive effects [16,33,35,36]. The IDC topology, on the other hand, consists of a single-layer planar structure typically fabricated directly on top of or underneath the ferroelectric layer. However, due to the resolution limits of conventional photolithography, IDC devices generate a lower electric field when using an equivalent bias voltage compared to a MIM device. This limitation can be addressed by using the high resolution of nanolithography to reduce the finger gap, as shown in [16]; however, this form of lithography adds greater complexity to the fabrication and requires more tools, which are not as readily available as those used for conventional photolithography. For these reasons, we decided to fabricate an IDC design to test the RF performance of our BST films.

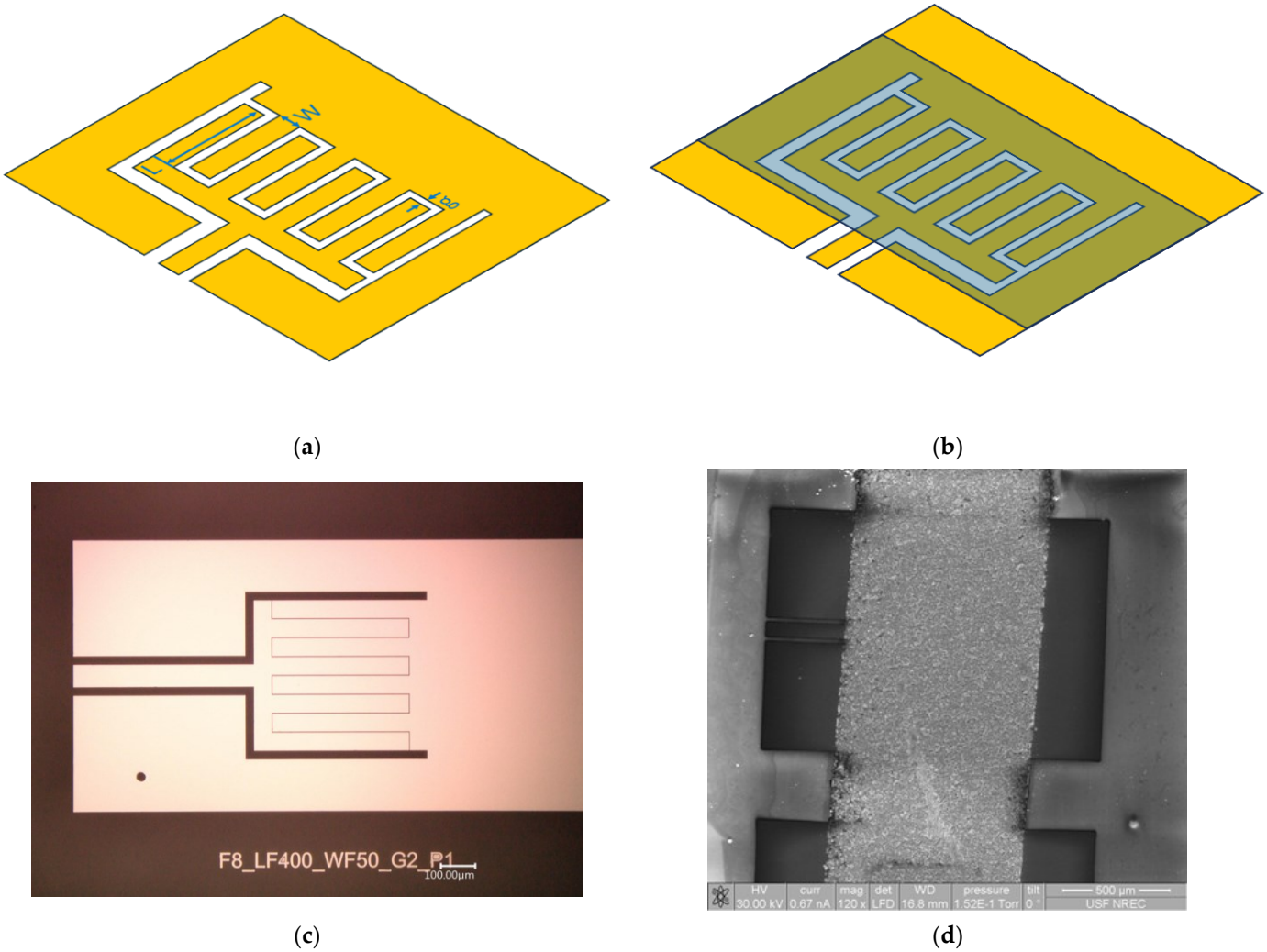
In this work, we report the initial results of our study on BST capacitors fabricated with a mix of conventional lithography for the electrode layer and AM techniques, using ambient air spray pyrolysis deposition of suspended BST nanoparticles, which are further enhanced by localized sintering and crystallization via photonic thermal processing. The device performance is evaluated using S-parameter measurements from 300 MHz to 10 GHz under a bias voltage range from 0 V to 50 V, from which the capacitance, tunability, and permittivity are extracted using equations. The deposited films are evaluated qualitatively using SEM imaging and XRD measurements. We demonstrate effective photonic sintering and initial crystallization of the deposited film, which achieves a performance comparable to that of BST devices thermally processed using conventional techniques without the need to expose the electrode and substrate layers to high temperatures for extended periods of time.

2. Materials and Methods

2.1. Capacitor Design and Fabrication

The initial designs of the fabricated devices were taken from [16] and were modified to better suit our fabrication process. The full layout design consisted of devices with four, six, eight, 10, and 14 interdigited fingers, each having a version with 2 µm, 5 µm, 10 µm, and 20 µm finger gaps and each exhibiting both one-port and two-port configurations. In this work, we present the measured results for the eight-finger one-port configuration, as depicted in Figure 1a,b, which has a finger length of L = 400 µm, a finger width of

W = 50 µm, and a gap of g = 2 µm. This particular configuration was preferred for a number of reasons. First of all, the one-port configuration is not only easier to measure, but also allows for accurate extraction of the performance parameters. Second, the 2 µm gap is the smallest we could consistently fabricate with conventional lithography methods and, thus, provides the highest electric field under a certain level of applied bias voltage potential. Third, the eight-finger configuration is right in the middle of the range of designs, thus providing a measurement of the median capacitance and operating frequency range. As it can be seen in Figure 1c,d, the complete device consists of the IDC as well as a segment of coplanar waveguide (CPW) line, which serves as a landing pad for our ground–signal–ground (GSG) probes employed for the RF measurement. The CPW line was designed to be longer than its typical design as a compromise to allow for some degree of misalignment during the masking process, which is used during the BST deposition. The complete dimensions for the measured design can be found in Table 1.



(**a**) (**b**)

(**c**) (**d**)

Figure 1. (**a**) Diagram of IDC device fabricated with key dimensions labeled; (**b**) diagram depicting how BST is deposited to only cover the finger area; (**c**) microscope image of fabricated electrode layer; (**d**) SEM image of a device after BST deposition.

Table 1. A set of key design dimensions for the measured IDC device.

Dimension	Size (μm)
Finger length	400
Finger width	50
Finger gap	2
Interconnect width	50
Feedline width	65
CPW gap	25
Feedline length	500
CPW ground width at IDC region	150

The electrodes were fabricated on top of a Pyrex substrate with a thickness of 500 μm by means of conventional cleanroom microfabrication techniques. A lift-off process with positive photoresist was used to pattern the metallization layer, along with RF sputtering, to deposit 300 nm gold electrodes on top of a 30 nm chrome adhesion layer.

2.2. BST Deposition and Thermal Processing

The BST solution was purchased from TPL inc. and it consisted of 50 nm BST particles suspended in an ethylene glycol solution. The particles had a $Ba_{0.5}Sr_{0.5}TiO_3$ stoichiometry and accounted for 49% of the weight of the solution. The solution was deposited using an ambient spray pyrolysis setup, as illustrated in Figure 2. As seen in the diagram, the die with the deposited electrodes was placed on top of a hot plate, which was mounted on a single axis motorized stage. The die was masked using the Kapton tape to cover the feedlines for probing, leaving only the main IDC finger area exposed for deposition, as seen in Figure 1b,d. Before deposition, the solution was placed in a centrifugal planetary mixer (ARE-310 Thinky Mixer) to break down any particle agglomerations and ensure homogeneity. It was then loaded into an Iwata HP-TH2 airbrush with a 0.06 mm nozzle connected to a commercial air compressor set to 35 psi and deposited on the IDC device die. The hot plate was maintained at a temperature of ~100 °C during deposition to begin the curing process and prevent overaccumulation of the liquid solution on the surface. To enhance the repeatability of the deposition process, the spray gun was kept at an approximate angle of 30° and at a height of 10 cm from the hot plate surface, the controller for the stage was set to a speed of 20 mm/s with an acceleration and deceleration of 80 mm/s^2, and the die passed below the spray region a total of ten times, with five passes in each direction to improve the uniformity of deposition. This process consistently yielded films with a thickness of approximately 18 μm and an average roughness of 2.5 μm. After deposition, the die was left on the hot plate for 2 min to promote the evaporation of most of the solvent before being put into a vacuum oven at 100 °C for 2 h to ensure that any trapped moisture and residual solvent evaporated. Initial attempts to fully cure the films with only the hot plate showed an increased likelihood of surface cracking and delamination of the films due to the rapid and uneven heating, while the sample was under a partially liquid state and occasionally still retained trapped moisture.

After the die was fully cured and dehydrated, the BST nanoparticles that made up the film were thermally processed using a PulseForge photonic thermal processing unit integrated into an nScrypt 3Dn-450-HP additive manufacturing platform. The PulseForge unit uses a flash lamp with a wavelength ranging from 200 nm to 1500 nm to produce high-energy broadband microsecond pulses, covering the UV to near IR range, to irradiate the surface layer and induce rapid transient heating of the top surface. The high surface-to-volume ratio of the BST nanoparticles increased the heat generated by these pulses, leading to high temperatures of the film layer and to the sintering of the nanoparticles, while the short length of the pulses ensured that the rise in temperature of the subsequent metal and substrate layers was mitigated. For the pulses, we used a 10 ms envelope made up of 10 pulses, with 50% duty cycle and a driving voltage of 300 V which generated a total energy of 4.44 J/cm^2. Because annealing is not a quick process, we exposed the films to a

total of 1000 repetitions of the envelope applied over five 200 pulse sessions to allow for the substrate to fully dissipate the heat and for the lamp to cool down and prevent overheating.

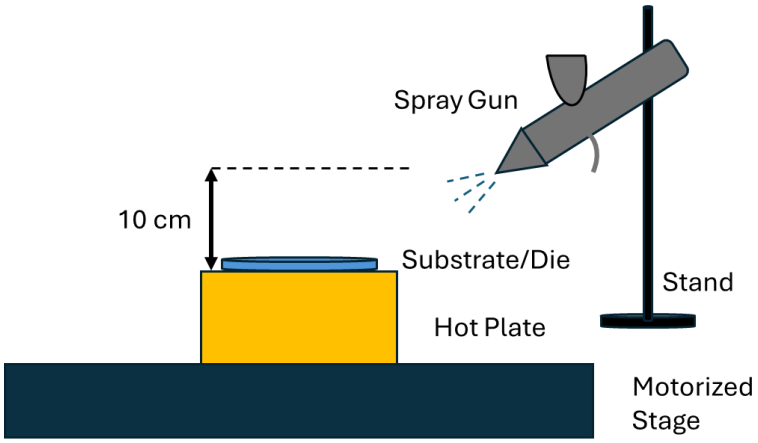


Figure 2. Diagram of ambient spray pyrolysis setup.

The high frequency RF performance of the fabricated devices was measured using a Keysight PNA N5227A (Keysight, Santa Rosa, CA, USA) vector network analyzer (VNA) with built-in bias tees rated for 250VDC and 2A. The GGB Model 40A GSG (GGB Industries Inc., Naples, FL, USA) probes with a 250 µm pitch size rated for 50 V were used and the biasing voltage was provided by a Rohde & Schwarz NGA100 (Rohde & Schwarz USA Inc., Columbia, IN, USA) power supply with a max DC output of 100 V and 2A per channel. A discreet series resistor of 1 MΩ was used between the power supply and the bias tee input as a precaution, serving as a current limiter in the event of a short circuit. Calibration was performed at 0 V bias voltage using a CS-5 calibration substrate and the one-port S-parameter frequency response of the device was measured over the range from 300 MHz to 10 GHz at various bias voltages from 0 V to 50 V. The voltage readout of the NGA100 has an accuracy of ± (<0.02% + 10 mV) and the accuracy of the CS-5 calibration substrate standards is ±0.25%.

The thickness and roughness of the deposited BST layers were measured using a C-BXT Bruker XT-A profiler. The deposited BST films were qualitatively assessed using XRD measurements and SEM imaging. SEM images were taken using a FEI Quanta 200 3D Dual Beam system (FEI Company, Hillsboro, OR, USA) under low vacuum conditions to mitigate electronic charge buildup. Due to the minimum film area required for the XRD measurements, a different sample had to be prepared. A BST film processed under the same processing conditions was deposited on a quarter of a 2-inch silicon wafer and measured using a Bruker D2 Phaser XRD (Bruker, Billerica, MA, USA).

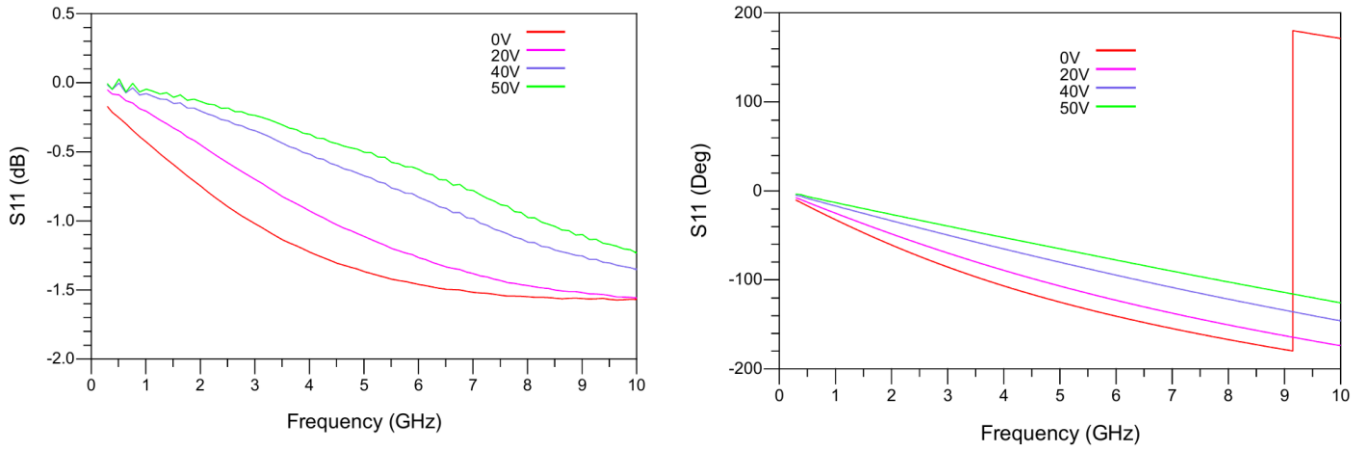
3. Results

3.1. High Frequency S-Parameter Measurments

As we increased the bias voltage applied to the capacitor, the dielectric constant of the BST decreased, in turn reducing the capacitance of the IDC. This decrease in capacitance led to an increase in the frequency at which series resonance occurs, as we can observe from Equation (1). This change in the self-resonance frequency was due to the fact that the contribution for the series inductance in the capacitor equivalent circuit originated from the metallization layer; thus, the inductance should remain largely unchanged in response to the increase in bias voltage [37]. We can observe from Figure 3a that the magnitude of the reflection coefficient increased along with the applied bias voltage, a phenomenon which was due to a decrease in the roll-off of the reactance of the device from the smaller capacitance. Also, as shown in Figure 3b, the device exhibited a series resonance at 9.2 GHz which was observed at 0 V. As seen in the literature [14–21], the dielectric constant of BST under an applied bias voltage should decrease consequently, decreasing the capacitance.

From Equation (1), we can observe that, if the inductance remains constant, then, as the bias voltage increases, the capacitance decreases, thus shifting the self-resonance to a higher frequency. As shown in Figure 3a,b, the self-resonance, as given by Equation (1), shifted to a higher frequency when a bias voltage was applied, and it no longer appeared within our measured frequency range.

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$



(**a**) (**b**)

Figure 3. (**a**) Magnitude of the reflection coefficient (S_{11}) of the BST IDC device under a varied bias voltage (0–50 V), and (**b**) phase of the reflection coefficient of the BST IDC device under a varied bias voltage (0–50 V).

3.2. BST Parameter Extraction

From the one-port S_{11} measurement results shown in Figure 3a,b, we can extract the capacitance C and the series resistance R by using Equations (2)–(5):

$$Z_{11} = Z_0 \frac{1 + S_{11}}{1 - S_{11}} \tag{2}$$

$$Z_{11} = R + j(X_L + X_C) \tag{3}$$

$$X_C = -\frac{1}{2\pi f C} \tag{4}$$

$$C = -\frac{1}{2\pi f X_C} \tag{5}$$

We first converted the measured S_{11} to Z_{11} by using Equation (2). Then, from Equation (3), we observe that the real part and imaginary part of Z_{11} corresponds to the series resistance and the total reactance of the device, respectively. In the frequency range where $X_C \gg X_L$, the total reactance in Equation (3) can be approximated by Equation (4). Equation (5) can then be applied to calculate the capacitance from the imaginary part of Z_{11}.

Figure 4a,b show the real and imaginary parts of the calculated Z_{11} parameters, respectively. Based on Equation (4), as the bias voltage increased, the capacitance decreased, leading to a larger negative reactance, which can be observed in Figure 4b. As also shown in Figure 4a, when the bias voltage increased, the series impedance decreased to the lower frequency region. This can be explained most likely by a greater contribution of the dielectric losses to the equivalent series resistance (ESR) of the BST varactor device at a lower frequency. At higher frequencies, the resistance contribution from the metallization layer dominated. One can also observe from Figure 4a,b that the effect of the noisy response

in Figure 3a at low frequencies for the 40 V and 50 V measurements can be seen prominently in the extracted impedance, but the reactance was only minimally affected.

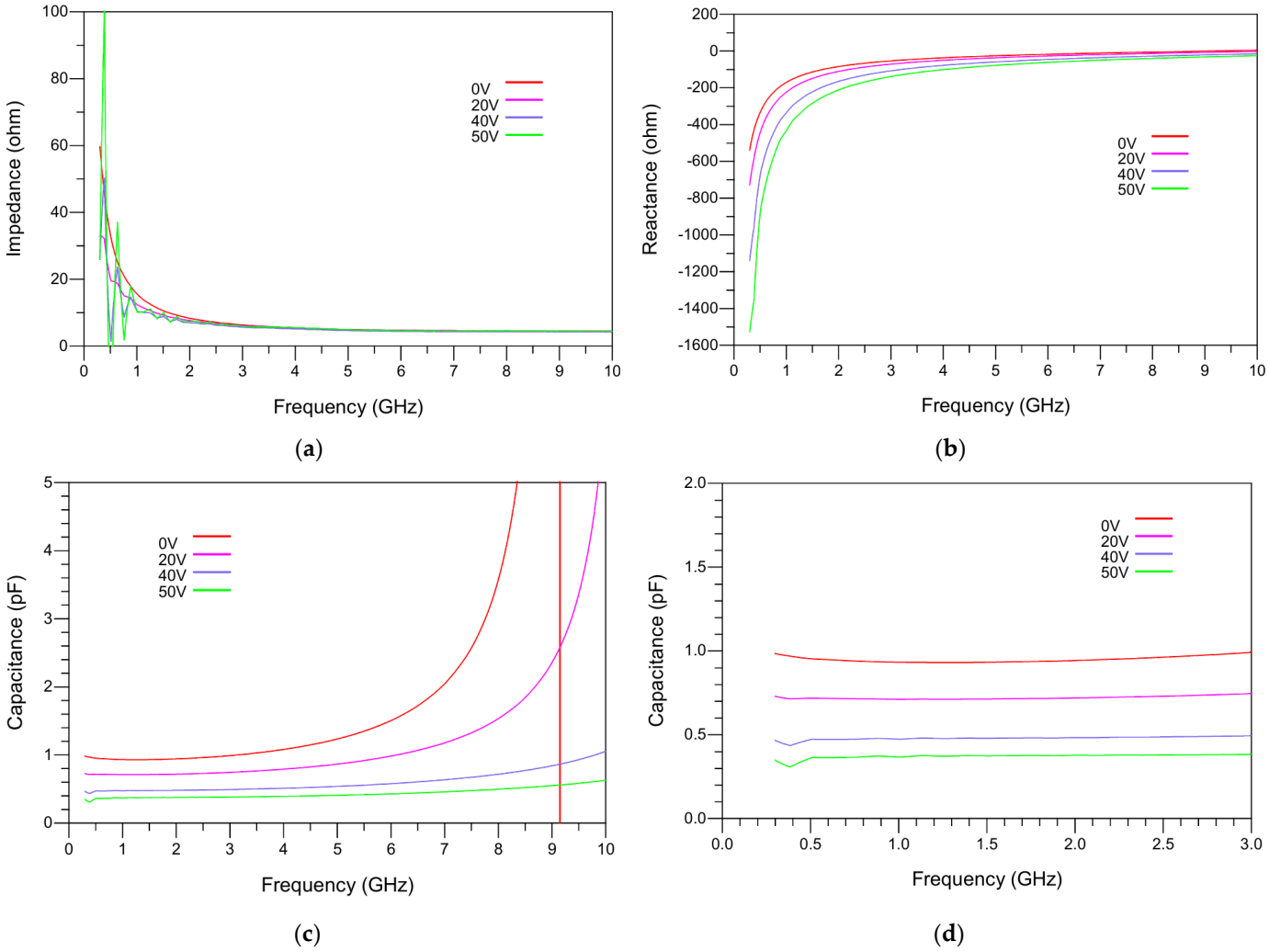


Figure 4. (**a**) Real part of the calculated Z_{11} (impedance) for different bias conditions, (**b**) imaginary part of the calculated Z_{11} (reactance) for different bias conditions, (**c**) calculated capacitance for the IDC device under different bias conditions, and (**d**) zoomed-in region of the calculated capacitance versus the frequency below 3 GHz.

The calculated capacitance shown in Figure 4c highlights the reduction in capacitance as a function of the bias voltage and it is observed that there was more than a 50% decrease between 0 V and 50 V. This decrease in capacitance was due to the decrease in the dielectric constant of BST as a result of applying an external electric field. This occurred because the applied electric field shifted the titanium ion at the center of the BST crystal structure, reducing its ability to store charge, lowering the effective dielectric constant [16]. The electric field tuning behavior observed is similar to what has been previously reported in the literature for BST exhibiting a similar stoichiometry [20,21,33–35]. It is observed in Figure 4d that the calculated capacitances were constant within the low-frequency region.

Based on the calculated capacitance under a certain level of applied bias voltage, Equation (6) can be used to determine the tunability as a function of the bias voltage (x):

$$T(x) = \frac{C_{Vdc=0} - C_{Vdc=x}}{C_{Vdc=0}} 100 \quad (6)$$

Figure 5a,b present the tunability as a function of bias voltage plotted over different frequency ranges. As it is shown, at each bias voltage, the tunability remained quasi-constant within the low-frequency range, after which the tunability level in terms of percentages started to rapidly change due to the effects of the resonance. At 1 GHz, with a bias voltage of 50 V, which is equivalent to an electric field of 25 kV/mm, a maximum tunability of about 60% was observed, and, even at a relatively low electric field of 7.5 kV/mm, a tunability of about 18% was demonstrated.

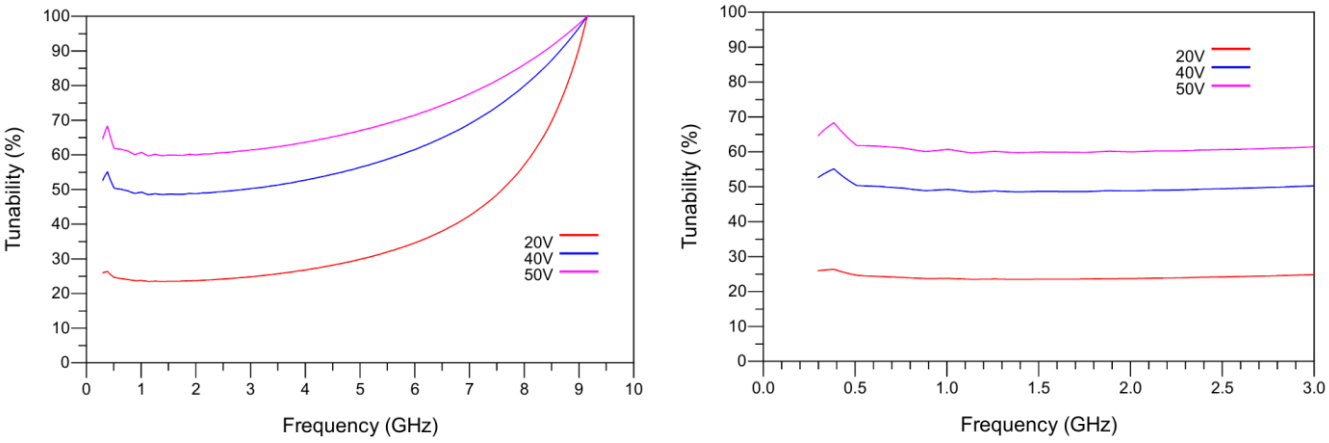


Figure 5. (**a**) Tunability vs. frequency of a measured IDC device at various bias voltages, and (**b**) zoomed-in tunability vs. frequency for a reduced frequency range up to 3 GHz, over which the tunability exhibits quasi-constant values.

The calculated capacitance and Equations (7) and (8) found in [37] can be used to derive the dielectric constant of the IDC device:

$$C = (\varepsilon_r + 1)L[(N-3)A_1 + A_2] \tag{7}$$

$$\varepsilon_r = \frac{C}{L\left[(N-3)A_1 + A_2\right]} - 1 \tag{8}$$

where L is the interdigit finger length in µm, N is the number of fingers, A_1 is the capacitance per unit length of the interior fingers, and A_2 is the capacitance per unit length of the two exterior fingers. A_1 and A_2 are functions of the substrate thickness to finger width ratio; however, for our case with no ground plane, their values became 4.409×10^{-6} pF/um for A_1 and 9.92×10^{-6} pF/um for A_2. Equation (7) shows that the capacitance is linearly dependent on the dielectric constant for an IDC device. Therefore, we can expect the plot of the derived dielectric constant to show the same trend as that exhibited by the capacitance, as it can be seen in Figure 6a,b. At 1 GHz, a maximum dielectric constant of 57 with no bias voltage and a minimum of 22 under a 50 V bias were observed.

Lastly, Equation (9) was used to calculate the quality factor Q of the measured IDC, and its inverse can be used to determine the loss tangent.

$$Q = \frac{X_C}{R} \tag{9}$$

In Figure 7, a trend whereby the Q factor increased as the bias voltage increased can be observed. This behavior was expected, as, from Equation (9), it can be seen that X_C becomes larger as the capacitance decreases due to the applied electric field.

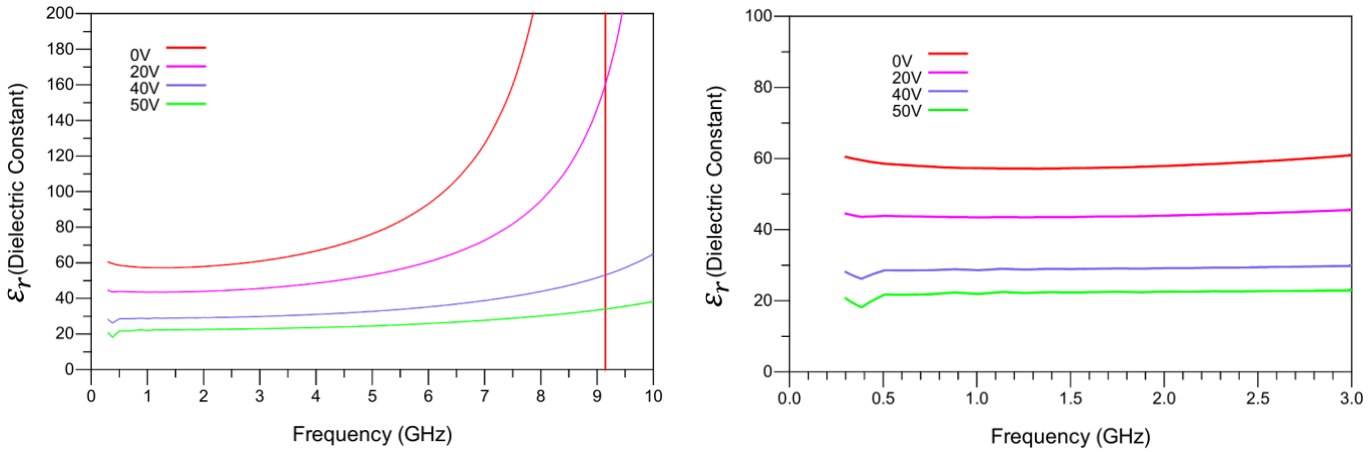


Figure 6. (**a**) Graph of the derived dielectric constant, and (**b**) zoomed-in dielectric constant graph.

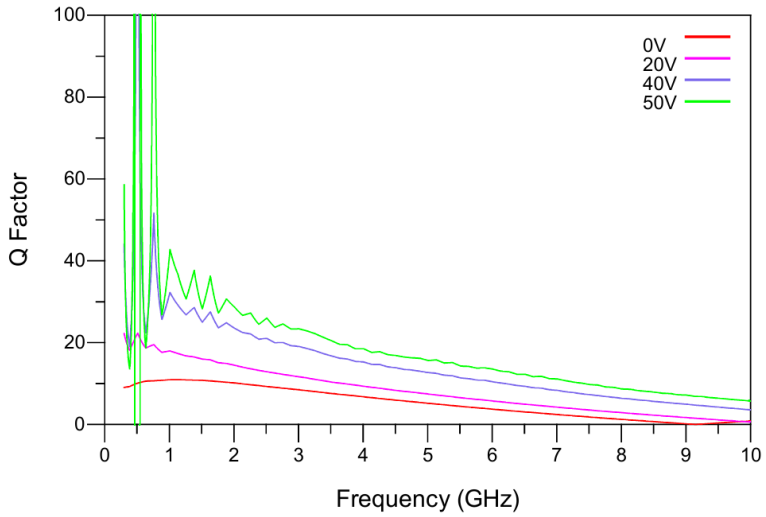


Figure 7. Calculated Q Factor of the IDC device as a function of frequency under various bias voltages.

The loss tangent, as seen in Figure 8a,b, was found to decrease as the applied bias voltage increased, which is consistent with the behavior presented by Muzzupapa et al. [33]. The loss tangent remained below 0.15 throughout the frequency range up to 3 GHz under a 0 V bias and below 0.05 under a 50 V bias, as observed in Figure 8b. We expected this to be the case because of the inverse relationship between the loss tangent ($1/Q$) and Q. A summary of all key characterization parameters of the BST IDC device at 1 GHz can be found in Table 2, and a comparison with other works can be found in Table 3.

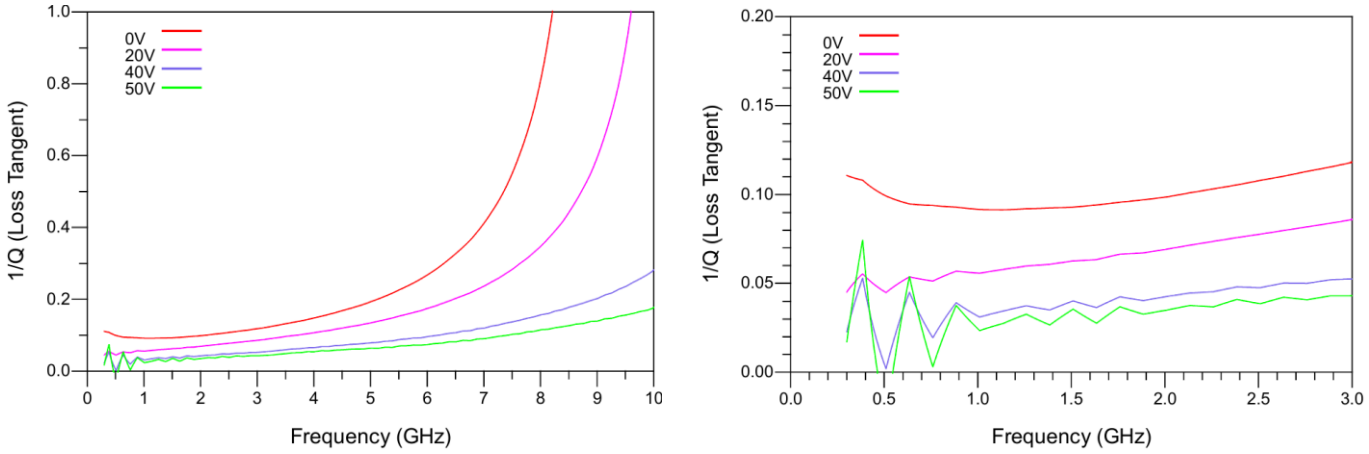


Figure 8. (**a**) Calculated loss tangent vs. frequency at a varied bias voltage (0–50 V), and (**b**) zoomed-in loss tangent vs. frequency at a reduced frequency range up to 3 GHz under a varied bias voltage (0–50 V).

Table 2. Key characterization parameters extracted from BST IDC measurements at 1 GHz.

Voltage (V)	*E* Field (kV/mm)	Capacitance (pF)	Tunability (%)	Dielectric Constant	*Q* Factor	Loss Tangent (1/Q)	Resonance Frequency (GHz)
0	0	0.932	0.0	57.3	10.9	0.092	9.2
20	10	0.711	23.7	43.5	17.9	0.056	10.5
40	20	0.474	49.2	28.6	31.3	0.032	13.1
50	25	0.367	60.6	22.0	41.7	0.024	14.9

Table 3. Comparison of the performances of BST capacitive devices.

Ref.	Deposition Method	Thermal Processing	Tunability (%)	*E* Field (kV/mm)	C_{0V} (pF)
[18]	PLD *	Furnace	15	4.38	1.00
[32]	Aerosol jet	Sinterless	15	10.00	Not reported
[33]	Sol–gel	RTA	40	16.70	0.15
This work	Spray pyrolysis	Photonic sintering	60	25.00	0.93

* Plasma laser deposition.

3.3. SEM Imaging and XRD Measurements

The SEM images shown in Figure 9a–d were taken from the BST film on the measured IDC device. Figure 9a shows the entire IDC device, depicting the BST film completely covering the IDC finger region as well as the slight misalignment offset during deposition as a result of the Kapton masking tape placement. As shown in Figure 9b–d, the as-deposited BST nanoparticles agglomerated into clusters, which were then sintered via photonic thermal processing. While the individual nanoparticles were originally 50 nm, the average size of the sintered crystals was observed to be roughly 500 nm.

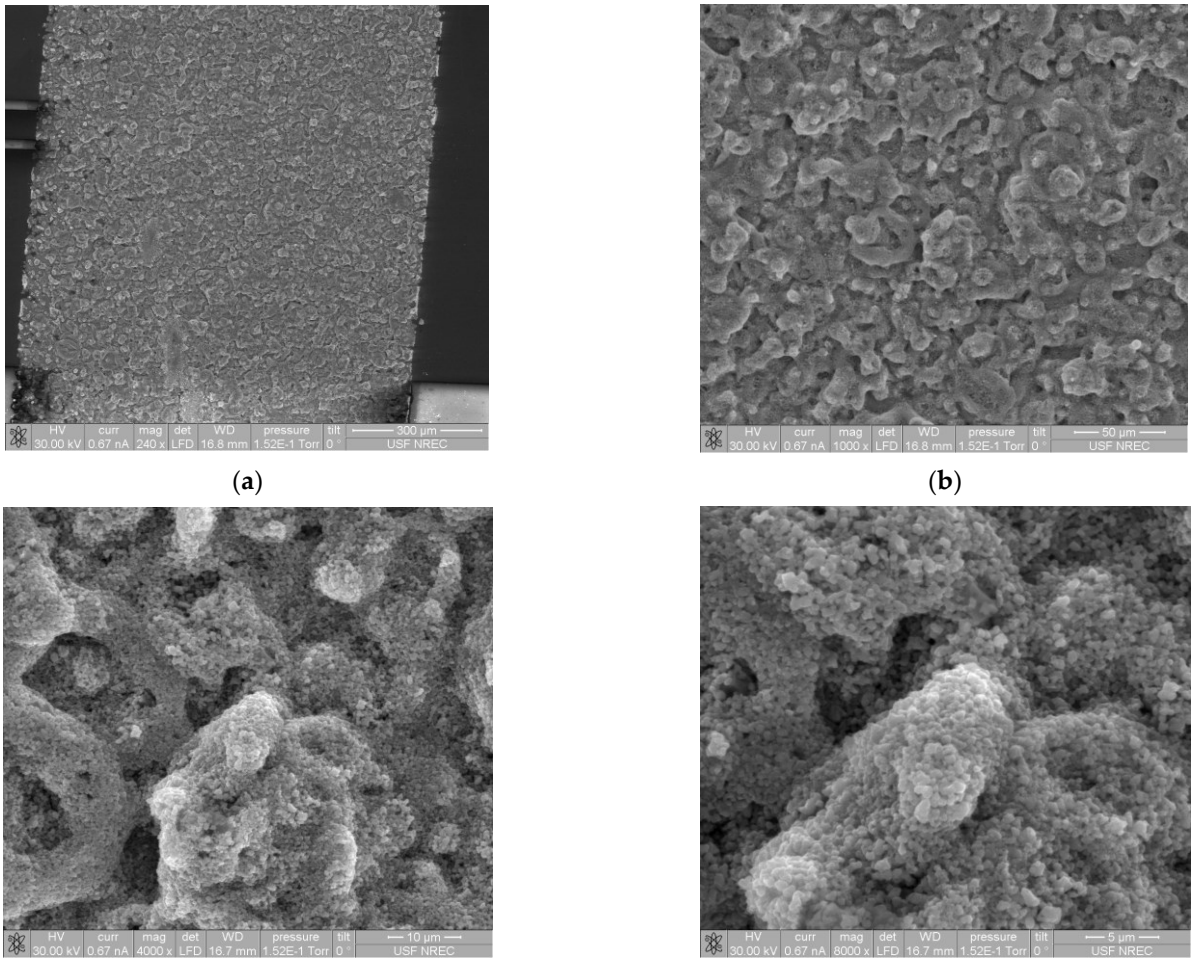


Figure 9. SEM images of the BST film deposited on the IDC device at different magnifications: (**a**) 240× magnification, (**b**) 1000× magnification, (**c**) 4000× magnification, and (**d**) 8000× magnification.

The results of the two-theta scan of the thermally processed film, as seen in Figure 10a, show that all the $Ba_{0.5}Sr_{0.5}TiO_3$ crystal orientations were present with a clear preference for the (110) orientation. All peaks corresponding to the BST and to the Si wafer were analyzed with X'pert HighScore and labeled accordingly, with the small unlabeled peaks belonging to the Kβ radiation. The comparison of the (110) peak between the as-deposited film and the film after the thermal processing in Figure 10b shows that the peak slightly shifted to a lower angle and its intensity increased after thermal processing, suggesting an induced change in the lattice parameter. The XRD peak of the as-deposited film slightly shifted to the right from the BST (110) peak, a phenomenon which suggests residual compressive stress [38]. This residual stress was released as the peak for the thermally annealed sample returned to the anticipated peak position after the photonic thermal processing. From this, it can be inferred that stress relaxation occurred.

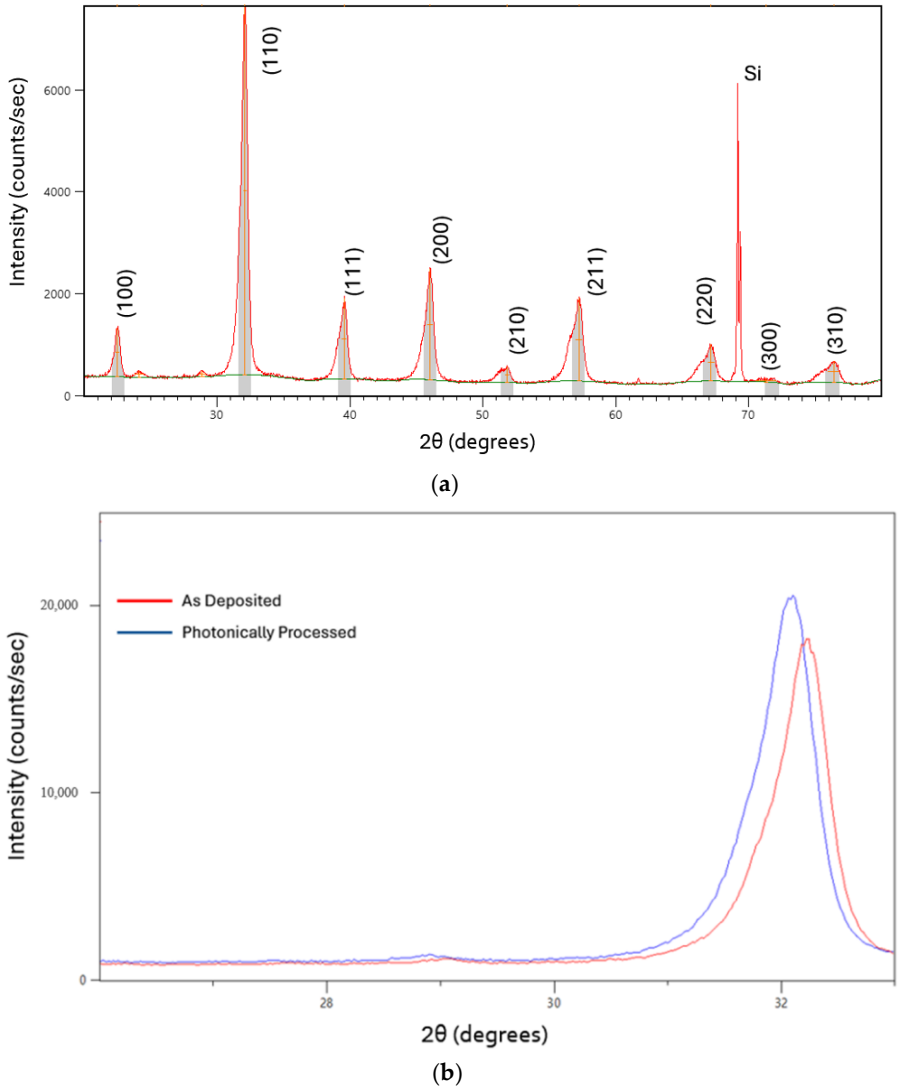


Figure 10. (**a**) Full span two-theta XRD scan of the BST film after the photonic thermal processing (unlabeled peaks correspond to Kβ), and (**b**) a comparison of XRD responses of as-deposited and thermally processed BST films.

4. Discussion

In this work, we fabricate and characterize reconfigurable BST IDC devices using a mix of conventional microfabrication and AM techniques. We sintered the deposited films at low temperatures by using photonic thermal processing, thus allowing for the direct heating of the top surface while minimizing the effect on the metallization layer and substrate. No delamination was observed after processing and film metrology verification using XRD and SEM, demonstrating that thermal processing caused sintering of the deposited nanoparticles and reduced the residual compressive stress in as-deposited samples. Device characterization using S-parameter measurements showed a good performance, with a maximum measured tunability of 60.6% at an applied electric field of 25 kV/mm and an acceptable loss tangent on par with those reported in prior works. The results presented here show promising initial results for the hybrid implementation of photonic thermal processing and AM with conventional fabrication to produce high-frequency reconfigurable ferroelectric varactors, which can potentially be integrated into tightly packaged and on-chip configurations where the thermal budget may limit the compatibility of in-situ thermal processing.

Future work includes the optimization of BST film deposition and thermal processing, and implementation and integration of BST reconfigurable devices into functional

RF circuit modules. The current deposition and photonic thermal sintering processes are still being improved and refined. Further optimization of the photonic pulses will be investigated to balance film quality improvement and heat generated on the substrate to increase compatibility with low thermal budget substrates such as thermoplastics used in AM. For the deposition, a compressed nitrogen with a regulator will be employed in place of the commercial air compressor currently used, as the latter cannot maintain a constant 35 psi pressure throughout the entire spray process. This should help improve the uniformity of each deposited layer, thus allowing for fewer layers to be deposited to achieve complete coverage and reduce layer roughness.

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References

1. Mitchell, A.; Lafont, U.; Hołyńska, M.; Semprimoschnig, C. Additive Manufacturing—A Review of 4D Printing and Future Applications. *Addit. Manuf.* **2018**, *24*, 606–626. [CrossRef]
2. Molitch-Hou, M. 1—Overview of Additive Manufacturing Process. In *Additive Manufacturing: Materials, Processes, Quantifications and Applications*; Zhang, J., Jung, Y.-G., Eds.; Butterworth-Heinemann: Oxford, UK, 2018; pp. 1–38. [CrossRef]
3. Zhang, Y.; Jarosinski, W.; Jung, Y.-G.; Zhang, J. 2—Additive Manufacturing Processes and Equipment. In *Additive Manufacturing: Materials, Processes, Quantifications and Applications*; Zhang, J., Jung, Y.-G., Eds.; Butterworth-Heinemann: Oxford, UK, 2018; pp. 39–51. [CrossRef]
4. Zenou, M.; Grainger, L. 3—Additive Manufacturing of Metallic Materials. In *Additive Manufacturing: Materials, Processes, Quantifications and Applications*; Zhang, J., Jung, Y.-G., Eds.; Butterworth-Heinemann: Oxford, UK, 2018; pp. 53–103. [CrossRef]
5. Moritz, T.; Maleksaeedi, S. 4—Additive Manufacturing of Ceramic Components. In *Additive Manufacturing: Materials, Processes, Quantifications and Applications*; Zhang, J., Jung, Y.-G., Eds.; Butterworth-Heinemann: Oxford, UK, 2018; pp. 105–161. [CrossRef]
6. Craton, M.T.; Albrecht, J.D.; Chahal, P.; Papapolymerou, J. Additive Manufacturing of a Wideband Capable W-Band Packaging Strategy. *IEEE Microw. Wirel. Compon. Lett.* **2021**, *31*, 697–700. [CrossRef]
7. Akbari, S.; Kostov, K.; Brinkfeldt, K.; Adolfsson, E.; Lim, J.-K.; Andersson, D.; Bakowski, M.; Wang, Q.; Salter, M. Ceramic Additive Manufacturing Potential for Power Electronics Packaging. *IEEE Trans. Compon. Packag. Manuf. Technol.* **2022**, *12*, 1857–1866. [CrossRef]
8. Solodov, A.N.; Shayimova, J.; Balkaev, D.; Nizamutdinov, A.S.; Zimin, K.; Kiiamov, A.G.; Amirov, R.R.; Dimiev, A.M. High-throughput, low-cost and "green" production method for high stable polypropylene/perovskite composites, applicable in 3D printing. *Addit. Manuf.* **2022**, *59*, 103094. [CrossRef]
9. Winczewski, J.P.; Arriaga Dávila, J.; Herrera-Zaldívar, M.; Ruiz-Zepeda, F.; Córdova-Castro, R.M.; Pérez de la Vega, C.R.; Cabriel, C.; Izeddin, I.; Gardeniers, H.; Susarrey-Arce, A. 3D-Architected Alkaline-Earth Perovskites. *Adv. Mater.* **2024**, *36*, 2307077. [CrossRef] [PubMed]
10. Chen, M.; Zhou, Z.; Hu, S.; Huang, N.; Lee, H.; Liu, Y.; Yang, J.; Huan, X.; Xu, Z.; Cao, S.; et al. 3D Printing of Arbitrary Perovskite Nanowire Heterostructures. *Adv. Funct. Mater.* **2023**, *33*, 2212146. [CrossRef]
11. Mendoza Sandoval, J.J. Mm-Wave Reconfigurable Antenna Arrays, Phase Shifters and Beamforming Networks with Reduced Hardware Complexity Using Integrated Microfluidic Actuation. Ph.D. Thesis, University of South Florida, Tampa, FL, USA, 2022. Available online: https://digitalcommons.usf.edu/etd/10328 (accessed on 28 October 2024).

12. Gheethan, A. Novel Pattern Reconfigurable Antenna Arrays Using Engineered Metamaterials and Microfluidic Principles. Ph.D. Thesis, University of South Florida, Tampa, FL, USA, 2014. Available online: https://digitalcommons.usf.edu/etd/5223 (accessed on 28 October 2024).
13. Liu, M.; Howe, B.M.; Grazulis, L.; Mahalingam, K.; Nan, T.; Sun, N.X.; Brown, G.J. Voltage-Impulse-Induced Non-Volatile Ferroelastic Switching of Ferromagnetic Resonance for Reconfigurable Magnetoelectric Microwave Devices. *Adv. Mater.* **2013**, *25*, 4886–4892. [CrossRef]
14. Gao, F.; Zhang, K.; Guo, Y.; Xu, J.; Szafran, M. (Ba,Sr)TiO_3/polymer dielectric composites–progress and perspective. *Prog. Mater. Sci.* **2021**, *121*, 100813. [CrossRef]
15. Nam, S.; Psychogiou, D.; Mortazawi, A. Reconfigurable Transfer Function BST Acoustic Wave Lumped Element Resonator Filters. In Proceedings of the 2021 51st European Microwave Conference (EuMC), London, UK, 4–6 April 2022; pp. 301–304. [CrossRef]
16. Price, T.S. Nonlinear Properties of Nanoscale Barium Strontium Titanate Microwave Varactors. Ph.D. Thesis, University of South Florida, Tampa, FL, USA, 2012. Available online: https://scholarcommons.usf.edu/etd/4390 (accessed on 20 February 2020).
17. Ouagague, B.; El-Shaarawy, H.B.; Pacchini, S.; Payan, S.; Rousseau, A.; Maglione, M.; Plana, R. BST tunability study at DC and microwave frequencies by using IDC and MIM capacitors. In Proceedings of the 2010 Asia-Pacific Microwave Conference, Yokohama, Japan, 7–10 December 2010; pp. 1837–1840.
18. Ouaddari, M.; Delprat, S.; Vidal, F.; Chaker, M.; Wu, K. Microwave characterization of ferroelectric thin-film materials. *IEEE Trans. Microw. Theory Tech.* **2005**, *53*, 1390–1397. [CrossRef]
19. Gautam, C.R.; Yadav, A.K. Synthesis and Optical Investigations on (Ba,Sr)TiO_3 Borosilicate Glasses Doped with La_2O_3. *Opt. Photonics J.* **2013**, *3*, 35643. [CrossRef]
20. Dey, S.K.; Kooriyattil, S.; Pavunny, S.P.; Katiyar, R.S.; Subramanyam, G. Analyses of Substrate-Dependent Broadband Microwave (1–40 GHz) Dielectric Properties of Pulsed Laser Deposited $Ba_{0.5}Sr_{0.5}TiO_3$ Films. *Crystals* **2021**, *11*, 852. [CrossRef]
21. Wang, Y.; Chen, X. Investigation of the Positive Temperature Coefficient Resistivity of Nb-Doped $Ba_{0.55}Sr_{0.45}TiO_3$ Ceramics. *Crystals* **2024**, *14*, 419. [CrossRef]
22. Guo, Z.; Pan, L.; Bi, C.; Qiu, H.; Zhao, X.; Yang, L.; Rafique, M.Y. Structural and multiferroic properties of Fe-doped $Ba_{0.5}Sr_{0.5}TiO_3$ solids. *J. Magn. Magn. Mater.* **2013**, *35*, 24–28. [CrossRef]
23. Bhoyar, D.N.; Somvanshi, S.B.; Nalle, P.B.; Mande, V.K.; Pandit, A.A.; Jadhav, K.M. Multiferroic Fe^{3+} ion doped $BaTiO_3$ Perovskite Nanoceramics: Structural, Optical, Electrical and Dielectric Investigations. *J. Phys. Conf. Ser.* **2020**, *1644*, 012058. [CrossRef]
24. Safronov, A.P.; Mikhnevich, E.A.; Lotfollahi, Z.; Blyakhman, F.A.; Sklyar, T.F.; Larrañaga Varga, A.; Medvedev, A.I.; Fernández Armas, S.; Kurlyandskaya, G.V. Polyacrylamide Ferrogels with Magnetite or Strontium Hexaferrite: Next Step in the Development of Soft Biomimetic Matter for Biosensor Applications. *Sensors* **2018**, *18*, 257. [CrossRef]
25. Yang, Z.; Wang, H.; Dong, X.; Yan, H.; Lei, C.; Luo, Y. Giant magnetoimpedance based immunoassay for cardiac biomarker myoglobin. *Anal. Methods* **2017**, *9*, 3636–3642. [CrossRef]
26. Zhao, M.; Cao, W.Q. The effects of deposition temperature on structure and dielectric properties of $Ba_{0.6}Sr_{0.4}TiO_3$ thin films produced by pulsed laser deposition. *Ceram. Int.* **2009**, *35*, 2283–2287. [CrossRef]
27. Silva, J.P.B.; Kamakshi, K.; Sekhar, K.C.; Moreira, J.A.; Almeida, A.; Pereira, M.; Gomes, M.J.M. Light-controlled resistive switching in laser-assisted annealed $Ba_{0.8}Sr_{0.2}TiO_3$ thin films. *Phys. Status Solidi A* **2016**, *213*, 1082–1087. [CrossRef]
28. Kang, M.G.; Cho, K.H.; Oh, S.M.; Do, Y.H.; Kang, C.Y.; Kim, S.; Yoon, S.J. Low-temperature crystallization and electrical properties of BST thin films using excimer laser annealing. *Curr. Appl. Phys.* **2011**, *11*, S66–S69. [CrossRef]
29. Podpirka, A.; Cole, M.W.; Ramanathan, S. Effect of photon irradiation on structural, dielectric, and insulating properties of $Ba_{0.60}Sr_{0.40}TiO_3$ thin films. *Appl. Phys. Lett.* **2008**, *92*, 212906. [CrossRef]
30. Nikfalazar, M.; Sazegar, M.; Friederich, A.; Kohler, C.; Zheng, Y.; Wiens, A.; Binder, J.R.; Jakoby, R. Inkjet printed BST thick-films for x-band phase shifter and phased array applications. In Proceedings of the 2013 International Workshop on Antenna Technology (iWAT), Karlsruhe, Germany, 4–6 March 2013; pp. 121–124. [CrossRef]
31. Nikfalazar, M.; Zheng, Y.; Wiens, A.; Jakoby, R.; Friederich, A.; Kohler, C.; Binder, J.R. Fully inkjet-printed tunable S-band phase shifter on BST thick film. In Proceedings of the 2014 44th European Microwave Conference, Rome, Italy, 6–9 October 2014; pp. 504–507. [CrossRef]
32. Ranasingha, O.K.; Haghzadeh, M.; Sobkowicz, M.J.; Kingsley, E.; Armiento, C.; Akyurtlu, A. Formulation and Characterization of Sinterless Barium Strontium Titanate (BST) Dielectric Nanoparticle Ink for Printed RF and Microwave Applications. *J. Electron. Mater.* **2021**, *50*, 3241–3248. [CrossRef]
33. Crunteanu, A.; Muzzupapa, V.; Ghalem, A.; Huitema, L.; Passerieux, D.; Borderon, C.; Renoud, R.; Gundel, H.W. Characterization and Performance Analysis of BST-Based Ferroelectric Varactors in the Millimeter-Wave Domain. *Crystals* **2021**, *11*, 277. [CrossRef]
34. Lee, Y.-C.; Lin, Y.-C.; Chen, W.-C.; Fu, J.-S. Fabrication and characterization of ferroelectric varactors for tunable wireless front-ends. In Proceedings of the 2010 Asia-Pacific Microwave Conference, Yokohama, Japan, 7–10 December 2010; pp. 1220–1223.
35. Borderon, C.; Ginestar, S.; Gundel, H.W.; Haskou, A.; Nadaud, K.; Renoud, R.; Sharaiha, A. Design and Development of a Tunable Ferroelectric Microwave Surface Mounted Device. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control.* **2020**, *67*, 1733–1737. [CrossRef] [PubMed]
36. Ghalem, A.; Huitema, L.; Crunteanu, A.; Rammal, M.; Trupina, L.; Nedelcu, L.; Banciu, M.G.; Dutheil, P.; Constantinescu, C.; Marchet, P.; et al. Electrical transport properties and modelling of electrostrictive resonance phenomena in $Ba_{2/3}Sr_{1/3}TiO_3$ thin films. *J. Appl. Phys.* **2016**, *120*, 184101. [CrossRef]

37. Bahl, I.J. *Lumped Elements for RF and Microwave Circuits*, 2nd ed.; Artech House: Boston, MA, USA, 2023; pp. 185–200.
38. Zhou, P.; Jin, X.; Chen, J.; Zhou, Y.; Luo, J.; Li, H.; Chu, C.; Yan, M. Residual stress estimation in laminated ZrB_2-SiC ultra-high temperature ceramics with strong interfaces using X-ray diffraction and indentation technique. *Ceram. Int.* **2017**, *43*, 12459–12465. [CrossRef]