Journal of Vacuum Science and Technology B

RESEARCH ARTICLE | OCTOBER 28 2024

# Scalable fabrication of vertically arranged $Bi_2Se_3$ crossbar arrays for memristive device applications

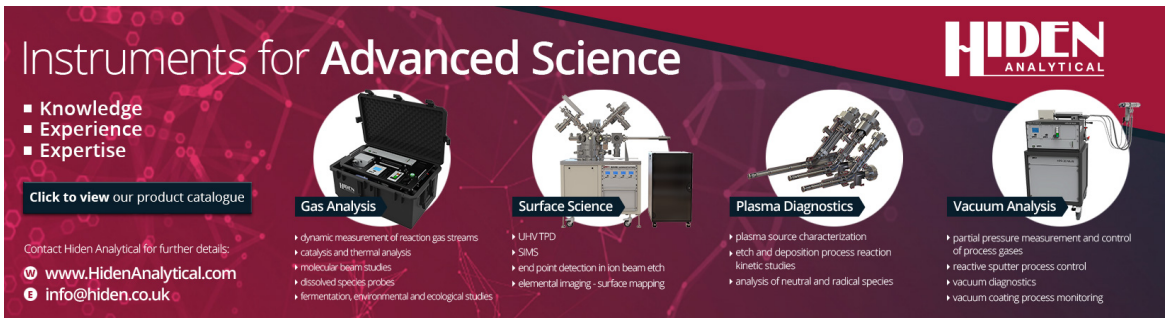
**Special Collection:** Papers from the 67th International Conference on Electron, Ion and Photon Beam Technology and Nanofabrication (EIPBN 2024)

Seung jun Ki ; Shiwoo Lee ; Mingze Chen ; Xiaogan Liang



*J. Vac. Sci. Technol. B* 42, 063203 (2024)
https://doi.org/10.1116/6.0004022
CHORUS





JVST B
Journal of Vacuum Science & Technology B

ARTICLE

pubs.aip.org/avs/jvb

# Scalable fabrication of vertically arranged $Bi_2Se_3$ crossbar arrays for memristive device applications

Cite as: J. Vac. Sci. Technol. B **42**, 063203 (2024); doi: 10.1116/6.0004022
Submitted: 29 August 2024 · Accepted: 9 October 2024 ·
Published Online: 28 October 2024



Seung jun Ki, Shiwoo Lee, Mingze Chen, and Xiaogan Liang[a)]

## AFFILIATIONS

Department of Mechanical Engineering, University of Michigan, Ann Arbor 48109, Michigan

**Note:** This paper is part of the Special Topic Collection: Papers from the 67th International Conference on Electron, Ion and Photon Beam Technology and Nanofabrication (EIPBN 2024).

[a)]**Electronic mail:** xiaoganl@umich.edu

## ABSTRACT

Despite the unique advantages of the memristive switching devices based on two-dimensional (2D) transition metal dichalcogenides, scalable growth technologies of such 2D materials and wafer-level fabrication remain challenging. In this work, we present the gold-assisted large-area physical vapor deposition (PVD) growth of $Bi_2Se_3$ features for the scalable fabrication of 2D-material-based crossbar arrays of memristor devices. This work indicates that gold layers, prepatterned by photolithography processes, can catalyze PVD growth of few-layer $Bi_2Se_3$ with 100-folds larger crystal grain size in comparison with that grown on bare $Si/SiO_2$ substrates. We also present a fluid-guided growth strategy to improve growth selectivity of $Bi_2Se_3$ on Au layers. Through the experimental and computational analyses, we identify two key processing parameters, i.e., the distance between $Bi_2Se_3$ powder and the target substrate and the distance between the leading edges of the substrate and the substrate holder with a hollow interior, which plays a critical role in realizing large-scale growth. By optimizing these growth parameters, we have successfully demonstrated cm-scale highly-selective $Bi_2Se_3$ growth on crossbar-arrayed structures with an in-lab yield of 86%. The whole process is etch- and plasma-free, substantially minimizing the damage to the crystal structure and also preventing the formation of rough 2D-material surfaces. Furthermore, we also preliminarily demonstrated memristive devices, which exhibit reproducible resistance switching characteristics (over 50 cycles) and a retention time of up to $10^6$ s. This work provides a useful guideline for the scalable fabrication of vertically arranged crossbar arrays of 2D-material-based memristive devices, which is critical to the implementation of such devices for practical neuromorphic applications.





## I. INTRODUCTION

Two-dimensional (2D) materials have been extensively studied for revolutionizing numerous electronic devices, including thin-film transistors,[1–3] photovoltaic[4,5] and optoelectronic devices,[6–8] and spintronics.[9,10] Recently, memristive switching devices based on 2D-layered transition metal dichalcogenides (TMDCs) such as $MoS_2$ have been reported.[11–14] These 2D-materials-based memristive devices exhibit unique characteristics such as low power consumption, effective tunability through electrostatic gates, and fast-switching rate attributed to their atomically thin structures.[15,16] In addition to TMDC-based materials such as $MoS_2$, other layered materials such as $Bi_2Se_3$ have also been investigated for making new resistive switching devices.[17–19] For example, Chen *et al.* recently reported laterally arranged $Bi_2Se_3$ memristors for neuromorphic processing of the temporal information carried by analog sensory signals.[20] Yin *et al.* also reported a resistance switching behavior of 2D topological $Bi_2Se_3$ nanosheets, fabricated by the damageless oxygen plasma injection method.[19] These 2D-material-based memristive devices have exhibited several important advantages in comparison with oxide-based memristors, including the lower threshold field for initiating state changes, significantly improved level of interconnectivity among multiple devices, and higher biological similarity for emulating real neuron functions.

Despite the explosive growth of the studies on 2D-layered material-based memristors, the scalable synthesis of uniform 2D materials over large areas for making arrays of vertically arranged memristors is an unresolved challenge. On the contrary, the memristor families based on transition metal oxides (TMOs) such as TiOx, TaOx, WOx, and HfOx have been extensively studied and some researchers have reported the memristors fabricated and

integrated into commercially viable circuit-level architectures.[21–25] In conventional oxide-based memristor fabrication processes, oxide-based insulating layers are deposited over the entire exterior surface of the substrate with prepatterned bottom electrodes using sputtering or thermal oxidation techniques, which are suitable for wafer-scale growths.[26,27] To realize such scalable wafer-scale fabrication of layered materials, vapor-based growth methods have been reported to successfully synthesize various 2D materials.[28–30] However, most 2D-material growth techniques generate isolated few-layer crystal grains or cluster islands across the cm-scale substrate surface, resulting in shorted nodes in the crossbar arrays over cm-scale areas. Additionally, the sample quality resulted from these growth methods is extremely sensitive to a series of processing parameters such as powder/vapor types, gas flow rates, types of substrate materials, substrate positions, growth temperatures, and processing time, resulting in significant variations in the qualities of 2D materials among the samples from different growth batches. Thus, additional research are needed to explore new 2D-material-based fabrication schemes and especially realize scalable fabrication of the vertically stacked device structures. A few works have been reported toward addressing this challenge. For example, Ahn *et al.* reported an atomic layer deposition (ALD) method to enable area-selective deposition of $MoS_2$, and Huang *et al.* demonstrated CVD-based selective growth of $Sb_2Te_3$ features.[31,32] In these works, however, strong chemical solutions are needed to completely eliminate the required seeding features after the growth process, which can damage as-grown layered materials.

In this work, we present a gold-assisted large-area physical vapor deposition (PVD) growth of the $Bi_2Se_3$-based crossbar arrays for the scalable etch-, chemical-, and plasma-free fabrication of 2D-material-based memristors. We also integrate the PVD process with COMSOL-based computational fluidic dynamics (CFD) analysis to investigate the changes in gas flows under various experimental and processing conditions. Such simulation results, along with the experimental results, allow us to examine the correlation between the resultant $Bi_2Se_3$ thickness distribution and the substrate placement configuration, as well as other critical processing parameters, leading to the optimization of the growth conditions essential to achieve a cm-scale 10 s nm thick few-layer $Bi_2Se_3$ features selectively grown on Au surfaces.

## II. EXPERIMENTS

### A. Photolithography for patterning the Au electrodes

A polydimethylglutarimide lift-off resist (PMGI SF 6) is spin-coated on a 500/3 $\mu$m thick $Si/SiO_2$ substrate using a CEE Apogee tool at 2000 rpm. After 190 °C baking for 300 s, the substrate is spin-coated with another 0.97 $\mu$m thick SPR 955 photoresist (PR) using a TEL Mark Vz Coater. The PR-coated substrate is exposed to UV light using a stepper (GCA Autostep). After the developing process, Ti/Au (10/100 nm) metal layers are deposited using an Enerjet Evaporator. The metal-deposited substrate is subsequently immersed into a Remover PG tool for performing the metal lift-off process.

### B. PVD of $Bi_2Se_3$

Au-patterned substrate ($1 \times 2$ cm$^2$ size) is loaded into a quartz tube furnace (25 mm OD × 20.5 mm ID × 600 mm L) for $Bi_2Se_3$ deposition through the PVD process. First, $Bi_2Se_3$ powder ($Bi_2Se_3$, 99.995%, Sigma-Aldrich) is loaded to the inlet area of a crucible boat (AdValue Technology) and the crucible boat is located at the center of the quartz tube. The target substrate is placed on an alumina crucible ($50 \times 12 \times 10$ mm$^3$), which is located downstream toward the open-end of the tube. Afterward, the PVD tube is pumped to a pressure below 160 mTorr, and the carrier gas (99.999% argon from cryogenic gases) continuously flows through the PVD tube with a flow rate of 100 SCCM. The outlet absolute pressure is maintained at 2.2 Torr (~293 Pa). After deposition over a 15 min course at 500 °C, the furnace is opened to let the tube cool down to the ambient temperature of 25 °C.

### C. COMSOL simulation setup

For the purpose of simplification, simulation only focuses on computational fluid dynamics (CFD), temporarily neglecting the thermal effects involved in the growth process. The modeled geometry includes the quartz tube, the alumina crucible holders for loading $Bi_2Se_3$ powder, and the target substrate. For both crucibles, the wall thickness is 2.5 mm. The argon gas flow inside the quartz tube is assumed to be laminar (Reynolds number: <100), with a boundary condition, which neglects the viscous effects in the boundary layer and only focuses on the distribution of free-stream flow velocity on the substrate. The inlet flow rate is set to 100 SCCM and the outlet absolute pressure is maintained at 2.2 Torr (~293 Pa), which are consistent with our experimental parameters. The argon gas temperature is set at 500 °C, with a density of 0.0018 kg/m$^3$, and a dynamic viscosity of $4 \times 10^{-6}$ Pa s, which is derived from ideal gas law and kinetic theory of gases. Here, the argon gas is assumed as an ideal gas due to its relatively high temperature and low pressure. Multiple parametric sweeps are conducted for simulating the growth cases with various positions of the $Bi_2Se_3$ sample and the target substrate holder.

## III. RESULTS AND DISCUSSION

Figure 1(a) schematically illustrates the overall fabrication route involving Au-assisted PVD growth and photolithography for patterning the top/bottom metal electrodes of the crossbar arrays. The detailed fabrication process includes the following specific steps. First, a 500 nm wide Au bottom electrode (BE) is patterned by photolithography followed by metal deposition and lift-off processes. Subsequently, the Au-patterned substrate ($1 \times 2$ cm$^2$) is loaded into the furnace for $Bi_2Se_3$ deposition through the PVD process. The $Bi_2Se_3$ powder ($Bi_2Se_3$, 99.995%, Sigma-Aldrich) is loaded to the inlet region of a crucible boat (AdValue Technology), and the crucible boat is located at the center of the PVD quartz tube. The target substrate with prepatterned Au bottom electrodes is placed at a downstream location in the furnace tube, facing up for the vapor deposition (condensation) process. Figures 1(b) and 1(c) show the top-view scanning electron microscopy (SEM) and energy-dispersive x-ray spectroscopy (EDS) images of a representative $Bi_2Se_3$ feature selectively grown on a prepatterned Au BE, respectively. Both results show a good continuity of as-grown $Bi_2Se_3$ over the whole BE region. The EDS images further indicate that most $Bi_2Se_3$ deposition takes place on the Au surface [Fig. 1(c)]. It is noted that there are still nonspecifically deposited

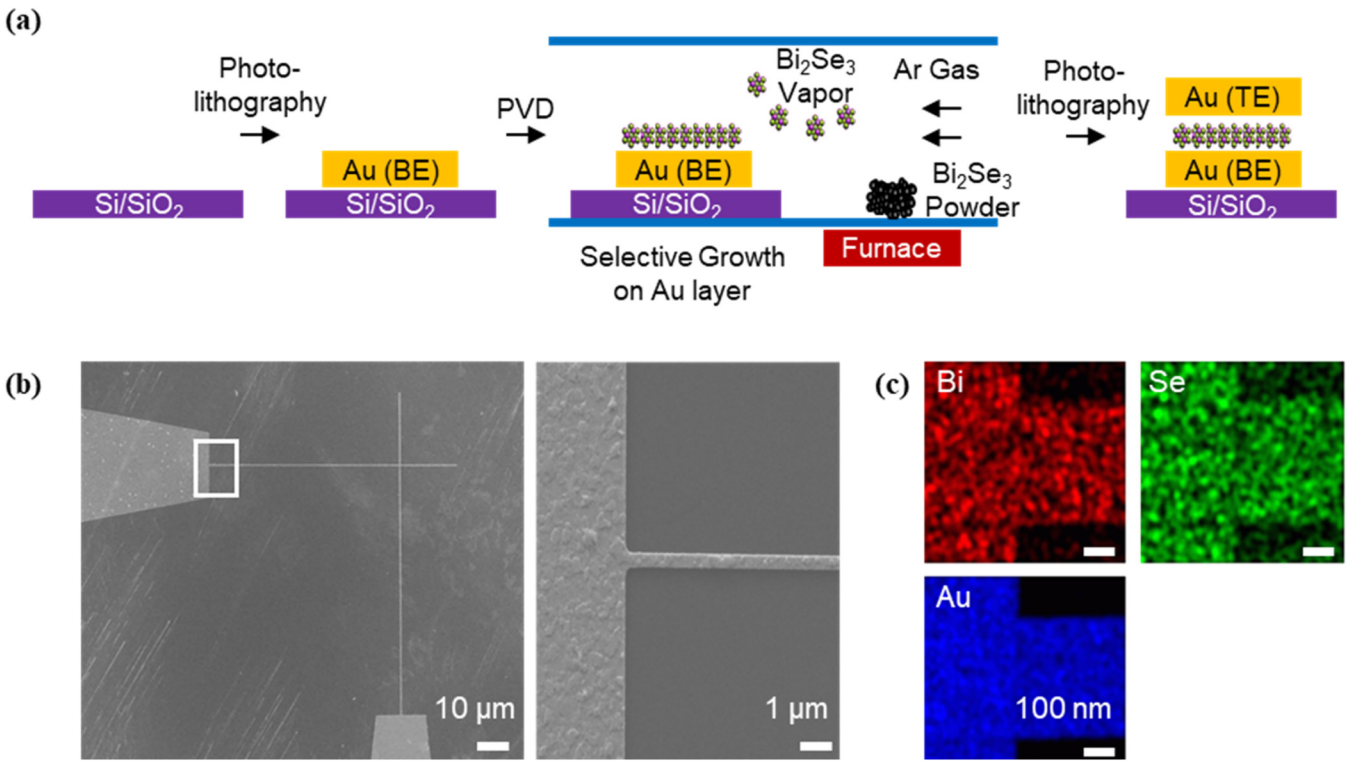



**FIG. 1.** (a) Illustration of the gold-assisted PVD and lithography processes to fabricate vertically arranged $Bi_2Se_3$ memristor devices, and (b) SEM (scale bars: 10 and 1 $\mu$m, respectively) and (c) EDS images of a representative as-grown $Bi_2Se_3$ memristor channel (scale bar: 100 nm).



$Bi_2Se_3$ flakes on bare $Si/SiO_2$ substrate regions. However, such non-specifically deposited flakes are not continuous over large areas.

To further optimize the fabrication process of the crossbar structures with vertically arranged memristors, we further analyze the growth results of $Bi_2Se_3$ films on both Au and $Si/SiO_2$ substrate regions. In this work, suppression of the growth of $Bi_2Se_3$ features on the bare $SiO_2$ substrate regions is preferentially pursued because it allows the etch-free patterning of 2D-material device features (i.e., direct formation of isolated memristor nodes for the crossbar implementation). Figure 2 demonstrates a quantitative comparison of the deposition results on Au and bare $SiO_2$ surfaces. As shown in Fig. 2(a), only sparsely distributed tiny triangular $Bi_2Se_3$ crystal grains are found on the bare $SiO_2$ surface regions near the edge of the Au BE. Contrarily, on the Au electrode surface (electrode width ~4 $\mu$m), the nucleated $Bi_2Se_3$ crystal grains have much bigger sizes and they continuously cover the whole Au electrode surface. Such a distinction of the growth results between Au and $SiO_2$ surfaces strongly implies the catalytic role of Au in the $Bi_2Se_3$ growth. We further quantitatively compare these growth results by measuring the statistical distributions of the $Bi_2Se_3$ grain size data captured from the two different regions, as displayed in Fig. 2(b). The average grain size of the $Bi_2Se_3$ crystals grown on the Au layer is ~450 nm, which is 50-folds larger than the crystal size grown on the bare $SiO_2$ substrate. Such a selective growth result is tentatively attributed to a hypothesized mechanism described in Fig. 2(c). Specifically, vapor-solid-state (VSS) $Bi_2Se_3$ molecules, which are vaporized after being heated up to 500 °C, have quintuple layer (QL) structures and two different types of dangling bonds. One type of the dangling bonds is located along the top and bottom Se atoms in a QL, while the other type of the dangle bonds is located along the side Bi atoms in the QL. Because Se dangling bonds have a stronger affinity to the gold layer than to the $SiO_2$ layer, they can preferentially initiate the nucleation of $Bi_2Se_3$ molecules on the Au surface. Furthermore, the Bi dangling bonds, which are parallel to the surface, can facilitate the formation of large $Bi_2Se_3$ crystal grains.

Nevertheless, over the whole $1 \times 2$ cm$^2$ size substrate surface, the resultant crystal qualities and growth selectivity are still not uniform. For example, as shown by the photograph in Fig. 3(a), the areal density of the as-grown $Bi_2Se_3$ crystal grains near the leading edge (LE) of the substrate is noticeably higher than that in the proximity of the trailing edge (TE) (here, the higher grain density is manifested as the apparently white color regions with the higher saturation in this macroscopic photo). To improve the yield and effective throughput of the growth of $Bi_2Se_3$ device features over large areas, such a nonuniformity issue needs to be addressed. Here, the nonuniformity of as-grown $Bi_2Se_3$ grains is further analyzed by examining the SEM images captured from both LE and TE areas [Fig. 3(b)]. These SEM images clearly indicate that for

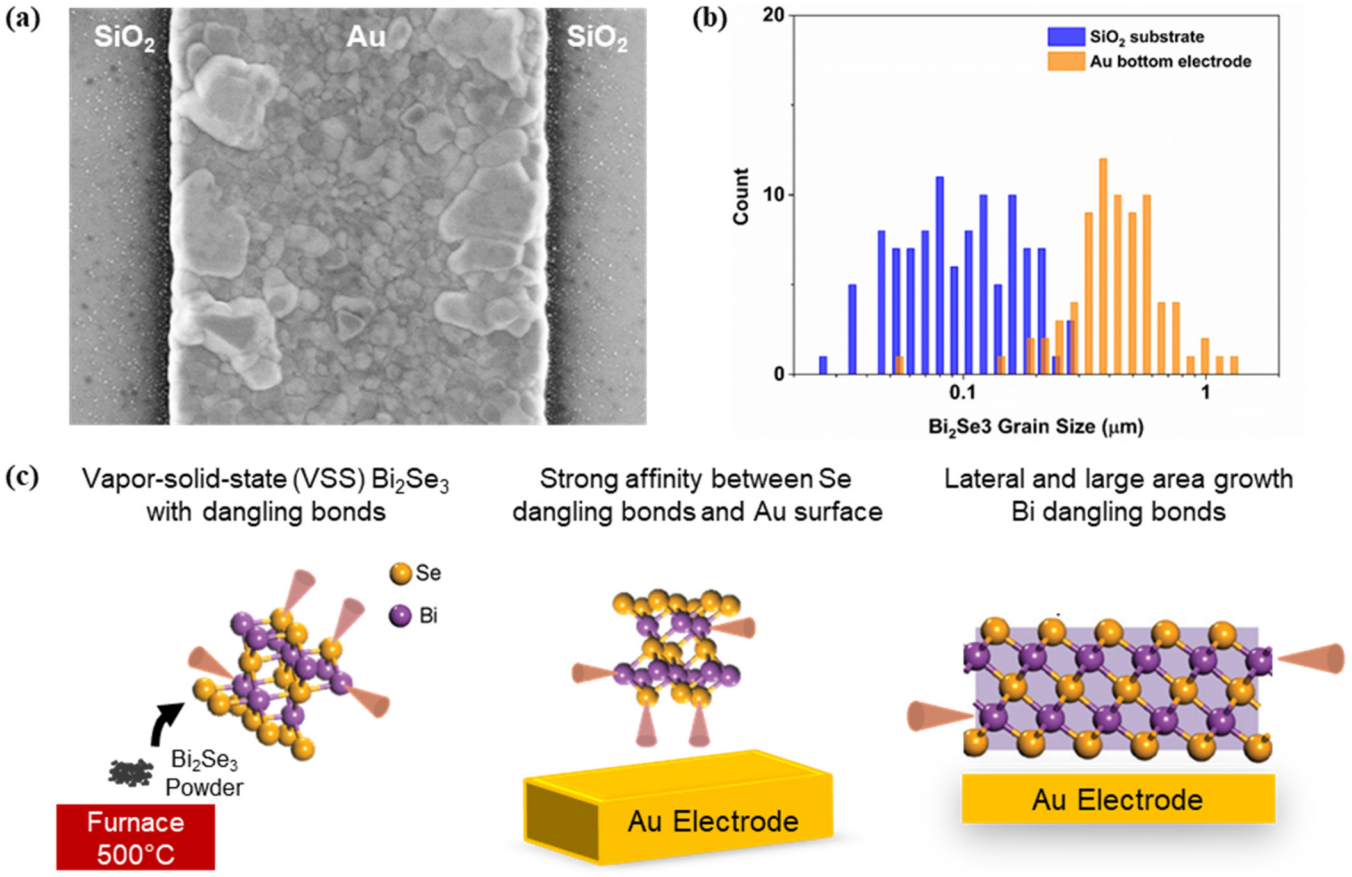



**FIG. 2.** Gold-assisted large-area PVD growth of $Bi_2Se_3$ thin films: (a) SEM image revealing the catalyzed growth of the $Bi_2Se_3$ thin film on a bottom Au electrode. (b) Quantitative comparison of the statistical data of $Bi_2Se_3$ grain size data captured from the bare $SiO_2$ substrate and Au bottom electrode. (c) Hypothesized mechanism of the Au-assisted large-area PVD growth of continuous $Bi_2Se_3$ crystal grains.

both LE and TE areas, the $Bi_2Se_3$ crystal grains nucleated on the Au surfaces exhibit quite similar crystalline morphologies, whereas the $Bi_2Se_3$ grains nucleated on the bare $SiO_2$ surfaces of these two regions exhibit a significant difference in their average grain sizes and areal densities. This also indicates that the $Bi_2Se_3$ nucleation in the proximity of the LE of the substrate exhibits a poor growth selectivity mediated by the presence of Au. Such unwanted $Bi_2Se_3$ features within the bare $SiO_2$ surface can cause significant leakage currents and failure of the crossbar arrays of memristors. We tentatively propose a hypothesized model for explaining this phenomenon. In this model, the carrier gas flow containing VSS $Bi_2Se_3$ molecules can develop vortices in the proximity of the LE of the substrate holder. The vortex flow field, formed near the LE of the substrate holder, can be attributed to the nonuniformity of $Bi_2Se_3$ grains growth by affecting the flow gas pressure and molecular concentration over the substrate. We further speculate the nonuniform growth result over the target substrate by examining two critical processing parameters: (1) the distance between the $Bi_2Se_3$ powder holder and the LE of the substrate holder ($D_1$) and (2) the distance between the LE of the substrate holder and the LE of the substrate ($D_2$), as schematically illustrated in Fig. 3(c).

To understand the nonuniform growth result and its correlation to the PVD processing conditions, COMSOL Multiphysics simulation is performed in accordance with the experimental setup. For simplification, simulation focuses solely on computational fluid dynamics (CFD), temporarily neglecting the thermal effects involved in the growth process. The argon carrier gas flow inside the quartz tube is assumed to be laminar because of the relatively small Reynolds number (~100), only considering the free-stream flow velocity distribution and neglecting the details of the flow in the boundary layer at the solid/fluid interface. As shown in Table I, seven different sets of processing parameters are experimentally tested and compared to the COMSOL simulation results obtained under these settings to identify the key factors responsible for the nonuniformity of $Bi_2Se_3$ growth over large areas.

Figure 4 shows the comparison between simulation and experimental results, obtained using three sets of processing parameters (i.e., Nos. 5, 6, and 7 in Table I). Under these processing

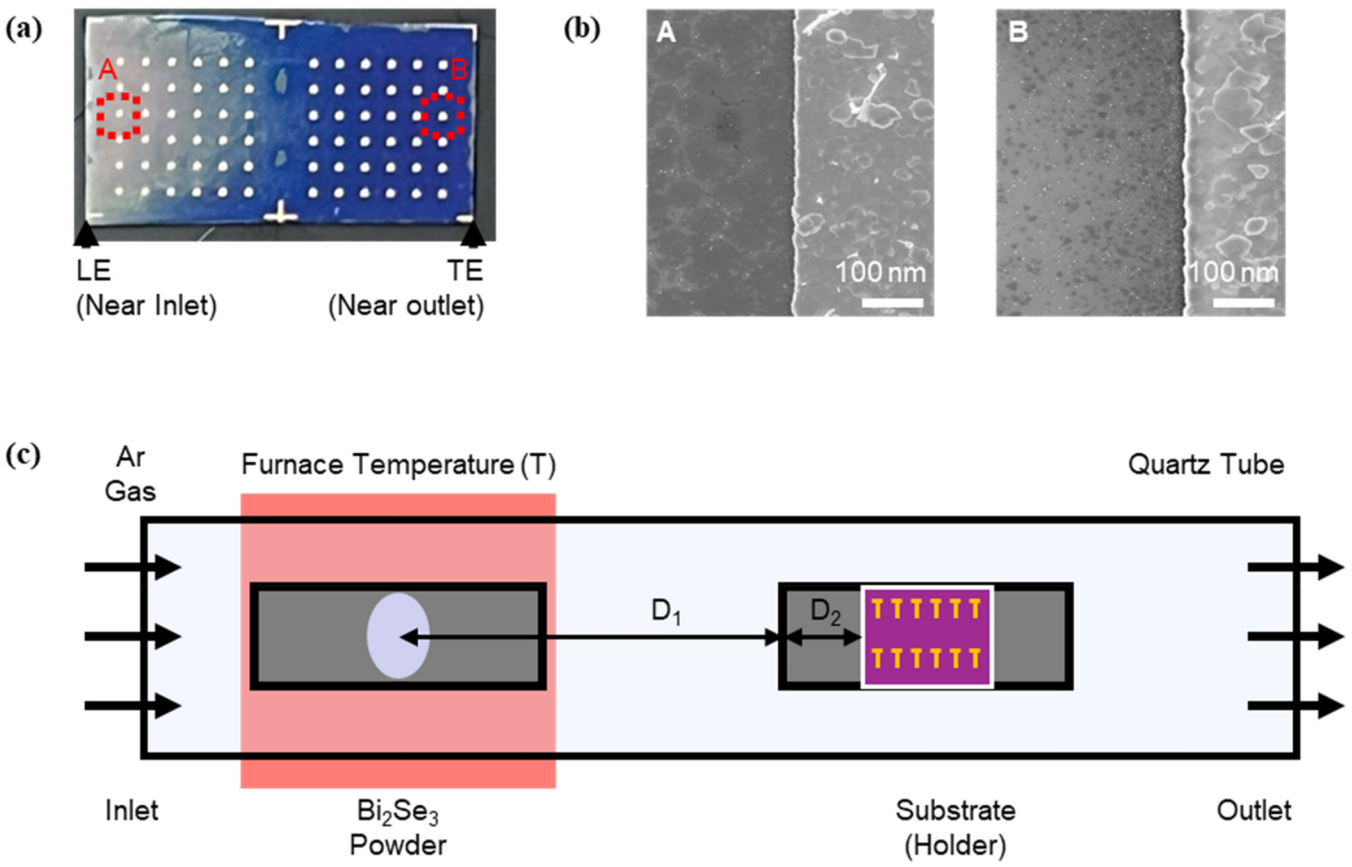



**FIG. 3.** Spatial nonuniformity of $Bi_2Se_3$ growth result over a $SiO_2$/Si substrate: (a) optical image of a 1 cm (height) × 2 cm (width) Si/$SiO_2$ substrate after PVD growth. The apparently white region indicates a poor selectivity for growing $Bi_2Se_3$. (b) SEM images captured from Sec. II A (LE) and Sec. II B (TE), further demonstrating the poor growth selectivity at the LE of the substrate (scale bar: 100 nm). Reduction of such white regions will enhance the yield and throughput of the Au-selectively grown $Bi_2Se_3$ device features. (c) Processing factors affecting the $Bi_2Se_3$ growth uniformity: distance between the $Bi_2Se_3$ powder holder and the leading edge of the substrate holder ($D_1$), distance between the LE of the substrate holder and LE of the substrate ($D_2$), furnace temperature (T), and growth time.

conditions, the holder of $Bi_2Se_3$ powder is placed at the same location in the tube; position parameters $D_1$ and $D_2$ have different values but $D_1 + D_2$ values remain a constant (i.e., the location of the substrate holder differs by a shift of $D_1$ while the distance between the LE of the target substrate and the powder holder remains the same). Figures 4(a)–4(c) depict the flow speed contour on top of the Si/$SiO_2$ substrate for process conditions No. 5, 6, and 7, respectively. Such a flow speed profile is important because it is related to the gas pressure and $Bi_2Se_3$ molecule concentration, as partially implied by Bernoulli equation analysis with approximation assumption. Bernoulli's equation suggests the decrease in velocity is associated with an increase in pressure. Since $Bi_2Se_3$ nucleation happens more frequently within the substrate area with the higher pressure (i.e., the higher capture frequency for $Bi_2Se_3$ molecules), it can be inferred using Bernoulli's principle that the deposition happens more actively in the substrate area with the lower gas flow speed.[33] In Figs. 4(a)–4(c), the flow speed contour profile at 5.3 m/s, which is approximately half of the maximum flow speed for the three cases, is plotted with the dotted lines. The dashed circles indicate the intersection of the 5.3 m/s contour profile and the center line. These simulation results imply that as $D_2$ decreases from 10 to 0 mm while $D_1 + D_2$ remains constant, the substrate area with flow speed less than 5.3 m/s increases by 87.1% (i.e., the distances between dashed circles and LEs for substrates No. 5, 6, and 7 are 0.31, 0.39, and 0.58 cm, respectively). This supports a correlation between the low-flow-speed regions (<5.3 m/s) and the

**TABLE I.** Seven sets of the processing parameters.

| Sample No | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| $D_1$ (mm) | 130 | 130 | 140 | 140 | 140 | 145 | 150 |
| $D_2$ (mm) | 10 | 0 | 0 | 5 | 10 | 5 | 0 |
| T (°C) | 500 | 500 | 500 | 500 | 500 | 500 | 500 |
| t (min) | 15 | 15 | 15 | 15 | 15 | 15 | 15 |

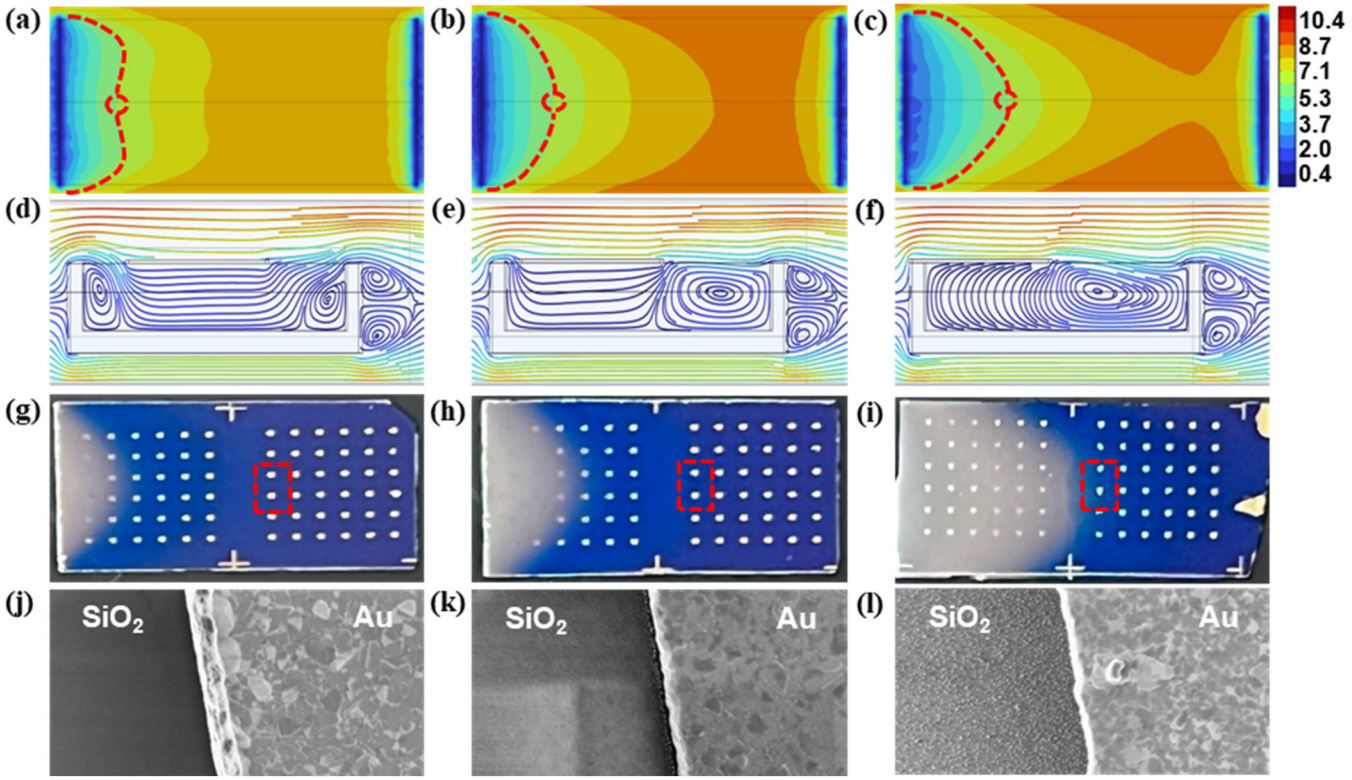



**FIG. 4.** COMSOL simulation and experimental results of the $Bi_2Se_3$ growth under various processing conditions (i.e., Condition No. 5: $D_1$ = 140 mm, $D_2$ = 10 mm, furnace temperature: 500 °C, growth time: 15 min; Condition No. 6: $D_1$ = 145 mm, $D_2$ = 5 mm, furnace temperature: 500 °C, growth time: 15 min; and Condition 7: $D_1$ = 150 mm, $D_2$ = 00 mm, furnace temperature: 500 °C, growth time: 15 min) with absolute position of the Si/$SiO_2$ substrates ($D_1$ + $D_2$) remaining the same for all three conditions: (a)–(c) display the top-view velocity profiles obtained by the COMSOL simulations at three processing conditions No. 5, 6, and 7, respectively; (d)–(f) display the corresponding side-view streamline maps; (g)–(i) are the optical images of the three samples experimentally processed with Conditions 5, 6, and 7, respectively; and (j)–(l) show the corresponding SEM images of the $Bi_2Se_3$ structures growth on the Si/$SiO_2$ substrates by using Conditions No. 5, 6, and 7, respectively. For each processing condition, the $Bi_2Se_3$ structures formed in the proximity of the first column of the right array are used for SEM imaging.

white regions observed in the optical images of the experimental samples, as shown in Figs. 4(g)–4(i).

The flow speed profile is not the only factor responsible for the formation of the apparently white region modulated by processing parameters $D_1$ and $D_2$. Figures 4(d)–4(f) show the simulated flow streamline distributions for three processing conditions. When the substrate position relative to the $Bi_2Se_3$ powder holder remains the same while varying the substrate holder location, the simulation results for these various cases demonstrate that a larger gap in front of the substrate (i.e., the large $D_2$ value) allows more carrier gas flowing toward the substrate holder's interior. As shown by the simulation result in Fig. 4(d), a vortex flow field is formed in the gap between the target substrate LE and the substrate holder. Such a configuration can indeed lower the local pressure on the substrate, thereby reducing the apparently white region (i.e., the region with the poor growth selectivity of $Bi_2Se_3$) and improving the effective yield and throughput of electrically isolated $Bi_2Se_3$ device features. Figures 4(j)–4(l) show the zoomed-in SEM images captured from the regions labelled with dashed boxes in OM images for three different processing conditions. These SEM results can serve as further experimental evidence to support the implication from our CFD simulation results that a large gap between the leading edges of the substrate and the substrate holder with hollow interior (i.e., the larger $D_2$ value) result in the smaller region with poor growth selectivity.

As shown in Figs. 2 and 3, the formation of unwanted apparently white regions (i.e., the regions with a poor growth selectivity of $Bi_2Se_3$ features gold and bare $SiO_2$ surfaces) is detrimental to the yield and throughput of the final $Bi_2Se_3$ device features. Our simulation/experiment-integrated work provides important technical insights toward addressing this issue. On the basis of the results in Fig. 4, we can quantitatively estimate the yields of the electrically isolated $Bi_2Se_3$ memristor channels resulted from the aforementioned processing conditions (i.e., Samples 5, 6, and 7). Here, the yield value is calculated by the number of the Au pad regions where growth selectivity is good (i.e., no continuous $Bi_2Se_3$ grains are formed on the bare $SiO_2$ region near the neighboring Au pad) normalized by the total Au pad number. Using this method, the

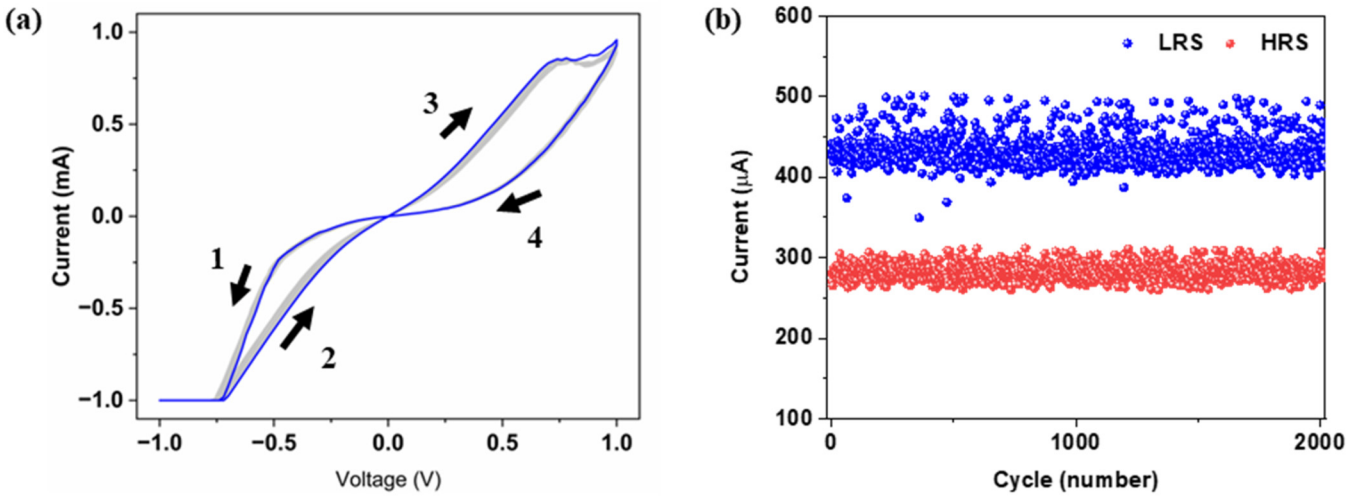



**FIG. 5.** Memristive switching characterization results measured from a representative vertically arranged $Bi_2Se_3$ memristor: (a) hysteric I–V characteristics measured from 50 consecutive cycles; (b) endurance characteristics of a pair of low-resistance and high-resistance states (LRS and HRS) repetitively set by $10^4$ pulse programming cycles.

yields of Samples 5, 6, and 7 are estimated to be 86.11%, 69.44%, and 43.05%, respectively. By involving more processing parameters such as temperature and growth time in both experimental and simulation analysis in the future, the yield of the device fabrication process could be further improved.

We further measured the hysteric I–V characteristics of a representative vertically arranged $Bi_2Se_3$ memristor made by using Condition No. 5, as shown in Fig. 5(a). For the measurement shown in Fig. 5(a), the voltage-sweep rate is 5 V/s, and the compliance current is set to 1 mA. In Fig. 5(a), the directions of four voltage-sweep processes (1–4) in a measurement cycle are labeled. During the negative voltage-sweep processes 1 and 2 (i.e., 0 to −1 to 0 V), the device conductance increases by 215% in a progressive way. During positive voltage-sweep processes 3 and 4 (0 to +1 to 0 V), the device conductance progressively changes back to its initial conductance states. Four voltage-sweep processes are highly repeatable over 50 cycles, as demonstrated in Fig. 5(a). Furthermore, we performed pulse programming to repetitively set the device to a pair of low-resistance state (LRS) and high-resistance state (HRS) and investigated its endurance property. Specifically, each cycle of pulse programming includes 10 positive voltage pulses (1 V, 1 ms) followed by 10 negative voltage pulses (−1 V, 1 ms). The instantaneous device conductance is sampled by a reading voltage pulse (0.2 V, 1 ms) after each programming pulse. In an endurance test, such a pulse programming cycle is repeated for $10^3$ times, as shown in Fig. 5(b). Figure 5(b) shows that the vertically arranged $Bi_2Se_3$ memristor made by Au-assisted PVD exhibits good endurance and holds the potential for neuromorphic computing applications.

## IV. SUMMARY AND CONCLUSIONS

We present research about the scalable fabrication of vertically arranged electrically isolated $Bi_2Se_3$ memristors in crossbar architecture. The fabrication route is termed the Au-assisted PVD growth. In this work, it has been observed that $Bi_2Se_3$ structures grown on Au layers exhibit 100-folds larger average crystal grain size and are more continuous in comparison with the grains non-specifically grown on bare $SiO_2$ substrates. This result indicates the catalytic role of Au layers in $Bi_2Se_3$ nucleation. The present work also provides the COMSOL CFD simulation results to elucidate the key processing parameters affecting the quality of grown crystalline structures as well as growth selectivity between Au and bare $SiO_2$ surfaces. Specifically, a series of experimental and CFD analyses show that the distance between $Bi_2Se_3$ powder and the target substrate and the distance between the leading edges of the substrate and the substrate holder are key processing parameters. With optimization of these parameters, we have demonstrated the production of uniform electrically isolated $Bi_2Se_3$ memristors arranged in crossbar-arrayed structures with an in-lab yield of 86%. The entire process is etch- and plasma-free, minimizing the process-induced damage to $Bi_2Se_3$ channels. Finally, we present the memristive switching results measured from as-fabricated vertically arranged $Bi_2Se_3$ memristors. Such devices exhibit repeatable switching behaviors and high endurance for cyclic operations. This work provides the scalable fabrication methods for layered-materials-based vertically stacked memristor devices with no need of additional etching or lithographic techniques, which can potentially serve as an important approach for producing hardware-based neuromorphic sensory systems.

## ACKNOWLEDGMENTS

This work is supported by NSF (No. ECCS-2331169). The authors would like to thank the staffs of the University of Michigan's Lurie Nanofabrication Facility for providing support for device fabrication.

## AUTHOR DECLARATIONS

### Conflicts of Interest

The authors have no conflicts to disclose.

### Author Contributions

**Seung jun Ki:** Conceptualization (lead); Formal analysis (equal); Investigation (lead); Methodology (equal); Writing – original draft (lead). **Shiwoo Lee:** Formal analysis (lead); Validation (lead); Writing – original draft (supporting). **Mingze Chen:** Investigation (supporting); Methodology (equal); Resources (lead); Writing – original draft (supporting). **Xiaogan Liang:** Conceptualization (equal); Funding acquisition (lead); Project administration (lead); Supervision (lead); Writing – review & editing (lead).

## DATA AVAILABILITY

The data that support the findings of this study are available within the article.

## REFERENCES

[1]H. Nam, B.-R. Oh, P. Chen, M. Chen, S. Wi, W. Wan, K. Kurabayashi, and X. Liang, Sci. Rep. **5**, 10546 (2015).
[2]M. Chen, H. Nam, S. Wi, G. Priessnitz, I. M. Gunawan, and X. Liang, ACS Nano **8**, 4023 (2014).
[3]H. Nam, S. Wi, H. Rokni, M. Chen, G. Priessnitz, W. Lu, and X. Liang, ACS Nano **7**, 5870 (2013).
[4]S. Wi, M. Chen, D. Li, H. Nam, E. Meyhofer, and X. Liang, Appl. Phys. Lett. **107**, 062102 (2015).
[5]S. Wi, H. Kim, M. Chen, H. Nam, L. J. Guo, E. Meyhofer, and X. Liang, ACS Nano **8**, 5270 (2014).
[6]S. Ki, M. Chen, and X. Liang, J. Vac. Sci. Technol. B **39**, 062201 (2021).
[7]Y. Park, B. Ryu, S. J. Ki, X. Liang, and K. Kurabayashi, Adv. Mater. Interfaces **8**, 2101291 (2021).
[8]Y. Park, B. Ryu, S. J. Ki, B. McCracken, A. Pennington, K. R. Ward, X. Liang, and K. Kurabayashi, ACS Nano **15**, 7722 (2021).
[9]J. F. Sierra, J. Fabian, R. K. Kawakami, S. Roche, and S. O. Valenzuela, Nat. Nanotechnol. **16**, 856 (2021).
[10]E. C. Ahn, npj 2D Mater. Appl. **4**, 17 (2020).
[11]S. Ki, M. Chen, and X. Liang, IEEE Nanotechnol. Mag. **17**, 24 (2023).
[12]D. Li, B. Wu, X. Zhu, J. Wang, B. Ryu, W. D. Lu, W. Lu, and X. Liang, ACS Nano **12**, 9240 (2018).
[13]S. J. Ki, J. Kim, M. Chen, and X. Liang, Appl. Phys. Lett. **123**, 223501 (2023).
[14]X. Zhu, D. Li, X. Liang, and W. D. Lu, Nat. Mater. **18**, 141 (2019).
[15]M. Wang *et al.*, Nat. Electron. **1**, 130 (2018).
[16]W. Huh, D. Lee, and C. H. Lee, Adv. Mater. **32**, 2002092 (2020).
[17]N. Tulina, A Rossolenko, I. Shmytko, N. Kolesnikov, D. Borisenko, S. Bozhko, and A. Ionov, Mater. Lett. **158**, 403 (2015).
[18]A. Zotov, V. Sirotkin, A. Il'in, O. Trofimov, D. Borisenko, N. Kolesnikov, and V. Tulin, Chaos, Solitons Fractals **143**, 110542 (2021).
[19]C. Yin *et al.*, Adv. Funct. Mater. **32**, 2108455 (2022).
[20]M. Chen, S. J. Ki, and X. Liang, ACS Appl. Electron. Mater. **5**, 3830 (2023).
[21]S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, Nano Lett. **10**, 1297 (2010).
[22]P. M. Sheridan, F. Cai, C. Du, W. Ma, Z. Zhang, and W. D. Lu, Nat. Nanotechnol. **12**, 784 (2017).
[23]S. Choi, J. H. Shin, J. Lee, P. Sheridan, and W. D. Lu, Nano Lett. **17**, 3113 (2017).
[24]S. Choi, P. Sheridan, and W. D. Lu, Sci. Rep. **5**, 10492 (2015).
[25]T. Chang, S.-H. Jo, and W. Lu, ACS Nano **5**, 7669 (2011).
[26]J. Rofeh, A. Sodhi, M. Payvand, M. A. Lastras-Montaño, A. Ghofrani, A. Madhavan, S. Yemenicioglu, K.-T. Cheng, and L. Theogarajan, *2015 IEEE 65th ECTC*, 26–29 May 2015, San Diego, CA (IEEE, 2015), p. 957.
[27]M. Rao *et al.*, Nature **615**, 823 (2023).
[28]B. Ryu, D. Li, C. Park, H. Rokni, W. Lu, and X. Liang, ACS Appl. Mater. Interfaces **10**, 43774 (2018).
[29]B. Ryu, J. S. Yoon, E. Kazyak, K.-H. Chen, Y. Park, N. P. Dasgupta, and X. Liang, Nanoscale **12**, 16917 (2020).
[30]M. Chen, S. Ki, and X. Liang, J. Vac. Sci. Technol. B **39**, 062203 (2021).
[31]R. Huang, S. L. Benjamin, C. Gurnani, Y. Wang, A. L. Hector, W. Levason, G. Reid, and C. De Groot, Sci. Rep. **6**, 27593 (2016).
[32]W. Ahn, H. Lee, H. Kim, M. Leem, H. Lee, T. Park, E. Lee, and H. Kim, Phys. Status Solidi RRL **15**, 2000533 (2021).
[33]J. Wei, P. L. Ong, F. E. Tay, and C. Iliescu, Thin Solid Films **516**, 5181 (2008).