Modelling the Effect of the DC Link Decoupling Capacitor of a Commutation Power Loop Using a Thevenin-Based Frequency Domain Approach

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***Abstract*—The high commutation speed of wide band-gap devices causes undesired voltage overshoots and oscillatory behavior observed across the drain-source port. The mitigation of these voltage overshoots and oscillations caused by the resonant interaction between the commutation loop parasitic inductance and the switch parasitic output capacitance requires additional design considerations. In this work, a Thevenin-based frequency domain approach for modelling the switch voltage overshoot and oscillations with respect to the commutation power loop is proposed. The switching transition and its associated slew rate is modelled using a clamped-ramp function. The two figures of merit used to quantify the effect of the circuit elements in the commutation power loop with respect to the resonant oscillations are the voltage overshoot and time to steady state. Using the clamped-ramp function and the two figures of merit, the effect of the parasitic inductance and the decoupling capacitor on the power loop is analyzed. The trends observed from the analyses are used to obtain recommendations regarding the sizing and placement of the decoupling capacitor in the power loop. The proposed Thevenin-based frequency domain model is experimentally validated by comparing the analytical results with both the LTspice simulations and the experimental waveforms for a SiC-based 400 V, 20 A double pulse test.**

***Index Terms*—commutation power loop, decoupling capacitors, decoupling factor, voltage overshoot, time to steady state, Thevenin model, clamped-ramp function, parasitic inductances, slew rates, double pulse test.**

I. Introduction

A major concern in the design of power electronic converters are the voltage spikes/overshoots accompanied by the oscillations observed across the output port of the switching devices (that is, the drain-to-source port for MOSFET-based power converters) [1]. These resonant overshoots and oscillations are primarily caused by the interaction between parasitic stray inductances associated with the commutation power loop and the parasitic output capacitance of the switches [1]–[3]. These parasitic stray inductances are present in both the PCB traces and in external wiring from the power supply [3]. Additionally, the lead inductances associated with traditional switch packages (such as TO-247 or TO-247-4) increases the overall parasitic inductance present in the commutation power loop of a converter [4].

Wide band-gap devices are superior to traditional silicon devices due to their higher breakdown voltage, higher operating temperatures, smaller on-state resistances, and higher switching frequencies [5]. However, the tradeoff to using these devices are in the excessive voltage spikes, oscillatiory/ringing behavior and severe common-mode (CM) currents [6]. These voltage overshoots have a significant impact on the switching performance and efficiency of power converters. The voltage spikes and oscillations lead to added switch stresses, increased losses, reduced efficiency, reduced reliability and lifetime, and electromagnetic interference (EMI) issues [7]. Additionally, the oscillations present across the drain-source voltage of the switch can be propagated to the gate loop of the device through the gate parasitics. This can cause oscillations/spikes across the gate-to-source voltage which can lead to mis-triggering of the switching device and possible shoot-through scenarios [5]. These voltage overshoot and oscillatory challenges are exacerbated by the shift from traditional silicon-based devices to wide-bandgap devices due to their high commutation speeds. Therefore, additional EMI considerations are taken when implementing them in power converters [5], [8]. There are different voltage suppression techniques used to mitigate the voltage spikes/overshoots and ringing behavior. These include the design of an optimal PCB layout for parasitic inductance reduction [5], using ferrite beads in power loop [9], bare-die technology [10], increasing gate resistances [11], snubber circuits [12], and decoupling capacitors [13].

This work focuses on the modelling and analysis of the voltage overshoot and oscillations propagated through the commutation power loop by the switching devices. The effect of decoupling capacitors as an overvoltage suppression technique is highlighted. The two figures of merit used in characterizing the oscillations are the "voltage overshoot" and "time to steady state". The time to steady state is considered as the duration it takes for the peak of the decaying oscillations to decay to $\pm 1\%$ of the input DC voltage. This manuscript is organized as follows. Section II introduces the proposed Thevenin-based frequency domain modelling approach of the

This work is partly supported by the National Science Foundation (NSF) under the Award Number 2205934, which is gratefully acknowledged.

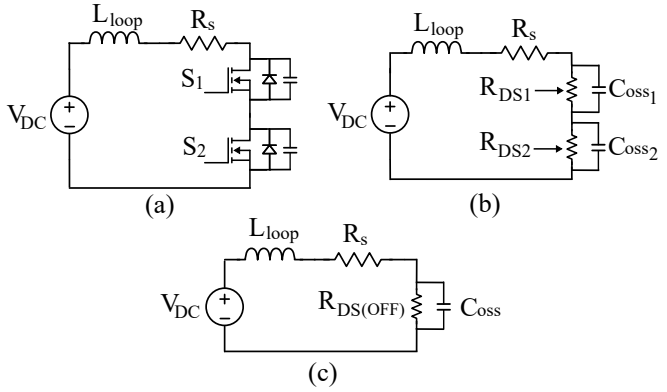


Fig. 1. Commutation power loop of a switching half-bridge: (a) using actual MOSFETs, (b) using MOSFET approximate model, and (c) equivalent circuit for operating modes.

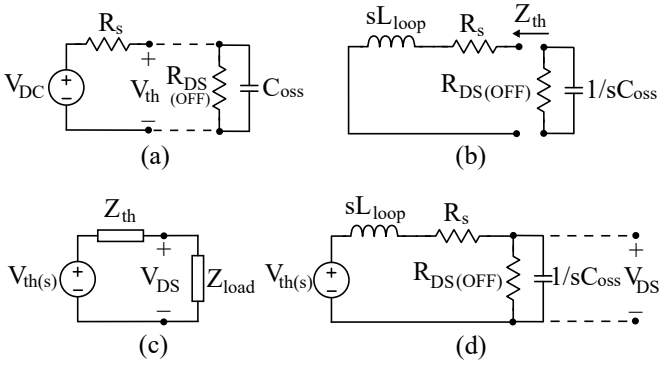


Fig. 2. Proposed Thevenin modelling approach: (a) large-signal equivalent circuit to determine Thevenin voltage, (b) small-signal equivalent circuit to determine Thevenin impedance, (c) generic Thevenin equivalent model, and (d) Thevenin equivalent model for the commutation power loop.

commutation power loop. Section III analyzes the effect of introducing a decoupling capacitor in the commutation loop which is compared with an LTspice simulation. Section IV describes the hardware setup, experimental results and LTspice simulations used to validate the propsed analytical model. Finally, Section V presents the conclusions in this manuscript.

II. Thevenin-based Modelling of the Commutation Power Loop Using a Clamped Ramp Perturbation

In Fig. 1, the layout and operation of the commutation power loop of a switching half-bridge is shown. The commutation power loop refers to the high-frequency path of current flow due to the exchange of charges that occur between the complementary devices in a half-bridge during a switching transition. The focus of this paper is on power converters that have a DC-link based commutation power loop. The commutation power loop consists of the input DC supply, the parasitic stray inductances and resistances, and the switching half-bridge as shown in Fig. 1 (a). The lead inductances of the switch package are lumped in with the equivalent stray inductances in the path. MOSFETs have a lot of non-linear behavior associated with it. As such, the parallel combination of its variable R_{DS} and C_{oss} is used to get an approximate behavior of the MOSFET in our analytical approach as shown in Fig. 1 (b). The R_{DS} is the drain-to-source resistance whereas the C_{oss} is the output drain-to-source capacitance.

In this section, to illustrate the proposed Thevenin modelling approach, the switching node of the half-bridge is left unconnected for a no-load switching operation. Fig. 1 (c) shows the equivalent circuit for the symmetric modes of operation of the network. The resonant oscillations are a result of the interaction between the parasitic loop inductance and the C_{oss} of the switch transitioning to the off state. In this work, the C_{oss} of the off-switch is considered to be a constant value during the switching transition. L_{loop} represents the overall parasitic inductance in the commutation loop including the internal wire bond and external lead inductances of the switch. $R_{DS(off)}$ represents the off-state channel resistance. R_s represents the equivalent series resistance in the commutation loop including the $R_{DS(on)}$ of the complementary switch turning on. Since the $R_{DS(off)}$ of the FET tends to very large values, the commutation power loop can be considered as an effective series RLC network.

The Thevenin-based analytical model utilizes the following tools: large signal analysis for DC operating point, small-signal analysis for determining the equivalent impedance seen from the V_{DS} port, and the Thevenin equivalent modelling of the network. Using Fig. 1 (c), the proposed modelling approach for analyzing the commutation loop is illustrated in Fig. 2 below. The switch is disconnected from the commutation power loop to determine the Thevenin voltage and impedance. A large-signal DC operating point analysis is used to determine the Thevenin voltage as shown in Fig. 2 (a). Then, a small-signal frequency domain analysis is used to determine the Thevenin impedance as shown in Fig. 2 (b). The Thevenin equivalent model of the commutation loop is determined as shown in Fig. 2 (d). Using Fig. 2 (c) and Fig. 2 (d), the following equations can be derived:

$$H(s) = \frac{V_{DS}(s)}{V_{th}(s)} = \frac{Z_{load}}{Z_{th} + Z_{load}} \tag{1}$$

$$Z_{th} = R_s + sL_{loop} \tag{2}$$

$$Z_{load} = R_{DS(off)} \parallel \left[\frac{1}{sC_{oss}}\right] \tag{3}$$

$H(s)$ represents the s-domain transfer function. $V_{DS}(s)$ represents the s-domain drain-source voltage of the off-switch. $V_{th}(s)$ represents the s-domain Thevenin voltage across the drain-source port. Z_{th} represents the Thevenin equivalent impedance. Z_{load} represents the impedance offered by the MOSFET approximate model. $R_{DS(off)}$ is considered as an infinitely large resistance. Upon substituting (2) and (3) in (1), the s-domain transfer function can be approximated as:

$$H(s) = \frac{V_{DS}(s)}{V_{th}(s)} = \frac{1}{s^2 + (\frac{R_s}{2L_{loop}})s + \frac{1}{L_{loop}C_{oss}}} \tag{4}$$

The poles s, damping factor α, and angular resonant frequency ω_o are determined from the characteristic equation of the transfer function and are given as:

$$s_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_o^2} \tag{5}$$

$$\alpha = \frac{R_s}{2L_{loop}} \tag{6}$$

$$\omega_o = \frac{1}{\sqrt{L_{loop}C_{oss}}} \tag{7}$$

The voltage overshoots and oscillations occur because the commutation loop is typically under-damped which implies that $\alpha < \omega_o$. From (6) and (7), it can be observed that the commutation loop parasitic inductance L_{loop} plays a significant role in the V_{DS} voltage response across the switch. The effect of L_{loop} is more emphasized due to the decreasing trend of the $R_{DS(on)}$ in newer generation SiC wide band-gap devices. L_{loop} should be minimized to improve the damping in the DC-link network especially at high commutation speeds. Increased damping causes a reduction in the V_{DS} voltage overshoot and a faster steady-state time. The s-domain V_{DS} voltage is determined from (4) and the corresponding time-domain response is derived by taking the inverse Laplace transform.

The accuracy of the calculated V_{DS} voltage response is heavily dependent on how the Thevenin voltage is modelled in the s-domain, that is, $V_{th}(s)$. In this proposed modelling approach, the Thevenin voltage $V_{th}(s)$ serves as the input perturbation to the commutation power loop and the drain-source voltage V_{DS} is the output voltage response. In Fig. 2 (a), the large-signal time domain Thevenin voltage is $V_{th}(t) = V_{DC}$. In the frequency s-domain, this translates to $V_{th}(s) = V_{DC}/s$ which corresponds to a step-change in the V_{DS} voltage for an idealized switching transition. However, practical switches have a dV/dt and dI/dt slew rate associated with the switching transition. The slew rate of the switch is due to the rise and fall times, the gate loop design, the power loop design, and loading condition of the power converter. Hence, the Thevenin voltage $V_{th}(s)$ is modelled to include the switching transition using a function coined the term "clamped-ramp" in this manuscript.

The clamped-ramp function consists of the subtraction of a time-shifted ramp signal from an original ramp signal with both ramps having the same slope/slew rate as shown in (8). The frequency domain translation of the clamped-ramp function is shown in (9). Note that "a" refers to the time duration between both ramps which corresponds to the voltage rise time. The corresponding $slope$ is given by V_{DC}/a. The inclusion of the slope in the clamped ramp function captures the impact of the device slew rate on the voltage overshoot.

$$V_{th}(t) = slope \times [t \cdot u(t) - (t-a) \cdot u(t-a)] \tag{8}$$

$$V_{th}(s) = slope \times \left[\frac{1}{s^2} - \frac{e^{-as}}{s^2}\right] \tag{9}$$

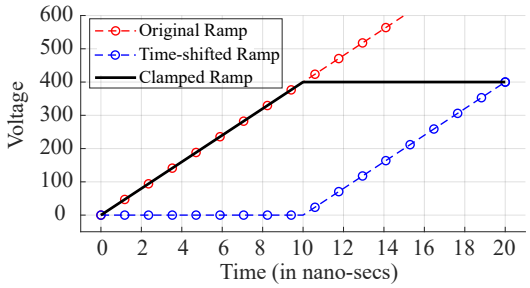


Fig. 3. Clamped-Ramp function for modelling switching transition.

The impact of the commutation loop inductance L_{loop} on the voltage overshoot and time to steady state using a parametric sweep is shown in Fig. 4 (a). The parameters for this analysis are: $V_{DC} = 400\,V$, $a = 10\,ns$, $slope = 40\,V/ns$, $C_{oss} = 144\,pF$ and $R_s = 100\,m\Omega$. L_{loop} is swept from 1nH to 100 nH in this parametric analysis. Fig. 4 (a) shows that decreasing L_{loop} from 100 nH to 1 nH causes a decreasing trend in both the voltage overshoot and time-to-steady state due to increased damping in the system as predicted by (6). However, when L_{loop} is decreased to around 20 nH, there is a sudden small rise and parabolic fall as L_{loop} is further decreased down to 1 nH. This parabolic/oscillatory behaviour observed around the lowest values of L_{loop} can be attributed to the phase difference between the two transient small-signal responses of the system to the two time-shifted ramp functions that form the clamped-ramp signal. The clamped-ramp perturbation is constructed from two individual ramp signals that have a phase shift of "a" between them. Hence, the resulting V_{DS} output voltage response is dependent on

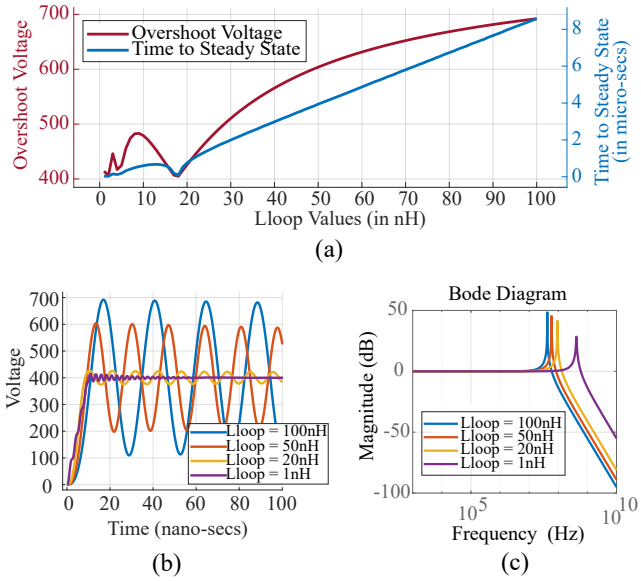


Fig. 4. Analytical results for parametric sweep of commutation parasitic loop inductance: (a) effect of loop inductance on voltage overshoot and time to steady state, (b) time-domain voltage response across drain-to-source of switch, (c) corresponding bode plots of transfer function.

the constructive or destructive interaction of the two transient small-signal responses corresponding to their respective ramp signals. In this analysis, $a = 10\,ns$ and as such, for larger values of L_{loop}, the resonant period T_o (that is, inverse of resonant frequency) is larger than 10 ns. Hence, the behavior due to the phase difference between the two small-signal responses is not as dominant. However, for $L_{loop} \leq 20\,nH$ which corresponds to the resonant period $T_o \leq 10\,ns$, the small-signal transient oscillations occur within the voltage rise time "a". This causes the constructive or destructive behavior due to the phase difference between the two small-signal transient responses to be more dominant. Fig. 4 (b) shows a significant improvement in the $V_{DS}(t)$ voltage response as L_{loop} is decreased to 1 nH. The corresponding bode plot in Fig. 4 (c) shows the increase in resonant frequency following a decreasing trend in L_{loop} which is as expected.

III. Modelling the Effect of Adding a Decoupling Capacitor to the Commutation Power Loop

Decoupling capacitors are incorporated into power electronic systems to provide a very low impedance path to the ground for high-frequency oscillations within the network. The addition of decoupling capacitors is a widely used voltage suppression technique to mitigate against the switch overvoltages and oscillations [13]. The decoupling capacitors splits the commutation loop into multiple parts. This causes multiple resonant loops to occur leading to lower frequency oscillations which can introduce EMI issues to the system. Decoupling capacitors reduce the effective parasitic inductive path for the highest frequency oscillations in the commutation loop. Hence, the placement of the decoupling capacitors in close proximity to the switching half-bridge is a design consideration that improves switching performance.

A. Analyzing the commutation Loop with the Thevenin-based modelling approach

In this section, a double pulse test (DPT) circuit with the decoupling capacitor at the DC link is considered as shown in Fig. 5. The V_{DS} voltage overshoot and ringing across the bottom-side switch during its hard turn-off transition is analyzed. The internal parasitic elements of the decoupling capacitor, that is, ESL and ESR are included in the model. In Fig. 5, the paths highlighted in red show the power path for the double pulse current. The paths highlighted in green show the decoupling path for the high-frequency oscillations termed the "decoupling loop". In Fig. 5 (a), the load inductor current flows through the channel of the bottom-side switch when it is turned on. In Fig. 5 (b), the switch is turned off and the load inductor current flows through the body diode of the top-side switch thereby shorting out its C_{oss}. The resonant oscillation occurs across the C_{oss} of the bottom-side switch due to the charges propagated in the paths highlighted in green forming the decoupling loop. Note that the MOSFET approximate model of the $R_{DS(on)}$ in parallel with the C_{oss} is used in this analysis as shown in Fig. 5 (c). In Fig. 5, the addition of the decoupling capacitor splits the commutation power loop into two parts. L_a and R_a represent the parasitic inductances and resistances between the decoupling capacitor and the half-bridge (including the leads of the switch). L_b and R_b represent the parasitic inductances and resistances between the DC input and the decoupling capacitor.

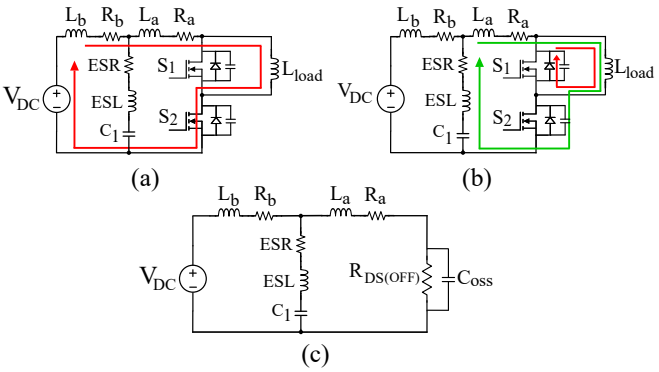


Fig. 5. Double pulse test hard turn-off transition of bottom-side switch: (a) bottom-side switch is ON, (b) bottom-side switch is OFF and, (c) equivalent circuit using MOSFET approximate model when bottom-side switch is OFF.

Using Fig. 5, the analytical modelling approach for the commutation loop is illustrated in Fig. 6. The switch is disconnected from the commutation power loop to determine the Thevenin voltage and impedance. A large-signal DC operating point analysis is used to determine the Thevenin voltage as shown in Fig. 6 (a). A small-signal frequency domain analysis is used to determine the Thevenin impedance as shown in Fig. 6 (b). The resulting Thevenin equivalent model of the commutation loop is shown in Fig. 6 (c). By analyzing Fig. 6 (b), the Thevenin impedance can be given by:

$$Z_{th} = R_a + sL_a + [Z_{cap,1} \parallel (R_b + sL_b)] \tag{10}$$

$$Z_{cap,1} = ESR + s.ESL + \frac{1}{sC_1} \tag{11}$$

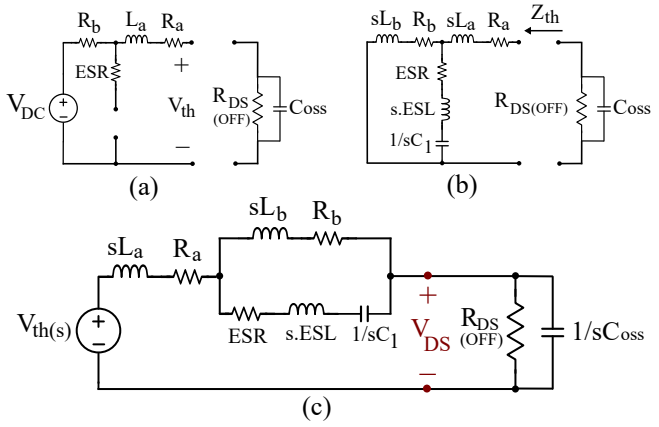


Fig. 6. Thevenin-based modelling of the commutation loop with a decoupling capacitor: (a) equivalent circuit for determining Thevenin voltage, (b) equivalent circuit for determining Thevenin impedance, and (c) Thevenin equivalent model.

The s-domain transfer function $H(s)$ of the commutation loop is re-calculated using (1) by substituting in (10) and (11). The s-domain $V_{DS}(s)$ voltage can be determined using the new transfer function as shown in (12).

$$V_{DS}(s) = V_{th}(s)\left[\frac{R_{DS(off)} \parallel \frac{1}{sC_{oss}}}{Z_{th} + R_{DS(off)} \parallel \frac{1}{sC_{oss}}}\right] \tag{12}$$

An LTspice simulation of Fig. 5 is used to validate the accuracy of the proposed Thevenin model in Fig. 6 (c). The V_{DS} waveform from the LTspice simulation is compared to the analytical model. The specifications of the double pulse test case study are listed in Table I. The manufactuer spice model of the SiC switch provides the internal die parasitic inductance (L_{die}) value and is also used in the LTspice simulation. The parasitic inductance of the leads of the TO247-4 package is estimated using the loop area formed between the leads and the PCB. Hence, the total parasitic inductance offered by each switch is given in (13). The total decoupling loop inductance considering the parasitics in the switch and PCB is determined using (14). Finite element analysis (FEA) via the Ansys Q3D platform is used to extract the values of the parasitic inductances and resistances present in the PCB layout. The values from the FEA analyses are validated using the Keysight E4990A impedance analyzer. The series parasitic resistances in the commutation loop includes the $R_{DS(on)}$ of the complementary switch. During the switching transition, there is a transient rise in this $R_{DS(on)}$ value due to the body diode conduction. This value is extracted from the LTspice simulation. The total decoupling loop resistance is determined using (15).

$$L_{switch} = L_{die} + L_{leads} \tag{13}$$

$$L_a = L_{decoupling} + 2L_{switch} \tag{14}$$

$$R_a = R_{decoupling} + R_{DS(on)} + R_{DS(on),transient} \tag{15}$$

In Fig. 7 (a), the comparative analysis shows a very similar behavior in the V_{DS} voltage profile determined from both the analytical model and the LTspice simulation. The voltage overshoot and resonant frequency of the oscillations seen in both cases are approximately the same. In both cases, the voltage overshoot and resonant frequency are estimated to be around 437 V and 72 MHz respectively. Both waveforms reach a steady state value around 210 ns. These similarities indicate that the analytical model is a good method for predicting the response of the V_{DS} voltage across a switch undergoing a hard turn-off transition. In Fig. 7 (a), it can be observed that the resulting slew rates of both waveforms are different. This can be attributed to the assumption taken that the MOSFET undergoes a constant linear change during the entire switching transition. In practical switching devices, this is not the case as the MOSFET is observed to have a non-linear behavior during certain parts of the switching transition. This non-linear behavior is contingent on the power converter operation and other non-idealities in the system. Fig. 7 (b) shows the V_{DS} response due to the analytical model.

TABLE I
DOUBLE PULSE TEST CASE STUDY SPECIFICATIONS

Parameter	Symbol	Value
DC Link Voltage	V_{DC}	400 V
Pulse Current	I_{pulse}	0 - 20 A
Load Inductor	L_{load}	300 μH
Voltage Rise time	a	12.5 ns
Slew Rate	$slope$	32 V/ns
Wolfspeed SiC Switch Part No: C3M0030090K TO247-4 package	C_{oss}	144pF
	$R_{DS(on)}$	30mΩ
	L_{die}	3.912 nH
	L_{leads}	6.5 nH
	L_{switch}	10.412 nH
Decoupling path stray inductance	$L_{decoupling}$	10.34 nH
Total decoupling loop inductance	L_a	31.164 nH
Bulk loop inductance	L_b	280 nH
Total commutation loop inductance	L_{loop}	311.164 nH
Transient $R_{DS(on)}$ (from LTSpice)	$R_{DS(on),transient}$	250 mΩ
Decoupling path resistance	$R_{decoupling}$	25 mΩ
Total decoupling loop resistance	R_a	305 mΩ
Bulk loop resistance	R_b	100 mΩ
Decoupling Capacitance Part No: CGA9Q1C0G2J104J280KC	C_1	100 nF
	ESL	2 nH
	ESR	130 mΩ

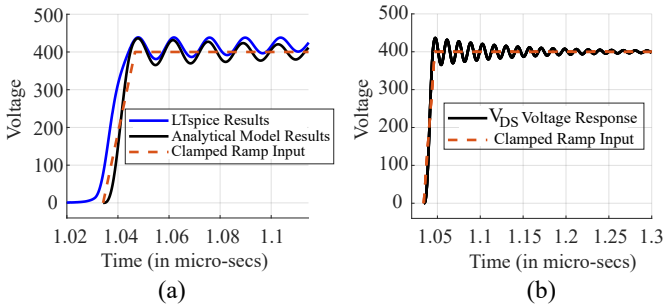


Fig. 7. Comparing the LTspice results with the analytical model: (a) superimposing the LTspice simulation results with the analytical model results, (b) overall voltage response using the proposed Thevenin analytical model.

B. Effects of Decoupling Capacitance, Decoupling Factor and the Decoupling Loop Inductance

In this section, the effect of the decoupling capacitor C_1, decoupling factor, and the parasitic decoupling loop inductance L_a is discussed. A parametric sweep of the decoupling capacitance C_1 is carried out to highlight its effect as shown in Fig. 8. This parametric sweep is carried out using values from 100 pF to 100 nF at 100 pF increments. The same case study values from Table I are used for the other parameters in this analysis. To generalize the effect of the decoupling capacitance with respect to the C_{oss} of the FET, a term coined the decoupling factor "D" is introduced. The decoupling factor

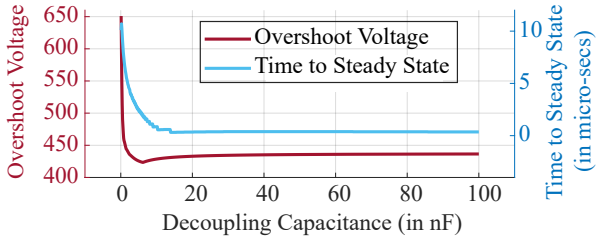


Fig. 8. Effect of decoupling capacitance on the voltage overshoot and time to steady state.

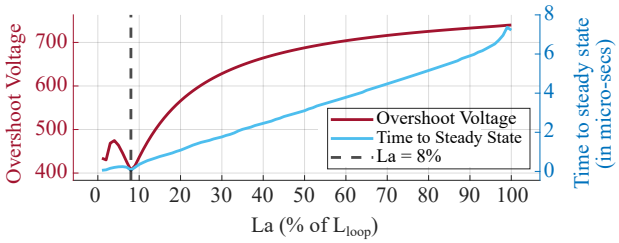


Fig. 10. Effect of varying parasitic decoupling loop inductance on the overshoot voltage and time to steady state.

is the ratio of the decoupling capacitance C_1 to the C_{oss} of the switch as shown in (16).

$$D = \frac{C_1}{C_{oss}} \tag{16}$$

Fig. 9 (a) shows the impact of the decoupling factor D on the voltage overshoots and time to steady state. As the decoupling factor D increases, the voltage overshoot and time to steady state both decrease up to a minimum value referred to as the "inflection point". As the decoupling factor D increases past the inflection point, there is a small rise in the voltage overshoot. This small rise is followed by a saturation profile in both the voltage overshoot and time to steady state upon any further increase of the decoupling factor. In the saturation region, the change in decoupling capacitance has minimal impact on the change in the voltage overshoot. This behavior is as expected following the trends predicted in [13]–[15]. The decoupling capacitance that yields this minimum voltage overshoot (or inflection point) is the optimal decoupling capacitance that can provide the best switching

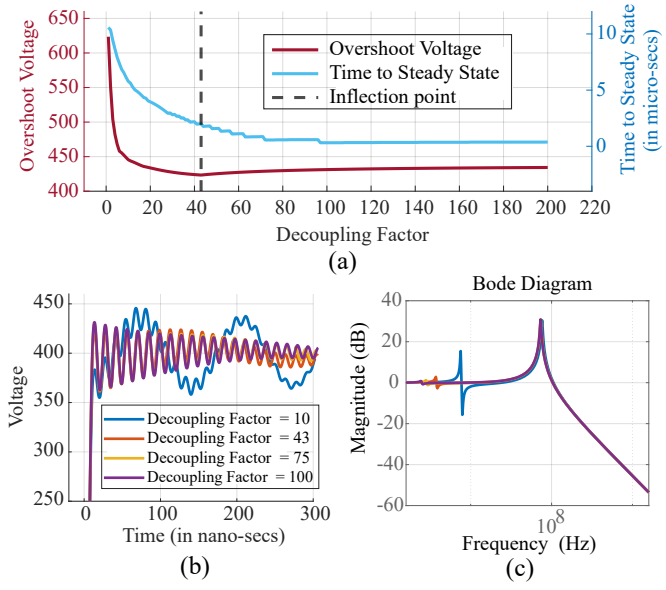


Fig. 9. Varying the decoupling factor: (a) effect of decoupling factor on the voltage overshoot and time to steady state, (b) V_{DS} time-domain voltage response and, (c) corresponding bode plots.

performance for this scenario. In Fig. 9 (a), the inflection point occurs at $D = 43$. Fig. 9 (b) shows the time-domain V_{DS} voltage response to different decoupling factors and Fig. 9 (c) represents the corresponding bode plots.

The physical placement of the decoupling capacitor is an important factor in maximizing the improvement in the V_{DS} behavior. The decoupling capacitors should be located as close as possible to the source of the perturbations which are the switches. This is to minimize the parasitic decoupling loop inductance L_a which improves the switching performance. A parametric sweep of the inductance L_a as a percentage of the total loop inductance L_{loop} (from Table I) is carried out in Fig. 10. It can be observed that the voltage overshoot and time to steady state have a decreasing trend with the decrease in L_a as expected. In Fig. 10, the smallest overshoot voltage occurs when $L_a = 8\%$. Hence, a good rule of thumb is to design and place the decoupling capacitors such that $L_a \leq 10\%\ of\ L_{loop}$. The reduction of L_a to really low values causes the ESL of the decoupling capacitor to play a more dominant role in the voltage overshoot and oscillatory behavior.

A design consideration in traditional power converters is to maximize the decoupling capacitance as constrained by the design layout. Fig. 11 illustrates the effect of varying the decoupling factor for different decoupling loop inductance L_a values. L_{loop} is the same as shown in Table I whereas L_a and L_b are treated as percentages of L_{loop} for this analysis. From Fig. 11, it can be observed that as the L_a percentage is increased, the minimum voltage overshoot offered by the decoupling factor at the inflection point increases. This is as expected because increasing the decoupling loop inductance L_a minimizes the effect of the decoupling capacitor. As shown in Fig. 11, the largest inflection-point decoupling factor is 31 for this case study. Hence, an approximate good rule of thumb is to size the decoupling capacitance to at least 50 times larger than the C_{oss} of the switch, that is, $C_1 \geq 50\, C_{oss}$. This would provide a good enough decoupling effect with respect to the suppression of the spikes and damping of the oscillations. In highly power dense designs, detailed analyses on the optimal decoupling capacitor sizing should be carried out.

C. Effects of the ESL and ESR of the Decoupling Capacitor

The decoupling capacitor can be modelled as a series RLC circuit considering the ESL and ESR. Typically, multiple capacitors are placed in parallel to reduce the ESL and ESR

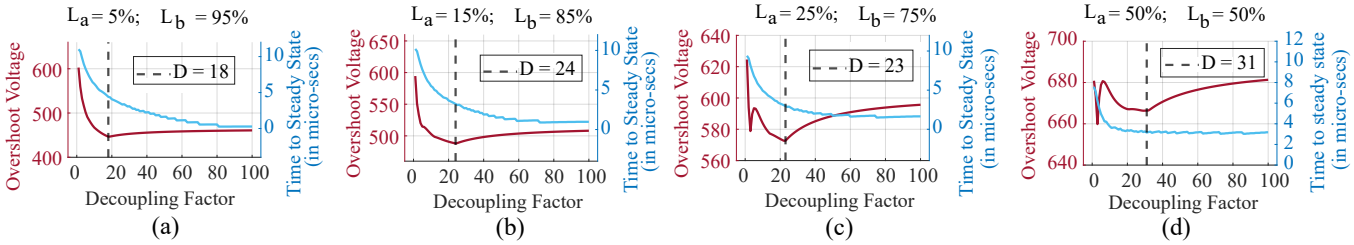


Fig. 11. Parametric sweep of decoupling factor for different decoupling loop inductance (L_a) values: (a) L_a is 5% of L_{loop}, (b) L_a is 15% of L_{loop}, (c) L_a is 25% of L_{loop}, and (d) L_a is 50% of L_{loop}.

elements while increasing the overall capacitance. The high frequencies present in the commutation power loop can exceed the self-resonance frequency of the capacitor. This causes the ESL of the decoupling capacitor to be the more dominant element and implies that the capacitor effectively offers an inductive impedance in the commutation loop. The relative magnitude of the ESL is typically smaller than the commutation loop inductance. Therefore, the decoupling capacitor can still provide the lowest impedance paths to ground for the highest frequency components. This phenomenon would still provide the voltage suppression and damping required across the V_{DS} of the switching devices. In Fig. 12 (a), the effect of the ESL on the V_{DS} voltage is shown. As the ESL is reduced, the overshoot voltage and time to steady state follow a decreasing trend as expected. In Fig. 12 (b), the ESR has a negligible effect on both the overshoot voltage and time to steady state. This is expected due to the low values associated with the ESR of the decoupling capacitors.

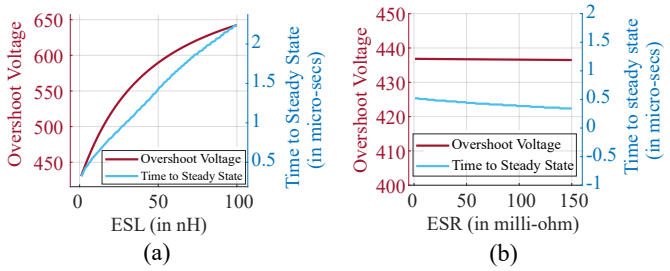


Fig. 12. Effects of the ESL and ESR of the decoupling capacitor: (a) sweeping the ESL and, (b) sweeping the ESR.

IV. Experimental Results and Discussion

In this section, a double pulse test setup is used to experimentally validate the accuracy of the proposed Thevenin-based analytical model as shown in Fig. 13. The double pulse test is carried out on one of the half-bridges of a SiC-based three-phase inverter which is the device under test (DUT). The focus of this experiment is on the hard turn-off switching transition of the bottom-side switch. There is a distributed capacitor network at the bulk portion of the commutation loop. This distributed capacitor network absorbs any second-order low-frequency oscillations generated from the

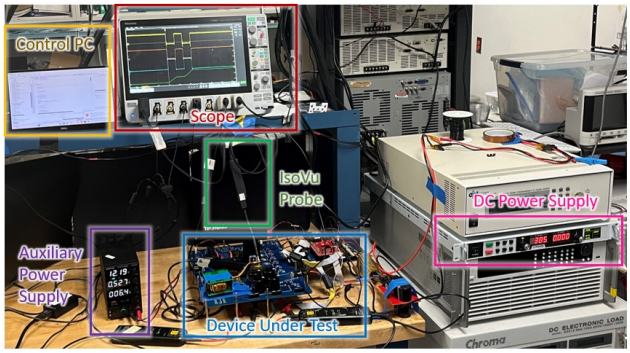
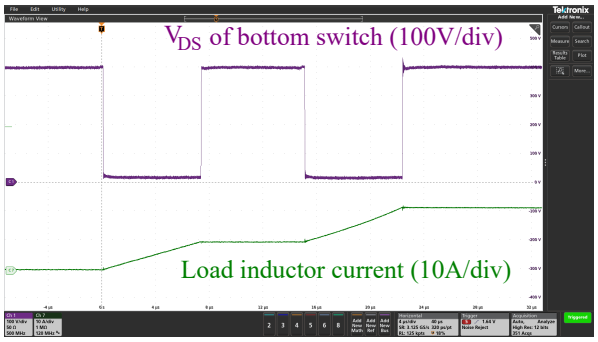


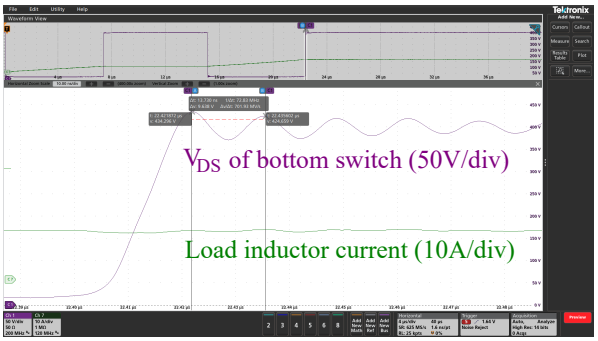
Fig. 13. Hardware setup for double pulse test of device under test (DUT).

decoupling capacitor. The Tektronix MS058 500 MHz high-bandwidth oscilloscope is used in performing this experiment. Also, the Tektronix IsoVu isolated 500 MHz TIVP05 probe with the ± 2.5 kV TIVPWS probe tip is used in capturing the high-frequency oscillations.

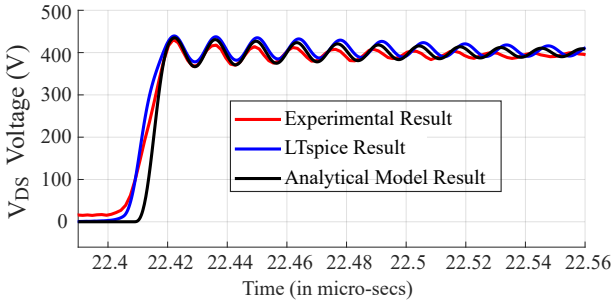
In Fig. 14 (a), the oscilloscope waveform of the double pulse test at 400 V and a load inductor current of up to 20 A is shown. This experimental data is extracted from the oscilloscope and superimposed with the results from both the LTspice simulation and the analytical model as shown in Fig. 14 (b). The superimposed experimental, LTspice and analytical waveforms from Fig. 14 (b) show a similar response in the V_{DS} voltage behavior. The voltage overshoot observed across all three waveforms is approximately 435 V. The oscillations observed across all three waveforms occurs around 73 MHz approximately. Additionally, all three waveforms take approximately 200 ns to decay to a steady state value. Based on the similarities observed across all three waveforms, the proposed Thevenin analytical model is validated. Hence, the Thevenin-based model is an effective method for predicting the response of the V_{DS} voltage across a MOSFET undergoing a hard turn-off transition. There are some minor differences in the three waveforms shown in Fig. 14 (b). The V_{DS} voltage from the analytical model has a steady state value of 400 V whereas the experimental and LTspice simulation both have a steady state voltage of 405 V. This difference is due to the voltage drop across the body diode during its conduction. Furthermore, the slew rates for all the three waveforms are different. This is attributed to the non-linear behavior associated with the MOSFET during the switching transition.



(a)



(b)



(c)

Fig. 14. The validation of the proposed analytical model: (a) experimental waveform from oscilloscope, (b) zoomed-in experimental waveform and, (c) superimposing the analytical model with the experimental results and LTspice simulation.

V. Conclusion

This work presents a Thevenin-based analytical approach for modelling the commutation power loop of a power converter. The clamped-ramp function is used to model the switching transition with its slew rate. The concept of a decoupling factor is introduced. The effects of the parasitic inductances, decoupling factor and decoupling capacitor including its ESL and ESR parasitics are analyzed. Several parametric sweeps are analyzed and used to obtain recommendations regarding the sizing and placement of the decoupling capacitor. The decoupling capacitors should be placed in close proximity to the half-bridge such that the decoupling loop inductance does not exceed 10% of the overall commutation power loop. Also, the decoupling capacitor should be sized to at least 50 times larger than the C_{oss} of the switch. The proposed Thevenin-based analytical model is validated using the developed hardware prototype for SiC switches at 400 V, and 20 A.

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