Rapid Chip Reverse Engineering Using Laser, FIB, and SEM

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Microscopy and Microanalysis, **30** (Suppl 1), 2024, 660–661
https://doi.org/10.1093/mam/ozae044.314

Microscopy AND Microanalysis

Meeting-report

Rapid Chip Reverse Engineering Using Laser, FIB, and SEM

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Reverse engineering of chips enables comparison between the chip as manufactured ("as built") and its original design specifications ("as designed"). This comparison is crucial for identifying discrepancies that may arise during the fabrication process, potentially impacting the chip's performance. The GDSII file format, standing as a cornerstone in this process, encapsulates the design data essential for manufacturing and verification purposes. Extracting the GDSII from the actual chip necessitates high-resolution imaging to capture the intricate details of different chip layers, followed by sophisticated image processing techniques for segmentation and GDSII extraction.

The delayering process, critical for exposing various layers of the chip for imaging, traditionally relies on FIB. While FIB offers unparalleled resolution and accuracy, its slow processing speed significantly lengthens the reverse engineering timeline. This slow pace impacts not only reverse engineering efforts but also failure analysis, where quick identification and resolution of issues are paramount. Although alternatives like mechanical polishing and chemical etching exist, they often fall short in terms of precision, controllability, and repeatability, heavily depending on the operator's skill and experience.

Addressing these challenges, this work proposes an innovative approach that significantly accelerates the delayering process. By employing a highly controllable, automated femtosecond laser scanning beam for material removal, we introduce a method that is orders of magnitude faster than traditional FIB, with minimal thermal effects on the material. This rapid delayering technique preserves the integrity of the sample circuitry for subsequent analysis.

Our methodology leverages the precision of femtosecond laser machining to achieve high-quality delayering suitable for detailed investigation of the chip's layers. The laser serves as an efficient tool for removing material up to a depth close to the layer of interest, which can then be polished using FIB to attain a clean view for SEM imaging. This hybrid approach combines the speed of laser delayering with the precision of FIB polishing, optimizing the preparation of samples for reverse engineering and failure analysis.

To demonstrate the effectiveness of our method, we present several examples. Figure 1 showcases a staircase structure created on an AFRL chip, delayered to varying depths using the laser technique. This demonstrates the laser's capability for precise material removal across different layers. Figure 2 illustrates the subsequent FIB polishing on a metal layer, highlighting the method's ability to reveal deep layers with clarity necessary for SEM imaging. Moreover, we showcase the potential of the laser technique to expose structures cleanly without FIB, after optimizing the parameters, further emphasizing the method's efficiency and precision.

This advanced delayering methodology not only addresses the speed limitations of traditional FIB but also introduces a level of precision and control previously unattainable with mechanical or chemical etching methods. By reducing the time and complexity associated with chip reverse engineering and failure analysis, our approach facilitates quicker insights into manufacturing discrepancies and potential failures, enhancing the overall reliability and performance of microelectronic components [3].

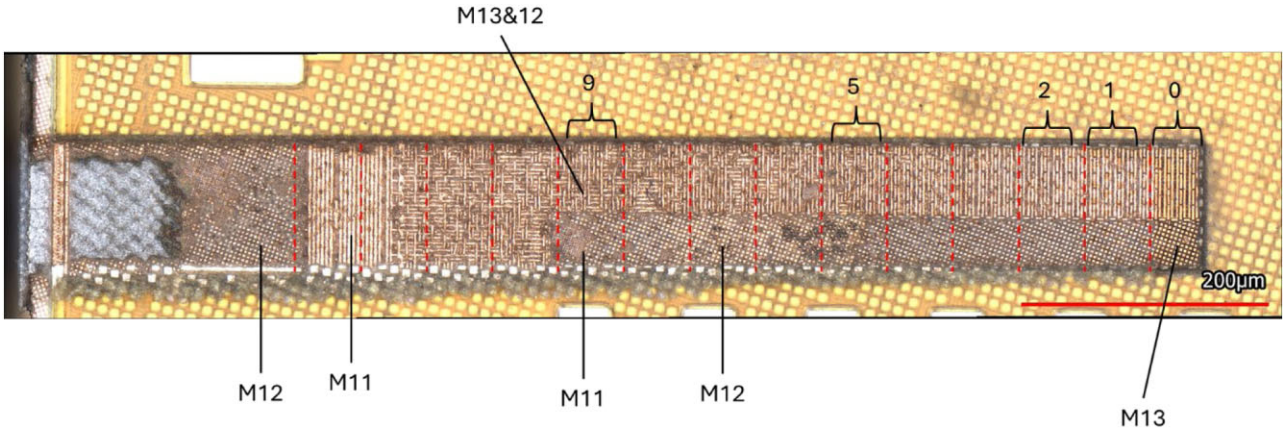

Fig. 1. A staircase structure created on an AFRL chip, delayered to varying depths using the laser technique

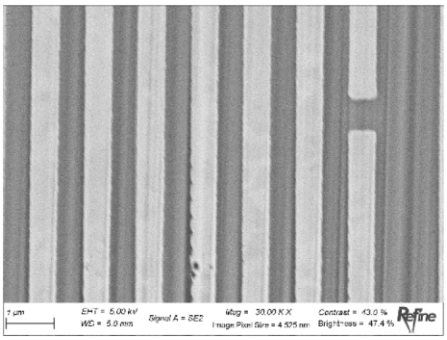

Fig. 2. Subsequent FIB polishing on a metal layer, highlighting the method's ability to reveal deep layers with clarity necessary for SEM imaging

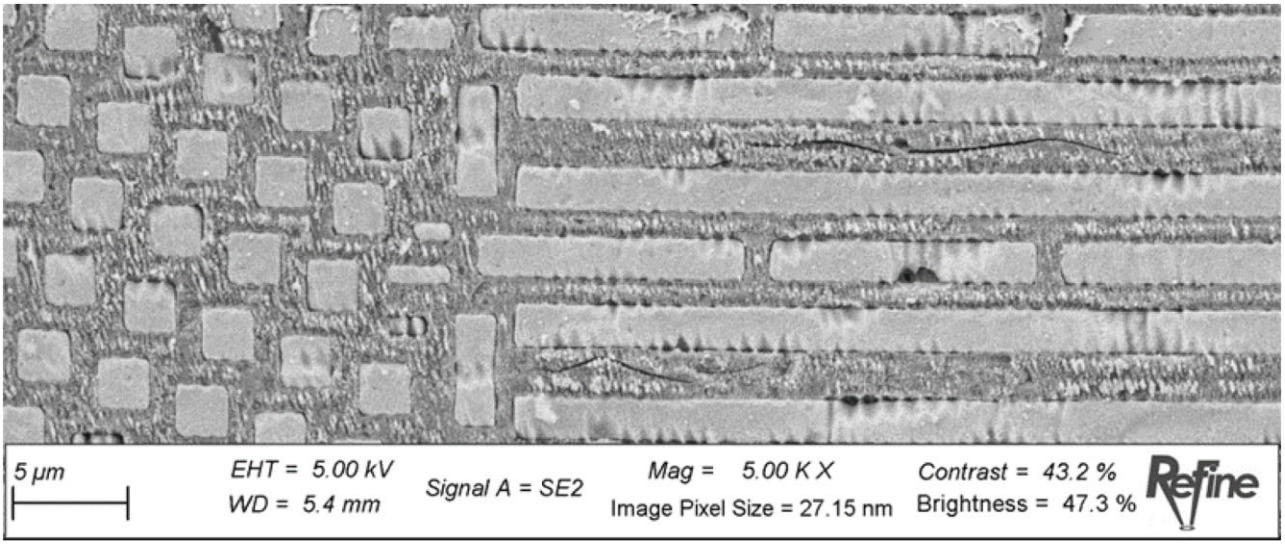

Fig. 3. Laser-only delayering, exposing a buried metal layer

References

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3. MM and HC are co-first authors.