

A 12 V Compliant Multichannel Dual Mode Neural Stimulator With 0.004% Charge Mismatch and a $4 \times V_{DD}$ Tolerant On-Chip Discharge Switch in Low-Voltage CMOS

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Abstract—This letter presents a 12 V-compliant 4-channel neural stimulator fabricated in a low-voltage bulk CMOS process. Arrays of current memory cells are used to implement anodic and cathodic current sources to generate anodic and cathodic current ratios that are robust to process-voltage-temperature variations. A novel, fully integrated discharge switch is presented that tolerates an output voltage up to $4 \times V_{DD}$, which is the highest reported for low-voltage bulk CMOS monopolar stimulators. The proposed neural stimulator can operate in both constant current mode (CCM) with a $1 \mu\text{A}$ – 1.2 mA output current range and constant voltage mode (CVM) with a 1–11 V output voltage range. The output waveform is fully programmable, including cathodic and anodic amplitudes and ratios designed to have excellent charge balancing with only 0.004% charge mismatch.

Index Terms—CMOS, constant current mode (CCM), constant voltage mode (CVM), discharge switch, high-voltage, neural stimulator.

I. INTRODUCTION

Neural stimulation is widely used in various clinical treatments, as shown in Fig. 1 (top left), including targeted stimulation for deep brain, epilepsy, cochlear, and retinal applications [1], [2], [3]. Each application has unique stimulation requirements, such as different stimulation modalities (current versus voltage stimulation), output current/voltage range, and stimulation waveform characteristics. A versatile neural stimulator that can be used across many different applications could significantly reduce the cost and complexity compared to specialized stimulators with narrow operating ranges each designed for a single application.

Standard, low-voltage CMOS processes are desirable due to low mass production costs and high levels of low-voltage digital and high-voltage analog integration. The CMOS bipolar stimulator topology using an H-bridge has been widely adopted for delivering biphasic pulses to neural tissue since it can achieve acceptable charge balancing performance and a high differential output voltage [4]. However, bipolar stimulators require two separate electrodes per working electrode plus an additional ground electrode per channel, which complicates implantation when the number of channels increases. A monopolar approach, in which a common return node is used for all the stimulation electrodes requiring only a single reference pad on the chip, is therefore preferred, but prior works suffer from several limitations, such as being limited to a fixed 1:1 ratio between anodic current (I_{CAT}) and cathodic current (I_{ANO}) [1] or

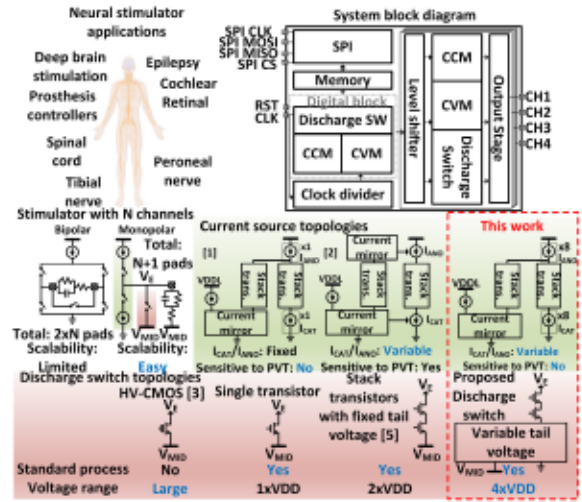


Fig. 1. Overview of neural stimulator applications (top left), system block diagram of the proposed neural stimulator (top right), and neural stimulator topologies (bottom).

allowing arbitrary ratios but being susceptible to process-voltage-temperature (PVT) variations [2]. Additionally, previous discharge switch topologies either limit the maximum output voltage range to $2 \times V_{DD}$ [5] or achieve large output voltage by using a nonstandard, high-voltage process [3]. To address these issues, this letter proposes a neural stimulator in a standard low-voltage 180 nm bulk-CMOS process that introduces a current sampling scheme adopting arrays of current memory cells to generate variable I_{CAT}/I_{ANO} ratios robust to PVT variations and a fully integrated on-chip $4 \times V_{DD}$ voltage-compliant passive discharge switch with variable tail voltage. To our knowledge, the proposed chip achieves the highest reported output voltage range for monopolar stimulators implemented in standard, low-voltage CMOS.

The structure of this letter is as follows. Section II presents the operation of the proposed high-voltage stimulator in both constant current mode (CCM) and constant voltage mode (CVM). Section III explains the operation of the proposed $4 \times V_{DD}$ tolerant discharge switch. Finally, the measurement and experimental results are reported in Section IV.

II. PROPOSED HIGH-VOLTAGE NEURAL STIMULATOR

The system block diagram of the proposed stimulator IC is shown in Fig. 1 (top right). The digital block uses a 20-MHz clock to control the finite-state-machine (FSM) of the discharge switch and a divided down 1 MHz clock to control the FSM responsible for producing CCM and CVM waveforms. The chip is configured by sending an 832-bit sequence through the SPI interface, which is stored

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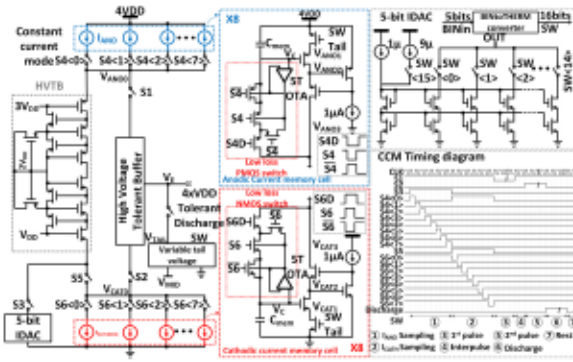


Fig. 2. Schematic of the stimulator in CCM (left), proposed current memory unit cells with low loss switch (middle), 5-bit IDAC (top right), and CCM timing diagram (bottom right).

in on-chip shift registers and controls all the stimulation parameters. Every aspect of the stimulation waveform is programmable, including stimulation mode (CCM or CVM), pulse waveform amplitudes and widths, cathodic/anodic current or voltage ratio, stimulation order (cathodic or anodic stimulation first), stimulation pulse time, interpulse delay time, discharge time, and total number of stimulation cycles. The proposed chip can thus be used for applications with vastly different specifications and requirements by programming the parameters accordingly. The output control signals from the digital block go through level shifters that step the voltage level up from 1.8 V to 3 ($1 \times V_{DD}$), 6 ($2 \times V_{DD}$), 9 ($3 \times V_{DD}$), or 12 V ($4 \times V_{DD}$) for controlling switches in the analog circuitry.

Fig. 2 (left) shows a schematic for the CCM block. In CCM, there are six operating phases: 1) current sampling which includes anodic current sampling and cathodic current sampling; 2) first stimulation pulse; 3) interpulse; 4) second stimulation pulse; 5) discharge; and 6) rest. In the current sampling phase, a current from a 5-bit IDAC (Fig. 2, top right) flows through switch S3 via a high voltage tolerant buffer (HVTB) and is sampled by the anodic current memory cells as in [4]. Subsequently, the current from the anodic current memory cell flows through the HVTB and is sampled by the cathodic current memory cell. The anodic and cathodic current ratio can be programmed between 1:1 and 1:8 by choosing how many current memory unit cells to enable on the anodic and cathodic sides during the current sampling phase. This scheme guarantees that the ratio between the anodic and cathodic currents is robust to PVT variations. The order of the anodic and cathodic pulses is determined by turning switch S1 on first and switch S2 on second for anodic first or vice versa for cathodic first. The current memory cell utilizes the ultralow leakage switch design introduced in [8] to maintain a constant current for an extended period of time without drift. The simulated leakage current of the low-leakage switch is 4fA, which is $250\times$ less than the 1pA leakage current of a conventional nMOS-only (or pMOS-only) switch of the same size. The proposed stimulator additionally adopts several techniques to minimize spikes generated due to the turn-on transients of switches S1 and S2, such as tail switching and slew rate control of the gate voltages of S1 and S2. The tail switches are turned on one cycle after the main switches S1 and S2 are enabled to charge (or discharge) the intermediate nodes (V_{CAT0-3} , V_{ANO0-3}) between SW Tail and main switches. This minimizes the charge sharing between intermediate nodes to the output and avoids spikes at the output. Slew rate control reduces charge coupled from gates of switching transistors through parasitic capacitance C_{GS} to output nodes.

Fig. 3 (left) shows the schematic for CVM. In CVM, there are five operating phases: 1) first stimulation pulse; 2) interpulse; 3) second

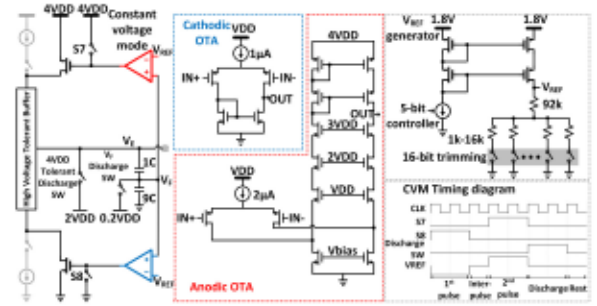


Fig. 3. Schematic of the stimulator in CVM (left), cathodic and anodic OTAs (middle), the voltage reference generator (top right), and CVM timing diagram (bottom right).

stimulation pulse; 4) discharge; and 5) rest. During each stimulation phase, the output electrode voltage (V_E) is divided by 10 by a capacitive voltage divider. The divided voltage V_F is fed back to a cathodic OTA and an anodic OTA and then compared to reference voltages (V_{REF}) to regulate V_E via negative feedback loops. V_{REF} can be set from 0.1 to 1.1 V and is generated using an on-chip VDAC shown in Fig. 3 (top right) by mirroring a current ranging from 1 to 11 μ A from a 5-bit IDAC and passing it through a resistive network with a total resistance of 100k Ω . The resistive network has 16-bit digital trimming control to cover up to 15% variation based on Monte Carlo simulations for manual calibration.

III. PROPOSED $4 \times V_{DD}$ TOLERANT DISCHARGE SWITCH

Discharge switches are indispensable components in stimulators even when both charge-balancing mechanisms and active charge-balance techniques are employed. A high-voltage discharge switch was implemented in a high-voltage process in [3]. A high voltage tolerant discharge switch with a stack of two transistors was presented in [5] in a low-voltage CMOS process; however, this switch used a fixed tail voltage at V_{MID} , which limited the output voltage range of V_E to only $2 \times V_{DD}$. The proposed high voltage tolerant discharge switch also uses a stack of two transistors but leverages a variable tail voltage to allow V_E to achieve a range up to $4 \times V_{DD}$.

Fig. 4 (top left) shows the schematic of the proposed $4 \times V_{DD}$ -compliant discharge current switch for low-voltage CMOS processes. The discharge switch consists of two nMOS devices connected in series and has one terminal connected to V_E and the other connected to V_{TAIL} . The bulks of the two nMOS devices are connected to dynamic body biasing circuits to avoid leakage current when V_E varies below or above V_{TAIL} . V_{TAIL} is set to 0 V when $V_E < 2V_{DD}$ and $2V_{DD}$ when $V_E > 2V_{DD}$. By setting the gate voltages of SW1, SW2, and V_{TAIL} properly according to the timing diagram in Fig. 4 (top middle), the proposed switch can safely withstand a voltage swing up to $4 \times V_{DD}$ at V_E . The gate voltage SW1 (GV_{SW1}) generator uses a 3-level stack of transistors to generate four different voltage levels: 0, $1 \times V_{DD}$, $2 \times V_{DD}$, and $3 \times V_{DD}$ by using 7 voltage control signals from V0 to V6 to switch ON/OFF 14 switches. The GV_{SW1} generator requires four main states for four different voltage levels and six intermediate transition states to move between the four main states as described in Fig. 4 (middle). The gate voltage SW2 (GV_{SW2}) generator uses a 2-level stack of transistors to generate three voltage levels: $1 \times V_{DD}$, $2 \times V_{DD}$, and $3 \times V_{DD}$. The tail voltage generator has the same circuit as the GV_{SW2} generator but with different gate bias voltages and produces three voltage levels: 0, $1 \times V_{DD}$, and $2 \times V_{DD}$. Gate control voltages V0–V10 are generated from the digital control block and go through level shifters to provide the required voltage ranges for control voltages.

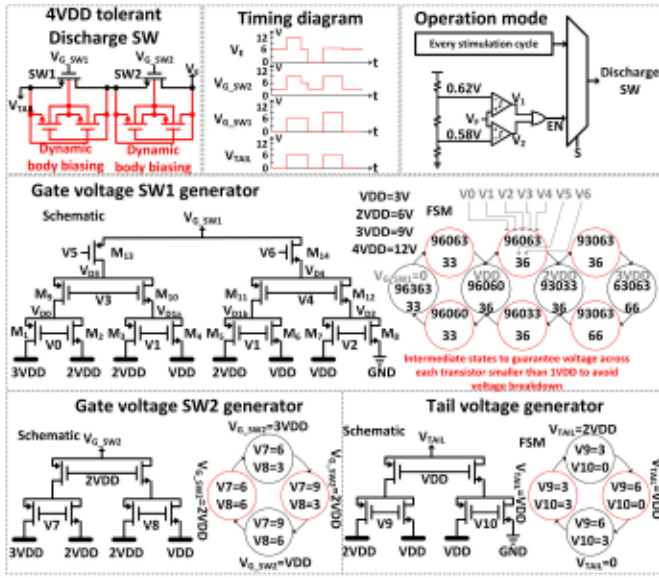


Fig. 4. Schematics of the proposed $4 \times V_{DD}$ tolerant discharge switch (top left), gate voltage SW1 generator, gate voltage SW2 generator, tail voltage generator, and timing diagram of discharge switch.

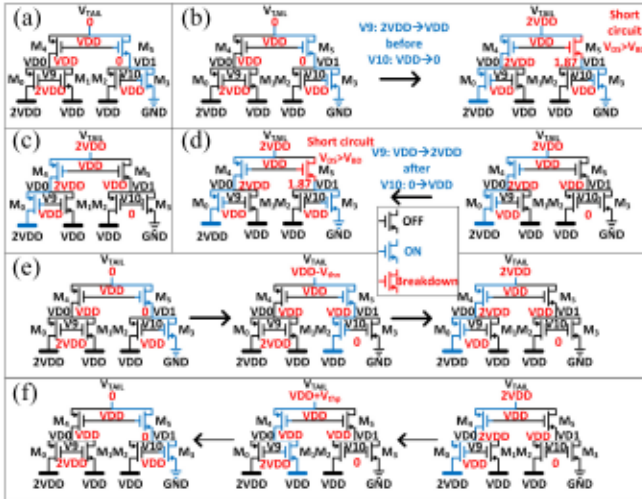


Fig. 5. Operation of SW TAIL generator with (a) $V_{TAIL} = 0$, (b) $V_{TAIL} = 6$, (c) direct transition from 0 to $2 \times V_{DD}$, (d) direct transition from $2 \times V_{DD}$ to 0, (e) transition with intermediate states from 0 to $2 \times V_{DD}$, and (f) from $2 \times V_{DD}$ to 0.

Fig. 5 shows the operation of the V_{TAIL} generator and the voltage levels associated with each node in the circuit. The body terminals of all transistors are connected to source terminals. Deep N-well is utilized for all nMOS transistors with source terminals connected to a voltage potential other than 0 V. The impedance of the M_0 – M_4 branch was designed to be much smaller than that of the M_5 – M_3 branch because the M_0 – M_4 branch serves as the main discharge current path for the electrodes. In the steady state, $V_{TAIL} = 0$ when $V_9 = 2 \times V_{DD}$ and $V10 = 1 \times V_{DD}$ as shown in Fig. 5(a), and $V_{TAIL} = 2 \times V_{DD}$ when $V_9 = 1 \times V_{DD}$ and $V10 = 0$ as shown in Fig. 5(b). During the transient, when V_{TAIL} changes from 0 to $2 \times V_{DD}$, if V_9 decreases from $2 \times V_{DD}$ to $1 \times V_{DD}$ before $V10$ decreases from $1 \times V_{DD}$ to 0, V_{TAIL} is charged to $2 \times V_{DD}$ while $VD1$ is only charged to 1.87 V. This causes a short circuit from $2 \times V_{DD}$ supply to GND and leads to an overvoltage condition for the M_5 transistor. A possible remedy is to add a delay line to force V_9 to change from $2 \times V_{DD}$

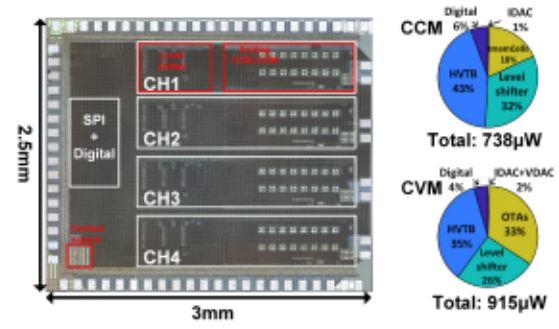


Fig. 6. Die micrograph (left) and power breakdowns (right) of the proposed stimulator chip in CCM with a stimulation current of $1 \mu A$ and in CVM with a stimulation voltage of $\pm 1V$ and a repetition rate of 1kHz.

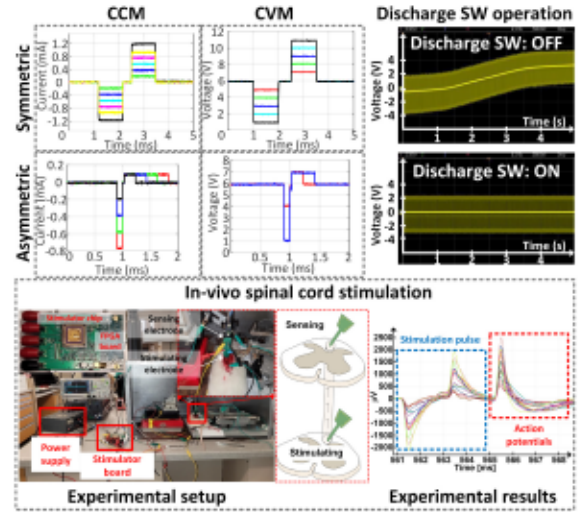


Fig. 7. Measured output waveform (top left), operation of the proposed discharge switch (top right), in-vivo experimental setup (bottom left), and experimental results (bottom right).

to $1 \times V_{DD}$ after $V10$ changes from $1 \times V_{DD}$ to 0. However, this intentional delay would introduce another issue when V_{TAIL} instead decreases from $2 \times V_{DD}$ to 0. In this scenario, when V_{TAIL} changes from $2 \times V_{DD}$ to 0, $VD1$ would discharge to 1.87 V while V_{TAIL} is still at $2 \times V_{DD}$ because V_9 would increase from $1 \times V_{DD}$ to $2 \times V_{DD}$ after $V10$ increases from 0 to $1 \times V_{DD}$. This again would cause a short circuit between $2 \times V_{DD}$ supply and GND, leading to overvoltage on M_5 . Therefore, different intermediate states are required for both V_{TAIL} voltage transitions. For the case when V_{TAIL} increases from 0 V to $2 \times V_{DD}$, an intermediate state is added to change $V10$ from $1 \times V_{DD}$ to 0 V first. This turns off M_3 and turns on M_2 , charging $VD1$ to $1 \times V_{DD}$ and leading to V_{TAIL} reaching $1 \times V_{DD} - V_{thn}$. Following this, V_9 is decreased from $2 \times V_{DD}$ to $1 \times V_{DD}$. $VD0$ is charged to $2 \times V_{DD}$ through M_0 , and V_{TAIL} is charged to $2 \times V_{DD}$. Similarly, for the case when V_{TAIL} decreases from $2 \times V_{DD}$ to 0, an intermediate state is added to change V_9 from $1 \times V_{DD}$ to $2 \times V_{DD}$ first. This turns on M_1 and turns off M_0 , discharging $VD0$ to $1 \times V_{DD}$ and causing V_{TAIL} to discharge to $1 \times V_{DD} + V_{thp}$. $V10$ is next increased from 0 to $1 \times V_{DD}$, causing $VD1$ to discharge to 0 and V_{TAIL} to reach 0. These intermediate states guarantee that all transistors in the V_{TAIL} generator operate in a safe voltage range and avoid any short circuit conditions. Operation of the GV_{SW1} generator and the GV_{SW2} generator operates in the same principle as the V_{TAIL} generator.

TABLE I
COMPARISON TABLE WITH PRIOR STATE OF THE ART HIGH VOLTAGE
STIMULATORS IN LOW VOLTAGE CMOS

	JSSC 2021 [5]	CICC 2022 [6]	TBioCAS 2023 [7]	This work
Technology	0.18 μ m LV CMOS 1.8/3.3	65nm LV CMOS 0.85/1.2	0.18 μ m LV CMOS 1.8/3.3	0.18 μ m LV CMOS 1.8/3.3
Stimulus mode	CCM	CCM	CCM/CVM	CCM/CVM
Stimulus configuration	Monopolar	Bipolar	Monopolar/Bipolar	Monopolar
# Stimulus channel	8	4	4	4
Stimulation current	100 μ A $\rightarrow$ 1.2mA	30 μ A $\rightarrow$ 440 μ A	3.6mA	1 μ A $\rightarrow$ 1.2mA
Stimulation voltage	N/A	N/A	3.6V	1V $\rightarrow$ 11V
Voltage supply	$\pm$ 6V	$\pm$ 2.4V	$\pm$ 6V	12V
Charge balance	N/R	N/R	$\leq$ 0.3%	0.004%
Voltage-compliance of discharge switch	2 $\times V_{DD}$ (7.2V)	1 $\times V_{DD}$ (1.2V)	2 $\times V_{DD}$ (7.2V)	4 $\times V_{DD}$ (12V)
Power consumption	8 mW	60 μ W	N/R	738 μ W(CCM) 915 μ W(CVM)
Chip area	4.2mm ²	4mm ²	1.16mm ²	7.5mm ²

N/A: Not available, N/R: Not reported

IV. CONCLUSION

The proposed neural stimulator is fabricated in a standard low-voltage 180 nm bulk-CMOS process, occupying $3 \times 2.5 \text{ mm}^2$ area for four independent channels. Supplies are produced off-chip, although they could be generated on-chip using charge pumps in the future. The die micrograph of the neural stimulator is shown in Fig. 6. The stimulator is fully programmable and can generate biphasic charge-balanced symmetric and asymmetric waveforms in both CCM and CVM with different amplitudes (1 μ A to 1.2 mA in CCM, 1–11 V in CVM), anodic and cathodic current/voltage ratios, and cycle timings (Fig. 7, top left). As shown in Fig. 7 (top right), without activating the switch, for a biphasic symmetric current stimulation with a 1000 μ s repetition rate and 100 μ s wide stimulation pulses, the output voltage across the electrode experiences minimal drift for up to 1 s before V_E noticeably deviates due to the well-matched cathodic and anodic currents. When activating the discharge switch, the output voltage waveform exhibits no noticeable drift regardless of duration. The charge balancing of the proposed neural stimulator is also validated with a charge mismatch measurement. The charge balance is calculated based on the difference of the voltage across the electrode to V_{MID} at the rest time divided by the number of stimulation cycles (500 cycles) with a load of $1\text{k}\Omega + (100\text{nF} \parallel 1\text{M}\Omega)$. The charge mismatch of the proposed neural stimulator is less than 0.5% across PVT variations for a standard deviation of 3 sigma based on extensive Monte Carlo simulations with a voltage supply range from 11.2 to 12.8 V, and temperature range from 0 to 80°C. The stimulator shows very good charge balance performance with only 0.004% charge mismatch. The power consumption and breakdown for each mode are shown in Fig. 6. The neural stimulator consumes 738 μ W in CCM and 915 μ W in CVM.

In-vivo animal experiments with the proposed stimulator were carried out for spinal cord stimulation in rats. The experimental setup is shown in Fig. 7 (bottom left). A stimulating probe was placed in the dorsal white matter at level L4 with the electrode array facing rostrally, while a sensing electrode array of the same size was implanted at the same cross sectional location of the dorsal spinal cord at level L2 facing caudally. A custom-designed clamp was 3-D printed to hold and align both probes. The stimulator output was connected to a stimulator electrode, while an INTAN recording chip was connected to the sensing electrodes. The stimulator sent continuous stimulation pulses in CCM with a repetition rate of 10 Hz and 10 μ A amplitude pulses and successfully triggered action potentials, shown in Fig. 7 (bottom right), demonstrating the viability of the proposed stimulator to be used in a practical in-vivo setting. Table I shows a performance comparison table against other recent work. To the best of the authors' knowledge, this is the first monopolar neural stimulator to feature an on-chip discharge switch with the highest reported voltage compliance of up to $4 \times V_{DD}$ in a standard low-voltage CMOS process.

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