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Design of a Low Parasitic Inductance Paralleled Module for 8.56 kV $\beta-Ga_2O_3$ MOSFET

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***Abstract*—Based on the parameters of a lab sample $\beta-Ga_2O_3$ MOSFET die, a laminated structure is proposed to reduce the parasitic inductance of a two-parallel MOSFET module. The inductance of the proposed laminated module is reduced to half that of the non-laminated module. Subsequently, a laminated double pulse test (DPT) circuit board with a symmetric structure is designed to reduce the PCB inductance and improve the performance of current sharing. Then, PCB thermal vias and multi-objective optimized heat sink are used in four-parallel Ga_2O_3 MOSFET dies to improve heat dissipation efficiency. The improved heat sink design is validated through steady-state thermal simulation, showing a maximum temperature reduction of 12.5 °C for the MOSFETs, which is 15.2% lower compared to the model without thermal vias and optimized heat sink.**

I. Introduction

With recent developments in wide bandgap (WBG) power devices, power electronics systems have achieved both high efficiency and high power density [1]. WBG devices such as SiC and GaN devices offer significantly higher breakdown voltages while maintaining the same size and on-resistance compared to silicon devices. Recently, Ga_2O_3 MOSFETs have emerged as a promising ultra-WBG semiconductor due to their higher breakdown field and more desirable material properties compared to SiC and GaN, making Ga_2O_3 a highly active area of research for future applications [2]–[4]. Ga_2O_3 MOSFETs have shown their advantages of high current density [5], high breakdown voltage [6], and low ohmic contact resistance [7]. Simulation results [8] show that Ga_2O_3 MOSFETs exhibit lower conduction losses but higher switching losses compared to commercial SiC MOSFETs. However, the thermal conductivity of Ga_2O_3, which ranges from 0.1 to 0.3 W/(cm·K), can cause severe self-heating effects, limiting the electrical performance of devices utilizing a native Ga_2O_3 substrate [9], [10]. On the other hand, achieving low on-resistance (R_{on}) while maintaining high drain current (I_d) is critical for enhancing power device performance. This challenge also applies to normally-off Ga_2O_3 devices, where the drain current is currently very low, often accompanied by a large R_{on}, which remains a problem that needs to be addressed for the material's effectiveness in high-power applications [11].

At this stage, achieving high current with a single Ga_2O_3 MOSFET die remains challenging due to technological and equipment limitations. To meet the demands of high power applications, multiple MOSFETs connected in parallel can be used to high-current operation. To ensure proper current sharing, device screening is essential. A method that considers the parameters such as V_{th}, g_{fs}, R_{on}, and V_{SD}, has been proposed and proven effective for parallel device current sharing [12]. In addition to device screening, a symmetrical low-inductance design is crucial for the reliable operation of parallel modules. An optimization method involving adjustments to the position and number of bonding wires has been used [12]. Another approach is the common source inductance compensation technique, proposed for SiC MOSFETs in parallel operations to mitigate dynamic current imbalance [13]. However, this method increases the complexity of the layout and wiring in the PCB board. To simplify bonding wires and reduce inductance, a sandwiched structure has been proposed for bonding the drain and source terminals [14]. While this method effectively reduces parasitic inductance, it increases capacitance, which can lead to voltage overshoot. Additionally, it is only suitable for vertical MOSFET dies. A PCB-embedded dual-side cooling module has also been introduced to minimize thermal resistance in vertical MOSFETs [15]. To address the low thermal conductivity of the lateral Ga_2O_3 MOSFETs, the thermal resistance can be reduced by introducing thermal vias in PCBs, with a decreased pitch size between two vias [16], [17].

In this paper, based on the lateral β-Ga_2O_3 MOSFET die discussed in [4], a laminated PCB with reduced inductance and symmetric structure by increasing coupling area of wiring and changing the position of outlet is designed, which can help to achieve equal current sharing for parallel MOSFETs. The performance of the proposed structure is verified through LTspice simulations. Additionally, the heat dissipation efficiency of the four parallel MOSFET dies is improved through the incorporation of PCB thermal vias and an optimized heat sink design. The heat dissipation efficiency of the module is verified by using Workbench steady-state thermal analysis. The rest of this paper is organized as follows: In Section II, the proposed PCB-embedded laminated module and parasitic inductance are presented, and the performance of current sharing in DPT circuit is verified through LTspice simulation; In Section III, PCB thermal vias and a heat sink optimized by using multi-objective techniques for four parallel MOSFETs

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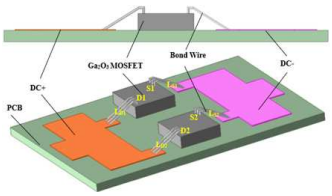

Fig. 1. Non-laminated module.

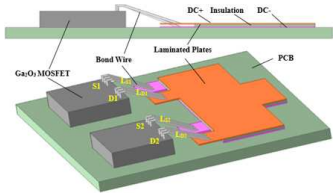

Fig. 2. Laminated module.

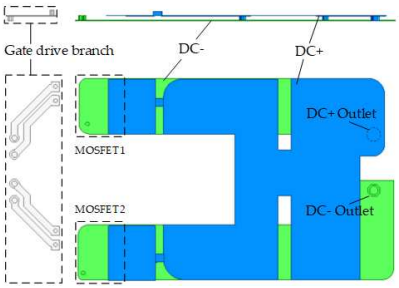

Fig. 3. The Q3D simulation model.

are introduced, and the results are validated through steady-state thermal analysis in Workbench. Finally, the conclusions are provided in Section IV.

II. The Laminated PCB Layout Design

The β-Ga_2O_3 die examined in this study operates at a low current level (less than 0.5 A), limiting its suitability for high-power applications. To address this limitation, two Ga_2O_3 dies are connected in parallel to increase the current capacity. However, the parallel MOSFETs introduce challenges such as parasitic inductance and imbalanced current sharing. In this paper, a laminated, symmetric board design is proposed to solve parasitic inductance and enhance current sharing.

A. Laminated module and parasitic inductance calculation

To reduce the parasitic inductance in the two-parallel β-Ga_2O_3 MOSFET dies, a laminated structure module is designed. For a non-laminated module shown in Fig. 1, DC+ and DC- are distributed on both sides of the MOSFET. The current flows in from one side and out from another side and there is no direct coupling between DC+ and DC-. In this work, the proposed laminated module is to stack DC+ and DC- wiring together as shown in Fig .2. The upper copper layer is DC+, and the lower copper layer is DC-, DC+ and DC- are separated by PCB interlayer insulation. To minimize parasitic inductance, the distance between DC+ and DC- should be as small as possible while maintaining adequate insulation. To verify the advantage of the proposed laminated structure, the parasitic inductance comparison is conducted using Q3D analysis at a 80 kHz operation frequency.

From the Q3D simulation analysis, the inductance of the laminated module is 2.1 nH and the inductance of the non-laminated module is 4.01 nH. The inductance for the laminated module is only half that of the non-laminated module. It is

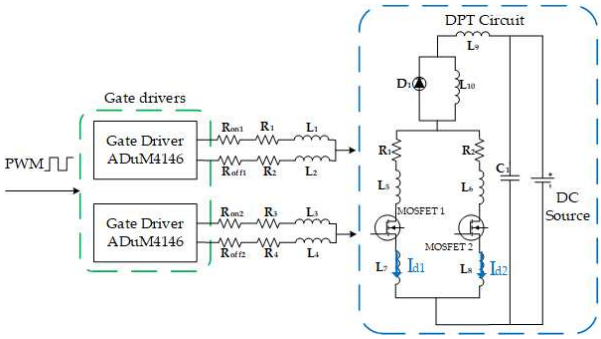

Fig. 4. The diagram of DPT circuit for two-parallel MOSFETs.

TABLE I
Inductance values in asymmetric model and proposed model

Inductance	Asymmetric model /nH	Proposed model/nH	Proportion
L_1	6	6	–
L_2	6.1	6.1	–
L_3	5.3	5.3	–
L_4	5.3	5.3	–
L_5	9.6	8.5	11.5%
L_6	9.7	8.4	13.4%
L_7	26.1	21.0	19.5%
L_8	22.2	20.2	9%
L_9	3.16	2.51	20.6%

evident that the laminated layout can significantly reduce the inductance of two-parallel MOSFETs.

B. The layout design for laminated PCB

To achieve equal current sharing for the two paralleled MOSFET dies in DPT circuit, a new model with symmetric laminated PCB layout is proposed. The designed PCB board consists of two layers, DC+ is on the upper layer, DC- is on the bottom layer, and DC+ and DC- are isolated from each other by the FR4 board. In this PCB layout, the inductance parameters in each branch are reduced by increasing the coupling area between DC+ and DC-. To achieve balanced current sharing in the DPT circuit, DC+ and DC- are arranged in a symmetrical structure, ensuring minimal inductance differences between the branches. The Q3D simulation model of the proposed PCB board is shown in Fig. 3. Through Q3D simulation, the inductance value of each part of the circuit shown in Fig. 4 can be obtained. To verify the advantage of the proposed design, the inductance of an asymmetric model without coupling wiring is also calculated. The inductance parameters are shown in Table I. From Table I, the parasitic inductance of each part of the circuit is reduced by $10\%-20\%$ with the proposed PCB board. The inductance difference between L_5 and L_6 is only 1.2%, and the inductance difference between L_7 and L_8 is reduced from 16.1% to 3.9% for the proposed model. Since the resistance R_1, R_2, R_3 and R_4 of the driving branch is very small (less than 1 mΩ), the resistance in drive circuit can be ignored. The inductance differences between the two drive branches(L_1 and L_3, L_2 and L_4) are 11%.

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TABLE II
THE PARAMETERS FOR 8.56KV Ga_2O_3 MOSFET [4]

V_{DS} [kV]	I_D [mA]	V_{GS} [V]	V_{th} [V]	R_{on} [Ω]	D [%]	T_{rise} [ns]	T_{fall} [ns]	f_{sw} [kHz]	Q_g [nC]
6	13.6	-25/15	-19	897	50	30	50	80	40

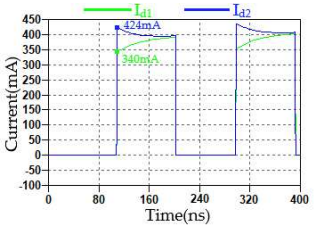

Fig. 5. The currents of the two branches for asymmetric model

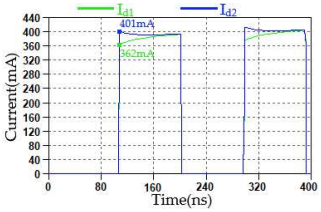

Fig. 6. The currents of the two branches for proposed model

C. Analysis of current sharing in DPT circuit

The proposed board structure's current sharing performance is tested through LTspice simulation. The DPT circuit with gate driver in Fig. 4 is built in LTspice. The gate drive used in the simulation is Analog Devices ADUM4146. The inductance parameters with asymmetric structure and proposed model are used for the current sharing performance comparison. From the results in Figs. 5 and 6, it can be seen that with the laminated symmetric structure, the transient current difference between the two MOSFETs is 10.2%, which is lower than that of using asymmetric structure (21.9%).

III. DESIGN OF HEAT SINK FOR FOUR-PARALLEL MOSFET DIES

Heat dissipation is another challenge of of multiple Ga_2O_3 MOSFET dies in high power applications. To improve the heat dissipation efficiency, the thermal vias on the PCB and optimized heat sink are used to cool down the module from the application level in this paper. It is necessary to calculate the loss of the heat source and determine the thermal conductivity and convection coefficient of each part before calculating the temperature field distribution of the model. The MOSFETs losses can be divided into conduction loss P_{on}, switching loss P_{sw}, and gate loss P_{gate}. The basic parameters for a lab sample 8.56 kV Ga_2O_3 MOSFET die are presented in Table II [4], the losses of these three parts can be obtained by the following equations:

$$P_{on} = I_D^2 \times R_{on} \times D \tag{1}$$

$$P_{sw} = V_{DS} \times I_D \times (t_{Rise} + t_{Fall}) \times f_{sw} \tag{2}$$

$$P_{gate} = Q_g \times V_{GS} \times f_{sw}. \tag{3}$$

For the lab sample Ga_2O_3 MOSFET, using (1)-(3), the conduction loss P_{on} is 0.083 W, the switching loss P_{sw} is 0.523 W, the gate loss P_{gate} is 0.064 W. It can be seen that most of the loss comes from the switching loss of the MOSFETs.

The thermal conductivity of each part in the simulation model is shown in Table III. K_{MOS} is thermal conductivity

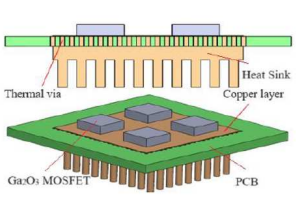

Fig. 7. The 4-parallel MOSFETs model with thermal vias.

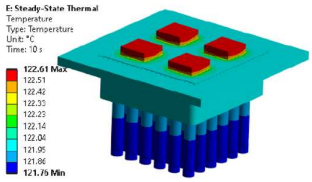

Fig. 8. Temperature distribution with thermal vias.

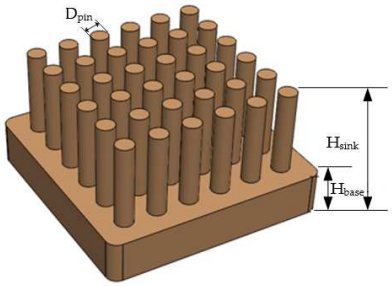

Fig. 9. The heat sink shape and optimized parameters.

for Ga_2O_3 MOSFET. K_{heatsink} and $K_{\text{copperlayer}}$ are thermal conductivity for heat sink and copper layer respectively. The thermal conductivity of the PCB board along three directions is $K_{PCB}[x/y/z]$. Since natural heat dissipation is adopted, the convective coefficient in this paper is taken as 10 W$/(\text{m}^2 * \text{K})$. The initial temperature of the model is 50 °C.

A. Design of thermal vias and thermal sink

To improve the efficiency of heat dissipation, the proposed module incorporates vias filled with copper shown in Fig. 7. The diameter of the vias is 0.5 mm. The steady-state thermal analysis is conducted to calculate the temperature field distribution using Workbench. As shown in Fig. 8, the maximum temperature in this module is 122 °C and the temperature rise of the module with thermal vias can be reduced by 7 °C compared to without the thermal vias, constituting a reduction of 9.7% in the total temperature rise. Therefore, the heat dissipation holes can significantly improve the heat dissipation efficiency of four-parallel MOSFETs.

Another design for improving the heat dissipation capacity of the four-parallel module is to use the multi-objective optimized heat sink. The parameters of the heat sink are properly chosen. As shown in Fig. 9, there are three parameters of the heat sink: the diameter of the pins D_{pin}, the total height of the heat sink H_{sink} and the height of the base H_{base}. The parameters' values are optimized using Icepak. Keeping two of the parameters unchanged, the curve of the maximum temperature of the module changing with the third parameter is shown in Fig. 10. The maximum temperature of the module increases as the diameter of the heat sink pins D_{pin} increases. The maximum temperature of the module decreases as the total height of the heat sink H_{sink} increases. The maximum temperature of the module increases as the height of the

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TABLE III
THE THERMAL CONDUCTIVITY AND THE CONVECTION COEFFICIENT OF THE MODEL

K_{MOS} [W/(m*K)]	$K_{heatsink}$ [W/(m*K)]	$K_{copperlayer}$ [W/(m*K)]	$K_{PCB}[x/y/z]$ [W/(m*K)]	h_{MOS} [W/(m^2 * K)]	$h_{heatsink}$ [W/(m^2 * K)]
27	401	401	16.5/16.5/0.25	10	10

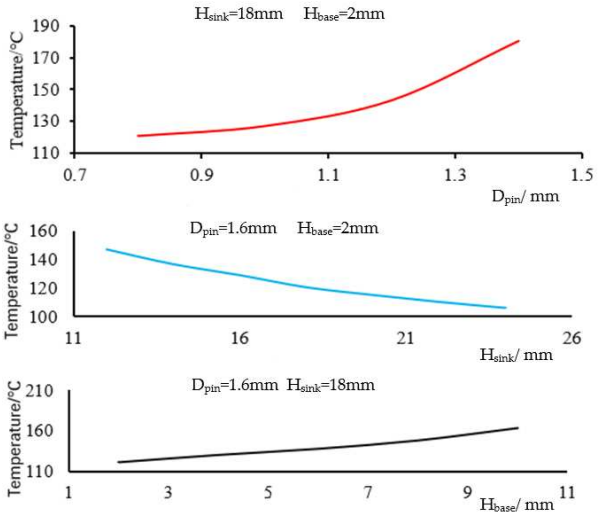

Fig. 10. The maximum temperature of model vary with D_{pin}, H_{sink}, and H_{base}.

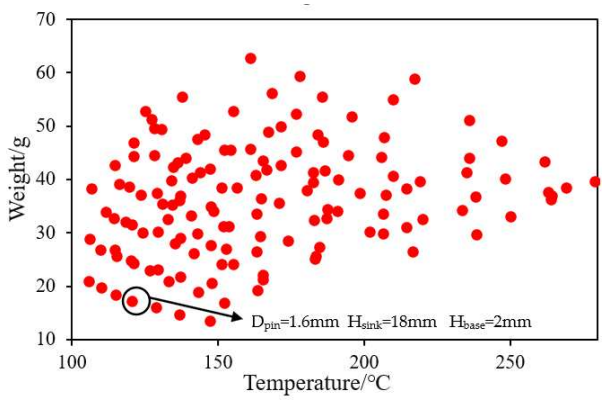

Fig. 11. Distribution diagram of multi-objective optimization results.

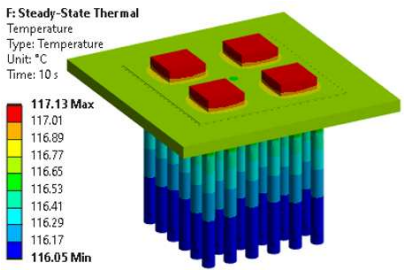

Fig. 12. Temperature distribution diagram of the optimized model.

base H_{base} increases. Under the premise of considering the mechanical strength and processing technology of the heat sink, in order to find a local optimal solution, the heat sink is analyzed using Icepak multi-objective optimization. The maximum temperature of the entire module and the weight of the heat sink are taken as the optimization targets. The three parameters D_{pin}, H_{sink} and H_{base} are parametrically scanned to obtain the point distribution diagram shown in Fig. 11. Considering the weight and volume of the heat sink under the premise of minimizing weight and the temperature rise of the model, the point marked by the black circle is selected as the local optimal solution. The local optimal solution is $D_{pin} = 1.6$ mm, $H_{sink} = 18$ mm and $H_{base} = 2$ mm. The temperature distribution of the module after optimization is shown in Fig. 12. The optimized model achieves a 5.5°C temperature reduction compared to the module with thermal vias, resulting in a 6.9% decrease in temperature rise for the four-parallel Ga_2O_3 MOSFET module.

IV. CONCLUSION

In this paper, with the laminated PCB design, the inductance of two paralleled modules is reduced to 50% compared to the non-laminated module. With the symmetric PCB layout, the equal current sharing for the paralleled MOSFETs is improved. LTspice simulation analysis proves the influence of parameter symmetry on dynamic current sharing. The temperature rise of the module with thermal vias is reduced by 7 °C compared to without thermal vias, which is a reduction of 9.7% in the total temperature rise. The heat dissipation efficiency of the heat sink was improved by parameterizing the pin diameter, length, and base height. The temperature rise of the optimized model is reduced by 5.5°C compared to the thermal vias model. Overall, these improvements result in a 15.2% reduction in temperature rise for the four-paralleled Ga_2O_3 MOSFETs dies, demonstrating the effectiveness of the heat sink design in improving thermal performance.

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