Title

Capillary Flow Printing of Submicron Carbon Nanotube Transistors

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Abstract

Printed transistors have a wide range of applications, but the limited resolution of printing techniques (10-30 μm) has been a barrier to their utility and scalability. Previous works have relied on chemical processes or tedious post-processing to realize printed submicron channel lengths, limiting their applicability. Here, we show that capillary flow printing can create as-printed submicron carbon nanotube thin-film transistors (CNT-TFTs) without chemical modification or physical manipulation post-printing. We show that the approach can be used to print conducting, semiconducting, and insulating inks on different types of substrates (silicon, Kapton, and paper), and can be used to fabricate various TFT device architectures. Printed CNT-TFTs yielded on-currents of 1.12 mA/mm when back gated on Si/SiO_2, and 490 μA/mm when side gated through ion gel on Kapton. Mechanical bending and sweep rate resilience of devices on Kapton show the wide utility of these printed devices for flexible applications.

Main text

Additive manufacturing has transformed many products through the low-cost and environmentally sustainable printing of 3D objects[1]. This has driven the exploration of printing for the electronics industry, where there is increasing attention on the environmental impact of emerging technologies[2]. Whether it is thin-film transistors (TFTs) for displays or nanoscale field-effect transistors for microprocessors, transistor fabrication processes are leading contributors to fluorinated greenhouse gas emission and resultant climate change[3,4]. Meanwhile, printed transistors have been demonstrated using eco-friendly processing and materials that are completely recyclable[3,5]. It has long been a goal to realize fully printed transistors with performance and size that are competitive with commercial devices from silicon or metal-oxide semiconductors[6].

Motivation for realizing printed transistors is not necessarily for replacing sub-10 nm, high-performance transistor technologies. There are opportunities to print backplane electronics for the display industry[7,8], transistors for the expanding Internet of Things and biomedical wearables spaces[9,10], and back-end-of-line (BEOL) devices for monolithically integrated functionality in chips[11,12]. A promising assortment of printable semiconductor inks have been formulated, including indium gallium zinc oxide (IGZO)[13], organics[14], two-dimensional materials[15,16], and carbon nanotubes (CNTs)[17,18]. CNT thin films offer high carrier mobility, chemical and mechanical robustness, and processability[19–21]. However, there remain limits in achievable dimensional scaling and performance of fully printed transistors from any semiconductor.

The smallest reliable resolution achievable with current printing techniques is around 10-30 μm using, for example, aerosol jet printing (AJP) or inkjet printing (IJP) – far larger than that required to achieve submicron channel lengths[22]. This resolution constraint manifests itself in both the linewidth of a single printed feature, as well as the gap between two printed lines, which

determine the channel length in a printed transistor. In addition, while inkjet printing offers precise liquid delivery with small ink volume requirements, it includes challenges with droplet dynamics (wetting, merging, and satellite drops)[22,23]. Similarly, AJP enables wide ink compatibility, but overspray and resolution constraints restrict the achievable feature sizes[24]. Besides these direct-write printing techniques, there are sheet or roll-to-roll approaches, such as gravure printing[25,26], that provide exceptional throughput capabilities. However, these techniques are limited to typical resolutions of 50 μm, or 2-5 μm in the most aggressively scaled cases, for conductive traces without the ability for alignment of multi-layer materials for active circuitry components such as transistors[27,28].

Techniques have been developed to sidestep the resolution constraints of printing technologies to achieve submicron dimensions for TFTs. Approaches included ink-to-ink repulsion (where ink solvent polarities cause two overlaying inks to repel from one another, yielding a micron-scale gap)[29], the use of self-assembled monolayers (which rely on the same repulsion technique to create micron-scale gaps)[30,31], post-print line-splitting[32], and dip-pen nanolithography (which is often a patterning lithography step requiring extensive chemical treatments and not a direct-write printing technique)[33,34]. While these work-arounds have enabled demonstrations of submicron gaps between conductive traces, there are challenges of repeatability due to process complexity, reliance on homogeneous chemical functionalization, and the difficulty of achieving fine control of transistor channel dimensions because of variability in line edge roughness.

In this Article, we show that a capillary flow printing (CFP) technique, derived from atomic force microscopy (AFM) technology, can provide repeatable submicron printing of CNT transistors in a simple and scalable manner without the use of cleanroom tools or environment.

The technique bypasses issues such as overspray, satellite droplets, and low throughput to enable the direct control of spacing between printed features at submicron levels. We print a variety of inks (metallic, semiconducting, and insulating) to fabricate and scale multilayer devices. In particular, we examine the effects of various gating architectures, contact geometries, post-processing conditions, and substrates on submicron CNT-TFT performance. Additionally, fully printed submicron CNT-TFTs on Kapton exhibited similar drive current to recent display backplane transistors, showing the viability of CNT-TFTs for display applications.

Capillary flow printing of nanomaterials

Direct-write, contact printers deposit material while the nozzle is touching the substrate to realize well-defined printed lines. Several direct-write printers have harnessed pressure[35,36] or electrical signals[37,38] to deposit ink while in contact with the substrate, achieving sub-500 nm features for chrome etchant[39] and photoresist[40]. Additionally, there have been uses of in-plane capillary deposition techniques to pattern inks, such as the self-aligned capillary-assisted lithography for electronics (SCALE) process[41,42]. These in-plane methods rely on inks flowing through capillaries that are physically imprinted into the substrate using a stamp, diminishing the number of compatible substrates and the customizability of the print patterns[43,44].

Combining capillary and direct-write printing, a capillary flow printing (CFP) system can be achieved. Borrowing concepts from an AFM, CFP deposits inks using a macroresonator tuning fork to detect deflections of a tip scratching across a surface at high frequencies (Extended Data Fig. 1). When a micropipette is placed on the end of the resonator and filled with a printable ink, the tip is able to effectively write or draw patterns of this ink onto a substrate, much like a fountain pen[45–47]. A wide range of materials are compatible with CFP, including biological materials[48,49], metallic CNTs[50], metal nanoparticles[51,52], self-assembled monolayers[53], and ruthenium

complexes[54] (see Supplementary Table 1 for full analysis of previous uses of CFP-style techniques). The high precision yet gentle contact of CFP makes this technique uniquely suited for biological applications, such as modifying cells[55] or patterning DNA[49]. Another potential application space is TFTs since highly scaled devices realized by CFP may be used for sensors or display backplanes[10]. While CFP has not yet been harnessed to print nanomaterial-based transistors, the capillary nib of a water marker pen has printed organic materials to fabricate organic field-effect transistors with low resolutions[56]. Interestingly, when a CFP technique was used to print CNTs from a sub-150 nm pipette tip diameter, the CNTs became aligned (90% at an angle below 30°) in the direction of writing[57,58]. By achieving aligned semiconducting CNT films for TFTs, there is potential for further improving the performance of printed devices as revealed by the aligned CNT films achieved through a modified dip-coating method[59].

In this work, a tabletop CFP system (Fig. 1a-c) was used to rapidly print nanomaterial patterns, resulting in fully printed CNT-TFTs with submicron channel lengths. When the pipette is in contact with the substrate surface, an ink meniscus is formed, meaning that when the pipette (or substrate) is moved, the meniscus leaves behind a "printed" pattern with virtually any ink (Fig. 1d). The macroresonator allows for the CFP nozzle to move vertically to account for topology changes on the substrate, ensuring the ink deposition is uniform on rough substrates such as paper or Kapton, similar to non-contact printing methods. This system may print inks with viscosities up to 100,000 cps, including inks with nanoparticles that are smaller than the diameter of the chosen nozzle, such as silver nanoparticles (AgNPs)[60], and particle-free inks such as SU-8[47] and PVP[60]. There are many factors that influence the line width of the deposited material, including diameter of the tip, wetting of ink on substrate and tip[54], evaporation rate of solvent[61], and particle displacement and diffusion in the meniscus[62]. The changes in ink spreading are readily accounted

for in the software-based "spreading factor" parameter to enable a fine degree of control over print features for each design. Note that the CFP system may print up to a speed of 10 mm/s and may be outfitted with many nozzles to continue to increase the throughput of the printer for scaling up manufacturing[45,51,63].

In this CFP tool, computer-aided design (CAD) files of the patterns are printed through movement in the X-Y plane of the platen holding the substrate (Supplementary Fig. 1). This capability not only enables rapid prototyping but also allows for the alignment of multiple layers, which is necessary to realize complex electronics such as CNT-TFTs. To demonstrate the fine control and versatility of this tool, several patterns were printed using different inks. Within the context of transistor fabrication, AgNP source and drain line spacing, or channel length (L_{ch}), may be tuned down to the 100s of nanometers with uniformity throughout the spacing, as seen in Fig. 1e. To demonstrate the printer's fine control capabilities, two AgNP electrodes were printed with a ~340 nm gap between them, as measured by scanning electron microscopy (SEM) (Fig. 1f), and shown to not be shorted together (i.e., electrically an open circuit) when tested. Importantly, this was achieved without any surface modification of the substrate or printed traces – the AgNP lines were simply printed directly onto the substrate with the 340 nm gap. Additionally, a Duke logo was printed from the AgNP ink, with a total pattern width of 200 μm, showcasing the ability for fine control to create high-resolution printed patterns (Fig. 1g). This highlights a key attribute of this printing technology: the ability to create printed patterns at submicron, and even sub-500 nm scales, which is particularly useful for the miniaturization of printed transistors.

Capillary flow printing is compatible with ink viscosities up to 100,000 cP, with no special accommodation needed from the user to enable material deposition with well-defined edges (i.e., no need for adjustment of piezoelectric driver or atomization current/flow parameter settings used

in other printers). This aspect of the printer is shown in Figures 1h-i, where ion gel of the same formulation was deposited using CFP and AJP, highlighting an important distinction where CFP produces thinner traces in height and width as well as crisp line edges without overspray (i.e., errant aerosolized particles from AJP). Additionally, CFP enables the printing of SU-8 6000.5 without dilution or other treatments – a reduction in processing steps from AJP printing of SU-8 (Supplementary Fig. 2a)[64]. To improve printability and reduce nozzle clogging in CFP, solvent volatility, surface tension, and nanoparticle dimensions must be accounted and optimized for when printing custom inks. When these factors are adjusted for, the application space for CFP-printed devices is wide. For example, scaling down dimensions enables the printing of many devices in a small area (132 devices were printed in 1 mm^2), such as the shrinking of biosensors to reduce the amount of liquid needed for conformal coverage of all devices (Fig. 1j and Supplementary Fig. 2b-c).

Submicron printed carbon nanotube transistors

To demonstrate the utility of CFP in printing CNT-based transistors, we began with a simple back-gated, bottom-contacted, and toluene-rinsed CNT-TFT device on Si/SiO_2 (this method uses the fewest steps and follows that used in previous work)[65]. This process requires two printing steps: 1) printing pairs of AgNP electrodes with <1 μm gap between them, followed by sintering of the AgNP patterns at 200 °C for 90 minutes, and 2) printing a CNT ink above the gap and rinsing the chip in 80 °C toluene for 10 minutes. It is worth noting that completely obviating the use of toluene (both in the ink solvent and in rinsing), which would promote better environmental stewardship, is possible with additional ink optimization[5]. An optical image of the CNTs being printed is shown in Figure 2a, where a visible line is seen due to residual ink solvent (toluene). SEM imaging confirms the presence of a dense and percolated CNT network bridging

the submicron channel length (Fig. 2b), thus forming a full back-gated CNT-TFT (the schematic of which is shown in Fig. 2c).

Among the most important of the many tunable parameters for CFP are print speed and ink formulation. First, we examined the effect of increasing the print (i.e., stage movement) speed during the printing of AgNP electrodes. As shown in Figure 2d, with a slow print speed (20 μm/s), the line is uniform with low edge roughness, allowing for fine control over the quality of the print, enabling consistency in printing submicron gaps between silver lines. As the speed is increased to 200 μm/s and 2 mm/s, control over the quality of the printed lines decreases, as is evident by the increase in low-density AgNPs at the edges of the printed line. This trend follows with the height of the printed AgNPs (Fig. 2e-f) – as the print speed is increased, there is less ink being deposited, meaning that the lines are thinner, but only to a certain point after which the height levels off and the width shrinks instead (Fig. 2g). Ultimately, a 20 μm/s print speed was used throughout this work due to the uniformity and repeatability of the printed lines, allowing for submicron gaps between the electrodes to be realized. Achieving a submicron gap is pivotal for boosting performance in CNT-TFTs as conduction through the channel changes from a percolation network (in which CNT-to-CNT junctions add series resistances in the channel region) to single CNTs bridging across the electrodes, significantly decreasing the channel resistance[66].

Similarly, while there are many ink formulation parameters that could vary print quality (e.g., viscosity, volatility, surface tension), CNT ink concentration tends to be the most significant with direct-write printing techniques and was thus our focus in this study. Density of the CNT thin film is critical and strongly dependent on ink concentration (Extended Data Fig. 2); a density that is too low will not yield sufficient percolative transport linkage in the transistor channel while density that is too high will increase the probability of a metallic nanotube electrically shorting the

submicron channel[67]. As shown in Figure 2h, the density of the film is relatively low at 25 µg/mL (barely forming a network between the two electrodes), moderate at 37.5 µg/mL (forming a dense cluster in a single thin area), and high at 50 µg/mL (forming a uniform, dense, and consistent film). Thus, 50 µg/mL was chosen as the ink concentration of choice for the remainder of the studies in this work. The high density after only one print pass is attributed to CNTs diffusing evenly within the meniscus and the electrostatic force between CNTs and the substrate allowing them to be deposited in one single layer throughout the entire printed line width[62]. Software-based CNT density analysis of SEM images of different devices showed a mean density of ~54.3% surface coverage, with a standard deviation of 4.8%, and a representative channel width (W_{ch}) of 15.5 µm (Extended Data Fig. 3). The average W_{ch} used for width normalization (e.g., for drain current in A/mm) was 16.4 µm. Since the pipette diameter used in this work is 5 µm, the deposited CNT film is a dense, randomly oriented percolation network with a well-defined width achievable with a single print pass.

In fabricating the back-gated CNT-TFTs, two different contacting architectures were examined: bottom contacts (Fig. 3a) and top contacts (Fig. 3b). Subthreshold (Fig. 3c) and transfer (Fig. 3d) curves of five representative bottom-contacted devices (all with submicron L_{ch}) show the strong device performance of this contact geometry. All five devices showed relatively similar performance, with modest on-currents of ~10-30 µA/mm, but with on/off-current ratios of 3 orders of magnitude. Interestingly, top-contacted devices (Figs. 3e-f) performed much better in terms of uniformity and on-current, reaching up to 1000 µA/mm, (average of 956 ± 112 µA/mm) but with a slightly lower average on/off-current ratio. Further, the transconductance of the top-contacted annealed devices is about two orders of magnitude higher than the bottom-contacted, toluene-rinsed devices (Supplementary Fig. 3). This noticeable improvement in on-current (by ~3 orders

of magnitude) and transconductance for top-contacted CNTs is attributed to the combination of better removal of residual wrapping polymer used in the CNT ink by using rapid thermal annealing (RTA) after CNT printing as well as more conformal interfacing of the CNT thin film with the substrate (which improves gating efficiency). However, this method is not always favorable as there is a tradeoff between high-temperature baking (a mechanism of obtaining high I_{on}) and material compatibility. Toluene rinsing the chip (soaking in toluene at 80 °C for 10 minutes) is an easier technique that is compatible with all components of the device (Si substrate, Ag electrodes, CNT channel) and a wide range of other substrates (e.g., Kapton), though it does require the use of an environmentally toxic solvent[5]. Contrarily, RTA avoids that issue and could be even more efficient at removing residual surfactant, but it does require an expensive and relatively energy-intensive tool that demands a higher thermal budget for all materials; in this case, the silver electrodes would corrode under such high heat (500 °C) and lose conductivity. Thus, these findings demonstrate the applicability of CFP with both post-processing techniques but emphasize the need to consider the tradeoff between performance, environmental impact, and material considerations.

Post-processing methods like burn-in and sintering could further enhance device performance. Burn-in is a technique where a high electric field is applied across the channel (via applied source-drain voltage, V_{DS}) to induce resistive heating that has a localized sintering effect on the film (Fig. 3g). Figure 3h illustrates the notable improvement in device performance characteristics for a bottom-contacted device; it showed an on-current of 21 μA/mm and an on/off-current ratio of $10^{1.8}$ before burn-in (light blue curve), and an on-current of 145 μA/mm and on/off-current ratio of $10^{3.4}$ after burn-in (dark blue curve). This increase in on-current is a result of burning off the residual insulating polymer, while the decrease in off-current is due to the burning of metallic tubes (note, burn-in was performed while a positive gate-source voltage was applied to

hold the semiconducting CNTs in the off-state). Similarly, longer sinter times show drastic improvements in the on-current of the device, with up to 672% change in normalized on-current between 20 minutes and 90 minutes of sintering (Fig. 3i-j). These two effects illustrate the possibilities of improving device performance through relatively simple techniques.

Fully printed submicron carbon nanotube transistors

To achieve the full potential of CFP for printed CNT transistors, the devices must be printed onto substrates beyond silicon through the addition of a printed dielectric and gate (Fig. 4a). We printed ion gel as the gate dielectric using AJP or CFP (Fig. 4b-c), modulating the CNT channel with low applied voltages (V_{DS} = -0.5 V, V_{GS} = ±1 V) due to the rapid formation of an electric double-layer (EDL) under applied electric fields attributed to the high ionic conductivity of the ion gel[68]. Although gating through ion gel degraded the on-, off-, and leakage currents, several device performance characteristics such as hysteresis, SS, and threshold voltage were improved along with a reduction in power consumption (Fig. 4d-e, Supplementary Fig. 4), highlighting the trade-off between gating through SiO_2 and ion gel.

The fully printed submicron CNT-TFTs gated with AJP ion gel (using a well-established ion gel print procedure) were further compared to devices gated with CFP ion gel. The submicron channels were successfully gated through AJP and CFP ion gel of the same formulation, modulating the channel within a V_{GS} of ± 1 V (Fig. 4e-f). When gating through ionic dielectrics, transistor performance depends on the sweep rate of the gate voltage due to the movement of ions within the film that form the EDL[65,68,69]. In comparing the sweep rate dependence of AJP and CFP ion gel-gated devices, most performance metrics showed similar trends in the measured range between 20 and 430 mV/s (Fig. 4e-f and Supplementary Fig. 5). Further, at lower sweep rates, the performance characteristics of both ion gels were similar besides a lower hysteresis, leakage

current, and subthreshold swing for the CFP ion gel. This study also revealed that the CFP ion gel has a greater resilience to changes in sweep rate for all examined device performance metrics. Notably, a 1550% and 148% change in I_{off} from 20 to 430 mV/s was observed for AJP and CFP ion gel devices, respectively.

The robustness and improved performance of the CFP ion gel may be attributed to the thinness of the resultant CFP film (<1 μm) compared to the AJP film (~10–20 μm) (Fig. 1h-i, and Fig. 4b-c), which reduces the total number of ions within the film and the average distance the ions must travel to form the EDLs. This lowers the time it takes to charge the EDLs since the ion gel's capacitance (16 nF cm^{-2} at 1 kHz[65]) is the same regardless of the thickness of the film[70]. CFP also produced ion gel traces with cleaner, overspray-free edges, reducing the ion gel coverage over the electrodes, which lowered the gate leakage current (Fig. 1h and Fig. 4c). This result provides further insight into the ion gel's thickness and resistance dependence with respect to frequency by using a side-gated structure as previous studies have observed this dependence using a vertical capacitor stack[70] and top-gated transistor[65]. To continue to improve the on-, off-, and leakage currents of the ion gel-gated devices, the ion gel may be patterned exclusively over the channel region or the source and drain electrodes may be passivated with an additional dielectric layer to suppress leakage pathways[71,72]. Further, the gating efficiency and switching speed may be increased through the use of a top gate rather than side-gate configuration, which may also boost other performance metrics such as on-current and transconductance.

Due to the superior performance of CFP ion gel, we benchmarked these devices relative to other fully printed CNT-TFTs on flexible substrates shown in literature, comparing channel length and a key performance metric (on-current, I_{on}). Importantly, at a gate sweep rate of 20 mV/s, the on-current behavior for these fully printed CFP CNT-TFTs (with AJP ion gel) is the highest,

especially for a channel length below a micron (Fig. 4g and Extended Data Fig. 4; data from Extended Data Table 1). The current of the CFP CNT-TFTs rivals that of the IGZO and LTPS devices, at a channel length smaller than a tenth of the devices fabricated with plasma-enhanced chemical vapor deposition (PECVD) processing. The relatively high on-current at a low drain-source voltage (490.4 μA/mm at a V_{DS} of -0.5 V) highlights the ability to achieve high-quality films with CFP even on rough surfaces like Kapton. This feat is particularly impressive when considering that these CNT-TFTs simultaneously push the achievable channel length of printed devices to well below a micron and demonstrate the viability of CFP CNT-TFTs for high-density applications on flexible substrates.

To assess the suitability of CFP CNT-TFTs for flexible electronics, submicron channels were fabricated using CFP on Kapton and tested for mechanical robustness (Fig. 4h). Ion gel was printed using AJP rather than CFP due to the surface roughness of Kapton, which may be overcome with optimization of CFP parameters[65]. The resultant 8 devices underwent mechanical stress testing from 0 to 1000 bend cycles around a 2 mm bend radius (Fig. 4i). Interestingly, although all average performance parameters worsened after 1000 bend cycles (besides I_{off}), most degradation of the device performance occurred within the first 100 bend cycles, with some recovery and relative stabilization as bending continued (Supplementary Fig. 6). This slight change and recovery in performance is attributed to the AgNPs shifting during bending to initially create and then partially fill microcracks in the film, as has been seen in studies of other printed AgNP thin films[73,74]. To improve the mechanical resilience of the AgNPs, the film thickness[75] and anneal time[76] may be further optimized. Contributions to the change in performance throughout bending is not likely from the ion gel or CNTs as both have shown high stability in their electrical properties throughout similarly aggressive mechanical bending[65]. Importantly, the overall performance of the

devices remained strong after 1000 bend cycles, demonstrating the mechanical resilience of CFP submicron devices, and paving the way for their use in flexible electronics applications.

Although CFP submicron devices mitigate pollutants by eliminating the use of cleanroom processes, ion gel is toxic to the environment. Therefore, to improve the sustainability of the submicron devices, crystalline nanocellulose (CNC), a biodegradable ionic dielectric[3], was also aerosol jet printed as the gate dielectric. Due to the high ionic resistance of nanocellulose, a recyclable graphene gate was aerosol jet printed over the CNC, covering the CNT channel region[3]. Since CNC is also an ionic dielectric, the gate sweep rate from 20 to 520 mV/s influenced the performance of the device with similar trends to those seen in the ion gel study (Extended Data Fig. 5). One noteworthy difference was the change in hysteresis direction around 50 mV/s from counterclockwise at slower sweep rates to clockwise at faster sweep rates, attributed to the charging current of the EDL at faster sweep rates (Extended Data Fig. 5c-d)[5]. The compatibility of CFP submicron transistors with AJP CNC and the ability of CFP to print conductive AgNP electrodes on paper substrates (Supplementary Fig. 7) are significant steps toward improving the sustainability of printed submicron transistors.

Conclusions

We have reported the direct printing of submicron channel length CNT-TFTs on both rigid and flexible substrates using a capillary flow printer. Channel lengths as small as 500 nm were fabricated with no chemical modification required using AgNP ink for source/drain electrodes. CFP of CNTs as the semiconducting channel material between submicron-spaced electrodes on SiO_2 yielded devices with on-currents up to 1.12 mA/mm. We also illustrated the versatility of this technique through its use in printing a wide variety of materials (AgNPs, CNTs, SU-8, and ion gel), different contact geometries (bottom and top contacts), and gating architectures (bottom, side,

and top gates) on various substrates (Si, Kapton, and paper). Furthermore, the sweep rate and bending resilience of these fully printed devices highlighted the utility of the approach in flexible electronics applications and beyond.

Methods

Materials

Silver nanoparticle (AgNP) ink was purchased from Hummink with an ink weight fraction of 68 +/- 2 wt% and was printed as purchased. Semiconducting CNTs (IsoSol-S100 polymer-wrapped nanotubes) were purchased from NanoIntegris Inc at a concentration of 50 μg/ml. The as-purchased ink was ultrasonicated for 1 hour to redisperse the CNTs into solution then printed without dilution unless otherwise noted. SU-8 6000.5 photoresist was purchased from Kayaku and printed without dilution. Ion gel was prepared by combining polystyrene-*b*-methyl methacrylate-*b*-styrene (PS(600)-*b*-PMMA(118000)-*b*-PS(600)) purchased from Polymer Source Inc, 1-ethyl-3-methylimidazolium bis(trifluoro-methylsulfonyl)imide (EMIM-TFSI) purchased from Sigma-Aldrich, and ethyl acetate purchased from Sigma-Aldrich in a 1:9:90 ratio by weight. The ion gel was stirred overnight before use in the printers. The crystalline nanocellulose (CNC-Slurry-HS) was purchased from Cellulose Lab at a concentration of 10 wt% solids. To prepare the ink for printing, the CNC was diluted in DI water to a concentration of 6% wt/wt CNC. Sodium chloride (>99.0% ACS reagent grade) was purchased from Sigma-Aldrich and was added to the CNC solution to a concentration of 0.05% wt/wt NaCl. Graphene ink (Sigma-Aldrich at 10 wt% graphene concentration) was diluted with DI water to an approximately 2.33 wt% solution of graphene before printing. Silicon wafers (p-doped) were purchased from University Wafer Inc with 90 nm of SiO_2. The Kapton polyimide film (electrical-grade Kapton polyimide film) was purchased from McMaster-Carr with a 0.001-inch thickness.

CFP printing

All printing was performed on a NAZCA printer (Hummink) with a glass pipette diameter of 5 μm. Hummink's autotune was used to find the resonant frequency of each pipette when filled with the specific ink being printed.

AgNP printing

All AgNP films on silicon were printed with a print speed of 20 μm/s, a lift level of 20 μm, and a frequency shift of 500 mHz. On Kapton, AgNP traces were printed with a print speed of 50 μm/s, a lift level of 20 μm, and a frequency shift of 200 – 500 mHz. One pass of AgNP ink was used in all prints. After printing, the AgNP traces were sintered 200 °C for 90 minutes in an oven.

Semiconducting CNT printing

All CNT films on each substrate were printed with a print speed of 20 μm/s, a lift level of 20 μm, and a frequency shift of 500 mHz. One pass of CNT ink was used in all prints. After printing, the CNT films were either soaked in a toluene bath for 10 min at 80 °C to remove excess wrapping polymer or annealed in a rapid thermal annealing system (Jipelec JetFirst 100) at 500 °C for 8 min with a 2-min temperature ramp to achieve a sufficiently conductive transistor channel.

SU-8 printing

All SU-8 6000.5 photoresist films on each substrate were printed with a print speed of 100 μm/s, a lift level of 20 μm, and a frequency shift of 500 mHz. One pass of SU-8 ink was used in all prints. After printing, the SU-8 film was exposed to UV light (365 nm) for 9 seconds then baked post-exposure for 2 min at 110 °C.

Ion gel printing

All ion gel films on each substrate were printed with a print speed of 50 μm/s, a lift level of 20 μm, and a frequency shift of 500 mHz. One pass of ion gel ink was used in all prints. The ion gel was functional as printed; therefore no post-processing was completed.

Aerosol jet printing

All aerosol jet printing was performed on an AJ-300 printer (Optomec).

Ion gel printing

A 150 μm diameter nozzle was used to print all ion gel films with the platen temperature at 80 °C and the ink temperature at 20 °C. A print speed of 2 mm/s, a sheath flow rate of 25 SCCM, an atomizer flow rate of 26 – 27 SCCM, and an ultrasonic current of 300–350 mA were used. One pass of ion gel ink was used in all prints.

Crystalline nanocellulose printing

A 300 μm diameter nozzle was used to print all CNC films with the platen at room temperature and the ink bath temperature at 20 °C. A print speed of 2 mm s^{-1}, a sheath flow rate of 30 SCCM, an atomizer flow rate of 35 SCCM, and an ultrasonic current of 400 – 450 mA were used. One pass of crystalline nanocellulose ink was used in all prints.

Graphene printing

A 150 μm nozzle was used to print graphene films with the platen temperature at room temperature and the ink bath temperature at 20 °C. A print speed of 2 mm s^{-1}, a sheath flow rate of 25 SCCM, an atomizer flow rate of 37-40 SCCM, and an ultrasonic current of 350 – 400 mA were used. One pass of graphene ink was used in all prints.

CFP transistor fabrication

Back-gated bottom-contacted transistors

To print the back-gated bottom-contacted transistors, a Si/SiO_2 wafer was placed onto the capillary flow printer platen. AgNP source and drain electrodes and contact pads were printed using the above print parameters for the AgNP ink. After AgNP printing, the substrate was baked at 200 °C for 90 min in an oven to achieve conductive AgNP films. The substrate was placed back onto the capillary flow printer platen and the CNT channel was printed using the above parameters. After CNT printing, the substrate was soaked in a toluene bath at 80 °C for 10 min to remove the binding polymer wrapped around the CNTs to achieve a conductive transistor channel.

Back-gated top-contacted transistors

To print the back-gated top-contacted transistors, a Si/SiO_2 wafer was placed onto the capillary flow printer platen. AgNP alignment marks were printed using the above print parameters for the AgNP ink. Without removing the substrate from the printer, the CNT channel was printed using the above parameters. After CNT printing, the substrate was either soaked in a toluene bath at 80 °C for 10 min or annealed in a rapid thermal annealer at 500 °C under nitrogen for 8 min to remove the binding polymer wrapped around the CNTs to achieve a conductive transistor channel. AgNP source and drain electrodes and contact pads were printed using the above print parameters for the AgNP ink. After AgNP printing, the substrate was baked at 200 °C for 90 min to achieve conductive AgNP films.

Fully printed ion gel-gated transistors

To create fully printed transistors, a Si/SiO_2 wafer or Kapton film was placed onto the capillary flow printer platen. AgNP source, drain, and side-gate electrodes and contact pads were

printed using the above print parameters for the AgNP ink. After AgNP printing, the substrate was baked at 200 °C for 90 min in an oven to achieve conductive AgNP films. The substrate was placed back onto the capillary flow printer platen and the CNT channel was printed using the above parameters. After CNT printing, the substrate was soaked in a toluene bath at 80 °C for 10 min to remove the binding polymer wrapped around the CNTs to achieve a conductive transistor channel. The substrate was placed onto either the aerosol jet printer or capillary flow printer and the ion gel gate dielectric was printed (350 x 150 μm square) using the above parameters.

Fully printed CNC-gated transistors

The same process was followed as for the fully printed ion gel-gated transistors with the exception of the final two steps where CNC and a graphene top gate were printed using AJP in this case.

CNT density analysis

CNT films were printed with CFP over AgNP electrodes with the parameters outlined above. An SEM was used to take images of each print and ImageJ, an image processing software, was used to determine the CNT density within the channel region. After uploading the image to ImageJ, the image threshold was adjusted, setting the image to binary. The brightness and contrast were manually changed to ensure the CNTs were sufficiently distinguishable from the background (Extended Data Fig. 3a-c). The desired channel region was selected and the area fraction was measured using the built-in ImageJ procedure. The resulting average CNT density was 54.3 ± 4.8%. After calibrating the image dimensions with the scale bar, the width of the channel was also measured (Extended Data Fig. 3d). The resulting average width of the channels was 16.4 ± 1.2 μm.

Instrumentation and characterization

SEM (ThermoFisher Scientific Apreo S) images and profilometry (Keyence VK-X3050) measurements were taken at the Shared Materials Instrumentation Facility (SMIF) at Duke. All electrical TFT measurements were completed with a manual analytical probe station connected to SMUs (Keysight B2902A).

Device parameter extraction

All extracted data was on the forward sweep ($-V_{GS}$ to $+V_{GS}$) other than hysteresis. The on-current was taken as the maximum current of the device in the p-type (largest magnitude negative gate voltage) regime. The off-current was taken as the minimum current of the device. The subthreshold swing was calculated as the minimum inverse slope of I_D on the p-type branch of the subthreshold curve averaged over ~0.2 V from maximum to minimum current. The gate leakage current was the average measured gate current at gate voltages at 20% of the maximum V_{GS} for the forward and backward sweep. The threshold voltage was taken at 0.1 μA for the fully printed devices. Since the performance of the back-gated devices is variable, the threshold voltage (V_{th}) was taken at an I_D value halfway between the minimum and maximum current. The hysteresis was measured as the voltage difference between the forward and reverse sweep for that same I_D value. The transconductance was the slope of the best fit line between 85% and 70% of the maximum V_{GS} on the p-branch for all devices.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Author Contributions Statement

B.N.S., F.M.A, and A.D.F. conceived the study. B.N.S., F.M.A., J.L.D, X. P., Q. M., M. S., and D. B. fabricated and tested the devices. B.N.S. and F.M.A. contributed to figure design and data analysis. M.P., P.B., N.B., and A.M. contributed to AgNP ink development and print conditions for submicron features. A.D.F. provided scientific guidance and supervised the project. B.N.S, F.M.A. and A.D.F. wrote the manuscript with revision and approval from all authors.

Competing Interests Statement

M.P., P.B., N.B., and A.M. are employees of Hummink, which develops and sells the NAZCA capillary flow printer. The remaining authors declare no competing interests.

Figure Legends/Captions (for main text figures)

Fig. 1 | Capillary flow printer capabilities. Pictures of (a) Hummink NAZCA capillary flow printer, (b) pipette printing on silicon wafer, and (c) pipette making direct contact with substrate while printing. (d) Schematic of capillary flow printing of AgNPs. SEM images of two sets of CFP AgNP traces showing (e) well-defined AgNP edges and a uniform gap between electrodes extending across 10s of microns and (f) an

electrically open gap (i.e., transistor channel length) of ~340 nm. (g) Profilometry profile of Duke logo printed with AgNPs. Pictures of ion gel traces printed by (h) CFP and (i) AJP with insets of profilometry showing CFP ion gel's thin trace and defined line edges (without overspray). (j) Image of 132 devices printed in a 1mm-by-1mm square, demonstrating CFP's ability to scale down device dimensions.

Fig. 2 | Capillary flow printing submicron CNT-TFTs. (a) Image of capillary flow printer depositing CNT ink onto printed AgNP electrodes. (b) SEM image of dense film of CNTs printed onto AgNP electrodes with a submicron channel length. (c) Schematic of a capillary flow printed CNT-TFT on 90 nm SiO_2 indicating submicron channel lengths (L_{ch}) can be realized without chemical treatments or modifications. (d) SEM images of capillary flow printed AgNP traces at print speeds of 20 μm/s, 200 μm/s, and 2 mm/s (from top to bottom), realizing denser and more uniform films at slower print speeds – all images at same magnification. Image (left) and profilometry measurement (right) of CFP AgNP electrodes printed at (e) 20 μm/s and (f) 200 μm/s. (g) Plot showing the mean AgNP trace height change as print speed is varied for n=4 with error bars representing +/- standard deviation. (h) SEM images of capillary flow printed CNT traces over AgNP electrodes at CNT ink concentrations of 25 μg/ml, 37.5 μg/ml, and 50 μg/ml (from top to bottom), realizing denser and more uniform films at higher concentrations.

Fig. 3 | Electrical characterization of back-gated CFP submicron CNT-TFTs. Schematic of process flow for printing (a) bottom-contacted and (b) top-contacted CNT-TFTs using CFP. Subthreshold (c) and transfer (d) curves for five bottom-contacted CNT-TFTs, with corresponding schematic and extracted parameters inset. Subthreshold (e) and transfer (f) curves for five top-contacted CNT-TFTs, with corresponding schematic and extracted parameters inset. (g) Plot demonstrating bottom-contacted device burn-in over time with V_{DS} ramp up (top) and corresponding I_D response (bottom) under an applied V_{GS} = 15 V for a device that exhibited burnout of metallic CNTs in the thin film. (h) Subthreshold curve for a device before and after burn-in, indicating performance improvement (increased on-current and on/off-current ratio). (i) Subthreshold curves for a bottom-contacted device tested after various sintering times at 200 °C. (j) Plot showing an increase in the average normalized on-current for five devices as the sintering time is increased, with error bars representing the standard deviation.

Fig. 4 | Fully printed submicron CNT-TFTs. (a) Printing fabrication process flow with schematics for side-gated CNT-TFTs. Note, AgNPs were sintered 90 min at 200 °C, and ion gel gate dielectric was printed over side-gate electrode and channel regions. Profilometry and optical image of (b) AJP and (c) CFP ion gel of the same formulation printed over a device with designed dimensions of 350 µm x 200 µm. (d) Subthreshold curves at different V_{ds} of a device with L_{ch} = 760 nm, back gated through SiO_2. Subthreshold curves at different sweep rates side gated through (e) AJP ion gel and (f) CFP ion gel on SiO_2. (g) Benchmarking plot of width-normalized on-current vs channel length for fully printed CNT-TFTs with Ag source and drain contacts. Data for other CNT-TFTs can be found in Extended Data Table 1. (h) Optical images of a fully printed CNT-TFT with ion gel gate on Kapton, with devices bent around a 2 mm rod to measure mechanical stability. (i) Subthreshold curves of bending cycles from 0 to 1000 cycles around a 2 mm bending radius for an ion gel-gated device with channel length of 560 nm, revealing minor degradation at 100 bends but remarkable recovery in device performance as bending proceeded. All channel widths ~ 9 µm.

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