A 4.2-to-0.5-V, 0.8-μA–0.8-mA, Power-Efficient Three-Level SIMO Buck Converter for a Quad-Voltage RISC-V Microprocessor

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***Abstract*— This article presents a Li-ion battery-compatible single-inductor-multiple-output (SIMO) buck converter that fulfills the power management need of an integrated sub-mW RISC-V microprocessor. The proposed converter can directly take a 4.2-V battery voltage and produce four power rails ranging from 1.8 V for I/O to 0.5 V for the processor core. The three-level input stage is chosen to reduce the inductor ripple size and switching loss, thus increasing power conversion efficiency (PCE). In addition, the fully digital implementation using novel domino flash analog–digital converters (ADCs) enables low static current. Also, pulse frequency modulation (PFM) results in a wide dynamic range. The proposed three-level SIMO converter has been prototyped in a 65-nm CMOS technology with the 32-bit RISC-V processor. Measurement results show that the converter achieves a 1000× load current range (0.8 μA–0.8 mA) to support the active or sleep modes of the processor. The converter marks the PCE of 56.2%–72.8%. Compared to the ideal buck-low-dropout voltage regulator (LDO) architecture (LDO-only), it improves the PCE by 23.8% (46.4%).**

***Index Terms*— Inductor-based power converters, multilevel converters, RISC-V microprocessors, single-inductor–multiple-output (SIMO) converters, ultralow power (LP).**

I. Introduction

A SUB-mW near-threshold-voltage (NTV) system-on-chip (SoC) integrates multiple cores, embedded SRAM, and analog/RF blocks for mobile, wearable, and embedded devices [1], [2]. It demands a novel power management architecture that takes Li-ion battery voltage (3.8–4.2 V) as input and produces multiple and wide-range output voltages for those building blocks. Indeed, this power management architecture must do so with a high conversion ratio, have a small form factor with few off-chip passive components, and cover a wide range of output power.

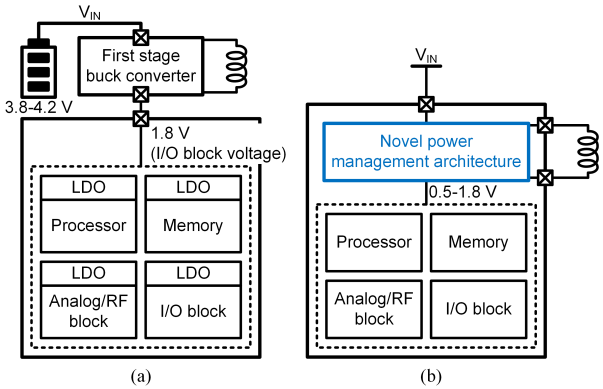

Fig. 1. (a) Conventional and power management architecture using a single buck converter followed by an array of LDOs. (b) Proposed power management architecture employs only one shared inductor.

Several architectures can be considered for such a power management need. First of all, we can employ multiple switched-capacitor (SC) converters. It is feasible to fully integrate them on a chip [3], [4], [5]. However, they can support only certain discrete conversion ratios. The efficiency degrades if they operate outside of those conversion ratios. On the other hand, employing multiple buck converters can offer the highest energy efficiency at an arbitrary conversion ratio. However, it requires multiple off-chip inductors, increasing printed circuit board (PCB) complexity, cost, and form factor. Alternatively, we can employ a single buck converter with an array of low-dropout voltage regulators (LDOs) [6]. Fig. 1(a) shows such an architecture. However, it achieves only limited power conversion efficiency (PCE) due to the large linear loss of LDOs, especially if they need to provide a wide range of output voltages.

In this work, we pursue the single-inductor multiple-output (SIMO)-based architecture [see Fig. 1(b)]. Such SIMO buck converters can create multiple voltage domains using only one inductor [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21]. The inductor current of an SIMO converter is distributed to multiple outputs, regulating output voltages. An SIMO converter can support arbitrary output voltage levels while maintaining good PCE.

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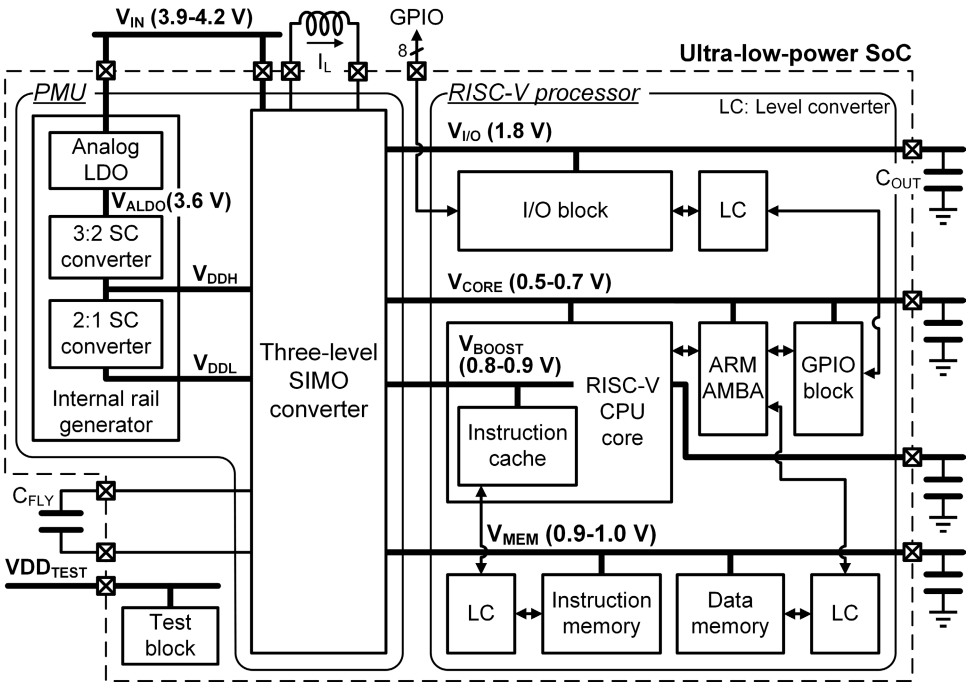

Fig. 2. Proposed ultra-LP SoC architecture.

However, designing an SIMO converter for the aforementioned power management for ultralow-power (LP) SoCs presents three challenges. First, it must support a wide dynamic range in load current. A typical ultra-LP processor exhibits a large dynamic range of load current, such as 100×–1000×, because it operates across active and sleep modes [22]. Especially when a processor is in the sleep mode (light load condition), the control loss will dominate the PCE, and we must minimize it.

Second, the SIMO converter turns on each output switch for only a short time. This so-called switch turn-on time is in the order of 100 ns in our converter and should be precisely controlled. A small variation in turn-on time may largely modulate the inductor current and output voltage. To support such short turn-on time, the control hardware must achieve a similar level of latency. Such an ns-latency controller will consume significant power, especially compared to the tiny power budget given to the SIMO converter in the targeted ultra-LP SoC.

Third, it must support a high conversion ratio since the supply voltage levels used in an ultra-LP SoC are low, for example, 0.5 V or less. However, supporting a large conversion ratio increases the inductor current ripple, worsening the conduction loss and PCE [23]. To mitigate those problems, we could employ a large inductor, but this increases the overall system size and parasitic effects. In addition, it is difficult to use high-performance transistors for high voltage because the voltage rating of transistors in scaled CMOS technologies is less than 2.5 V.

In this work, we propose novel SIMO converter hardware that can directly take 3.8–4.4 V and produce four output voltages from 0.5 to 1.8 V. We create and adopt four techniques. First, we create a fully digital pulsewidth modulation (PWM) controller employing *synchronous* domino flash analog-to-digital converters (ADCs) to improve the latency performance of the controller while minimally increasing its power consumption. Second, we adopt pulse frequency modulation (PFM) to minimize the static current draw and improve a dynamic load current range. Third, we adopt the three-level input stage to maintain high PCE even when the output voltage is low (0.5 V). Finally, we develop a feedforward controller to improve the transient performance. We prototype a 65-nm test chip that integrates the proposed three-level SIMO converter with a sub-mW 32-bit RISC-V microprocessor. The silicon measurements show that the converter supports a 1000× load current range (0.8 μA–0.8 mA) with reasonably high PCE of 65.0%–61.7% across both active and sleep modes of the ultra-LP SoC.

This article is organized as follows. In Section II, we describe the design of the three-level SIMO converter. Section III describes the microprocessor design, including an RISC-V processor core, memory blocks, and peripherals. Section IV shows the measurement results of the proposed SIMO converter and then we conclude this article in Section V.

II. Proposed SIMO Architecture

A. Top-Level Architecture

Fig. 2 shows the proposed SoC architecture. The architecture integrates a digital three-level SIMO converter and a 32-bit RISC-V processor. The SIMO produces four independent outputs: 1) $V_{\mathrm{I/O}}$ (1.8 V) for the I/O driver in the RISC-V processor; 2) V_{CORE} (0.5–0.7 V) for the core, ARM advanced microcontroller bus architecture (AMBA), and general purpose input/output (GPIO); 3) V_{BOOST} (0.8–0.9 V) for the instruction cache (i-cache); and 4) V_{MEM} (0.9–1.0 V) for the instruction and data memory (DMEM). In this section, we will present

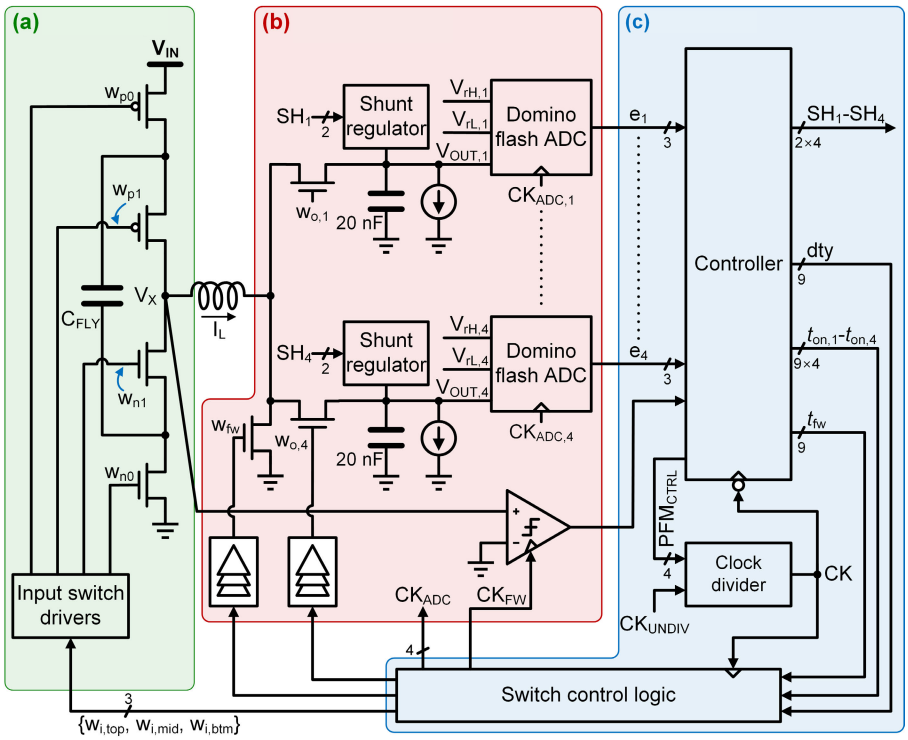

Fig. 3. Proposed digital SIMO converter architecture. (a) Input stage. (b) Output stages. (c) Controller.

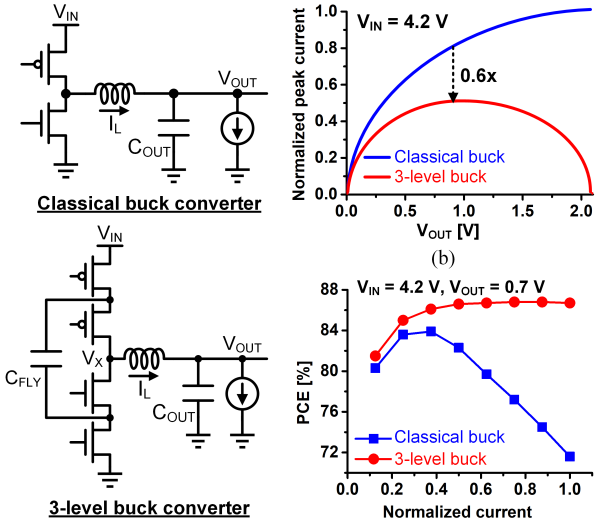

Fig. 4. (a) Schematics of the classical buck converter (top) and the three-level buck converter (bottom). (b) Inductor peak current. (c) Simulated PCE.

the details of the three-level SIMO converter. We will discuss the RISC-V processor and its building blocks in Section III.

B. Three-Level Input Stage

Fig. 3 shows the proposed digital SIMO converter architecture. It is mainly divided into three blocks: 1) an input stage; 2) output stages; and 3) a controller. The proposed SIMO takes the 4.2-V Li-ion battery output directly and supports a high conversion ratio of up to 8.4 (V_{IN}/V_{OUT} = 4.2/0.5 V).

We adopt the multilevel input stage for improving a conversion ratio while maintaining high PCE [see Fig. 4(a)]. Multilevel converters can achieve a wide input–output range by merging the advantages of inductive and conductive converters [23], [24], [25], [26]. In addition, the voltage swing at the inductor terminal V_X reduces, thus decreasing the switching loss. Even though multilevel converters require careful circuit design to address the charge balance problem [24], the advantages of multilevel converters outweigh the disadvantages.

We have analyzed the benefits of the multilevel input stage compared to the classical counterpart [see Fig. 4(a)]. The classical and three-level converters at the discontinuous conduction mode (DCM) have the same peak inductor current (I_{PEAK}) equation, as shown below

$$I_{PEAK} = \sqrt{\frac{2I_{LOAD} \cdot V_{OUT}}{L \cdot f_{SW}}\left(1 - \frac{V_{OUT}}{V_{SW}}\right)} \quad (1)$$

where I_{LOAD} is the load current, L is the inductor value, f_{SW} is the effective switching frequency, V_{OUT} is the output voltage, and V_{SW} is the voltage swing at the inductor terminal V_X.

Fig. 4(b) shows this inductor peak current when V_{IN} is 4.2 V. The three-level input reduces the voltage swing at the inductor terminal V_X (V_{SW}) by half. Therefore, based on the above equation, the effective switching frequency doubles, and the peak current decreases at the three-level SIMO converter. At 0.9 V, we observe that the peak current decreases by 60%. Fig. 4(c) shows the simulated PCE of these two converters. At high load current, the single-level buck converter exhibits significantly degraded PCE due to the large inductor ripple. In contrast, the three-level converter maintains high PCE across load levels.

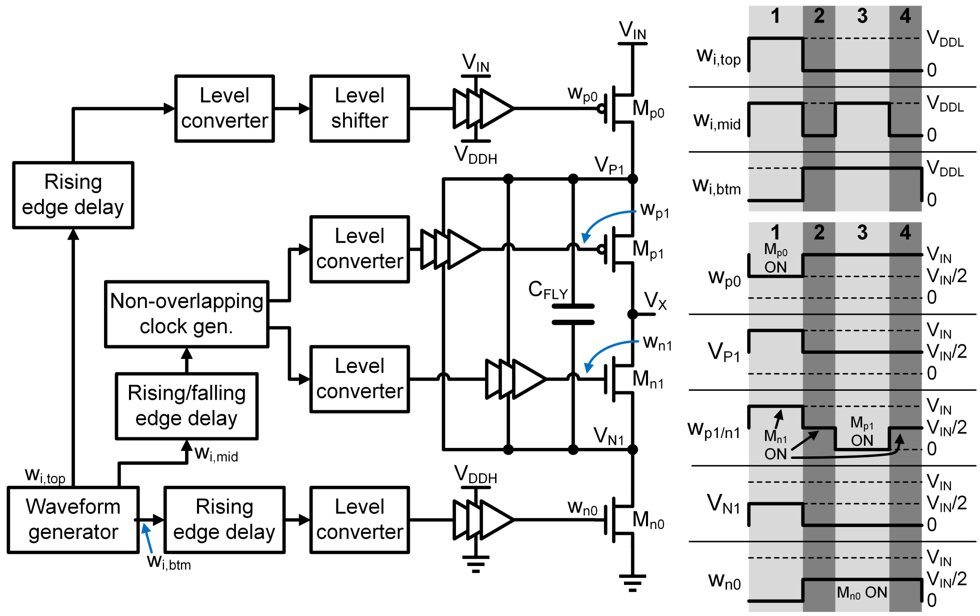

Fig. 5. Schematic of the drivers for the three-level input stage and the timing diagram of important node voltages and signals.

C. Drivers for Input Switches

The proposed SIMO produces output voltages less than $V_{IN}/2$. Therefore, when we design the drivers for input switches, we consider only the case when the duty cycle is less than 0.5 instead of all cases. V_X swings between $V_{IN}/2$ and 0, and therefore, the stacked structure can reduce voltage stress across each device to $V_{IN}/2$. Thus, we can use 2.5-V-thick-oxide transistors. Input transistors are sized so that their ON-resistances are identical.

We have designed the drivers for the three-level input stage as shown in Fig. 5. The level converters and level shifters properly set the voltage swings of gate voltages (w_{p0}, w_{p1}, w_{n0}, and w_{n1}). To reduce power consumption, we implement the driver circuits in thin-oxide transistors. Also, the input switch driver includes the rising/falling edge delay circuits and nonoverlapping signal generation circuits to remove short-circuit currents. Fig. 5 also shows the timing diagram of important node voltages and signals. The flying capacitor voltage is $V_{IN}/2$; thus, it can reduce the voltage swing of the inductor terminal V_X (V_{SW}) by half.

To supply power to these blocks, we need additional voltage rails whose voltages are much smaller than V_{IN}. Therefore, we designed and integrated the power rail generator for the SIMO converter. It generates power rails V_{DDH} ($\sim V_{IN}/2$) and V_{DDL} ($\sim V_{IN}/4$).

Fig. 6 shows the block diagram of the proposed internal power rail generator. It consists of an analog LDO, a 3:2 SC converter, and a 2:1 SC converter. The CMOS technology we choose provides a high-voltage MOS (HVMOS) for 4.2 V. However, HVMOS's performance and area efficiency are not stellar compared to the thick - and thin-oxide devices. Thus, we use HVMOS devices only for the analog LDO to generate 3.3–3.6-V V_{ALDO}. We develop the 3:2 and 2:1 SC converters using the thick-oxide devices, generating 2.2–2.4-V V_{DDH} and 1.1–1.2-V V_{DDL}, respectively.

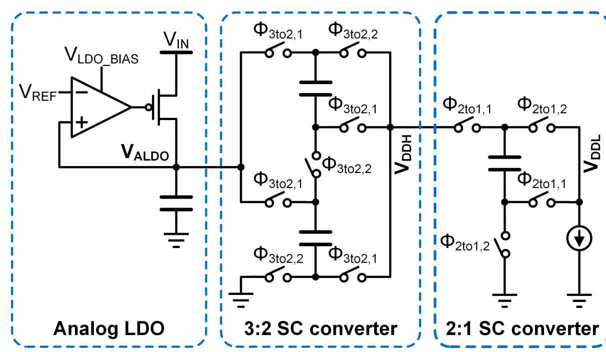

Fig. 6. Block diagram of the proposed internal power rail generator.

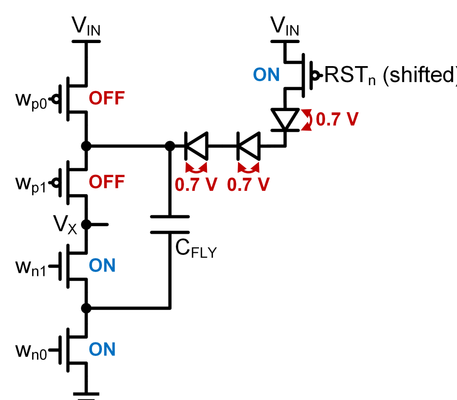

Fig. 7. Circuit for the start-up operation of the proposed converter.

Fig. 7 shows the circuit for the startup operation of the proposed converter. At the reset phase, we turn on only nMOS power transistors. With three series diodes, we charge the flying capacitor voltage to 2.1 V ($\sim V_{IN}/2$).

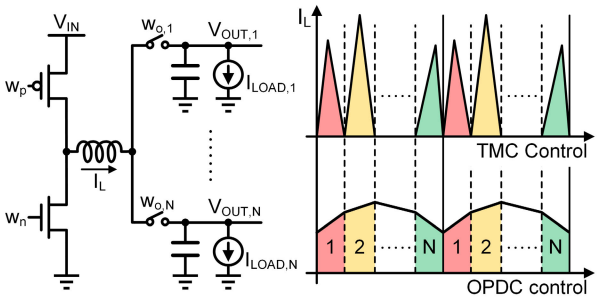

Fig. 8. Two most common SIMO controls: TMC and OPDC.

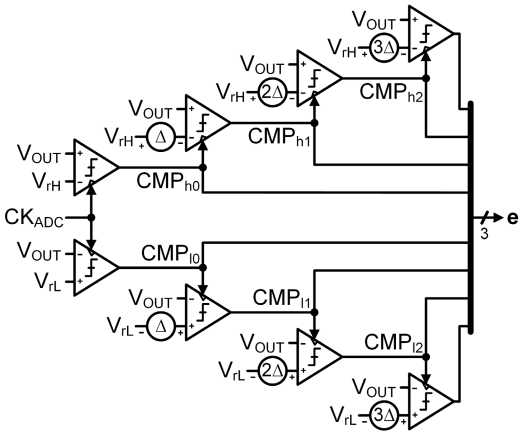

Fig. 9. Proposed 3-bit synchronous domino flash ADC.

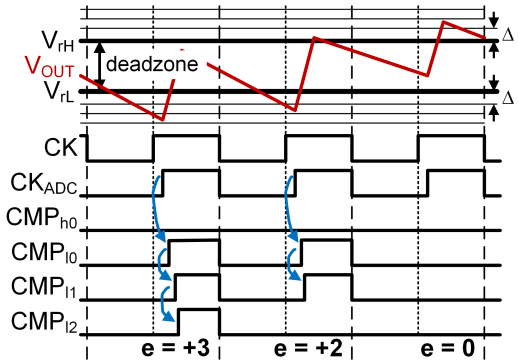

Fig. 10. Timing diagram of the ADC operation.

D. Digital Control

1) Conventional Control for SIMO: The two most common control schemes for an SIMO converter are: 1) time-multiplexed control (TMC) and 2) ordered-power-distributive control (OPDC).

As shown in Fig. 8, the TMC scheme supplies the inductor current to only one output during one switching cycle [7], [8]. This control can resolve the cross-regulation problem but generally suffers from the slow transient response and large output ripple [9]. Also, the input switches switch N times to support N outputs, increasing switching loss. Thus, it dissipates larger energy as N increases, especially for the light load condition of SoCs.

To avoid these problems, many recent works adopted the OPDC scheme [10]. Unlike the TMC scheme, the OPDC scheme supplies inductor current to all N outputs in one switching cycle. It can improve the transient response and ripple. In addition, it can achieve high PCE by reducing switching loss.

To implement the OPDC, earlier SIMO converters employ analog error amplifier circuits to perform the integral control [11]. Recent works also adopt continuous-time voltage comparators and analog-mixed-signal (AMS) circuits, such as a phase-locked loop [12]. However, such analog hardware draws a considerable amount of static current. Furthermore, its power consumption remains the same even if the SIMO output power scales. This makes it difficult to employ analog control hardware for ultra-LP applications.

2) Proposed Digital Control for SIMO: To address the limitations of analog control hardware, we have designed fully digital feedback control hardware, which consists of an ADC, a digital controller, and a switch control logic (i.e., digital-to-analog converter [DAC]) (see Fig. 3). It also makes the proposed converter scalable.

3) ADC Circuits: The proposed digital control hardware employs an ADC, which digitizes the voltage error between the reference voltages (V_{rH} and V_{rL}) and the output voltage (V_{OUT}). We have found that employing at least a 3-bit resolution is desirable for improving the transient response [27]. However, it requires eight clocked voltage comparators, greatly increasing control loss, especially during the steady state. Therefore, we need an LP ADC [28].

For this, we propose an LP synchronous domino flash ADC. Fig. 9 shows the schematics. Where it employs the same eight voltage comparators, only the two innermost comparators receive the clock signal directly. The rest six comparators are triggered only if the two innermost comparators find the output voltage (V_{OUT}) is outside of the deadzone (between V_{rH} and V_{rL}). Fig. 10 shows the timing diagram of the ADC operation. If the (minimum) output voltage is inside the deadzone ($e = 0$) at the steady state, the outer six comparators do not switch, which can reduce the clock power dissipation by 4×. Note that employing the deadzone incurs a dc output voltage error, but we can set the deadzone size and achieve our target voltage with a margin by setting V_{rH} and V_{rL}.

The ADC employs several different comparator circuits depending on V_{OUT}, which is the input voltage of the comparator. If the input voltage is less than the core voltage (1.2 V), we adopt a comparator in thin-oxide transistors [see Fig. 11(a)]. It follows the two-stage design. The first stage performs preamplification, generating V_{XN} and V_{XP} [27]. The regenerative feedback in the second stage amplifies the difference in V_{XN} and V_{XP} to the rail-to-rail differential output signals (LV and LVB).

On the other hand, we use different circuits for V_{OUT} for the I/O driver (1.8 V). In this case, we employ a comparator whose first stage has thick-oxide transistors [see Fig. 11(b)]. It uses a different clock signal CK_{HIGH}, which a level converter produces. However, since we only utilize V_{XN} and V_{XP} in the second stage, we can use the thin-oxide transistors with V_{DDL} as same as the comparators for the other three V_{OUT}s except for input transistors, thus reducing power consumption.

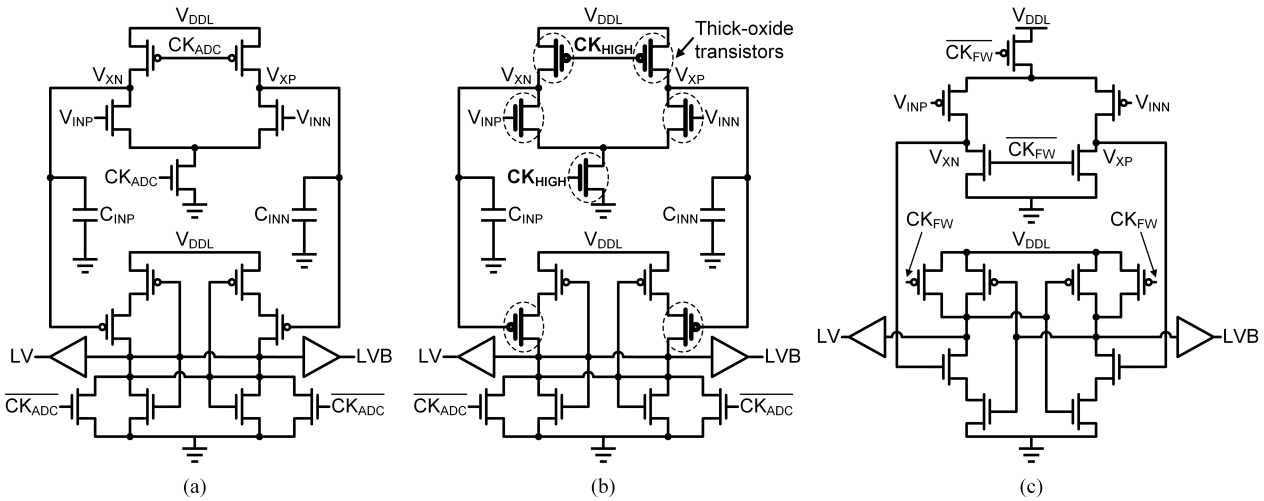

Fig. 11. Three types of clocked comparators for (a) low input voltage, (b) high input voltage, and (c) inductor current detection.

We also reduced the power overhead associated with reference voltage generation in the ADC circuits. The top (bottom) four comparators share only one reference voltage V_{rH} (V_{rL}). Still, we create input-referred offsets ($\pm\Delta$, $\pm 2\Delta$, and $\pm 3\Delta$) into the outer three comparators using a 5-bit binary programmable capacitor bank. We set Δ as 15–20 mV, and the capacitor bank can make up to $\pm 3\Delta$ offsets.

We also employ one additional comparator to check the inductor's current polarity. It compares the inductor terminal V_X with 0 V. Since the two input voltages are very low, we employ a pMOS–nMOS flipped topology [see Fig. 11(c)].

4) Control Laws for PWM Control: The proposed controller adopts the proportional-integral (PI) law. Because the proposed SIMO converter always operates in the DCM mode, the controller calculates three controller outputs: 1) duty cycle (dty); 2) four output switch turn-on time ($t_{\mathrm{ON},1}$ to $t_{\mathrm{ON},4}$); and 3) free-wheeling (FW) switching timing (t_{fw}) for the PWM operation. The PI control law consists of proportional (P) for improving transient performance and integration (I) parts for minimizing the steady-state error [29]. Here, the unit time (for 1 bit) is determined by the delay cell of the delay lines in the switch control logic explained in the following section. For example, the actual output switch turn-on time ($T_{\mathrm{ON},i}$) is as follows:

$$T_{\mathrm{ON},i} = t_{\mathrm{ON},i}[k] \cdot (\text{Delay cell unit delay}). \tag{2}$$

Fig. 12 shows the controller's PWM operation in two phases. In the first phase, when the controller's clock (CK) is low, the controller grabs the four domino ADC outputs (e_1–e_4) and the output of the inductor current detection comparator (e_{fw}) achieved from Phase 2 in the previous cycle. Here, e_{fw} means the inductor current polarity when the FW switch was turned on in the previous cycle. For example, if e_{fw} is 1, it means that the FW switch is turned on early before the inductor current goes below zero. Then, the controller calculates the duty cycle (dty) based on the following formulas:

$$\mathrm{dty}[k] = I_{\mathrm{dty}}[k] + K_{P,\mathrm{dty}} \cdot (e_1 + e_2 + e_3 + e_4) \tag{3}$$

$$I_{\mathrm{dty}}[k] = I_{\mathrm{dty}}[k-1] + K_{I,\mathrm{dty}} \cdot (e_1 + e_2 + e_3 + e_4) \tag{4}$$

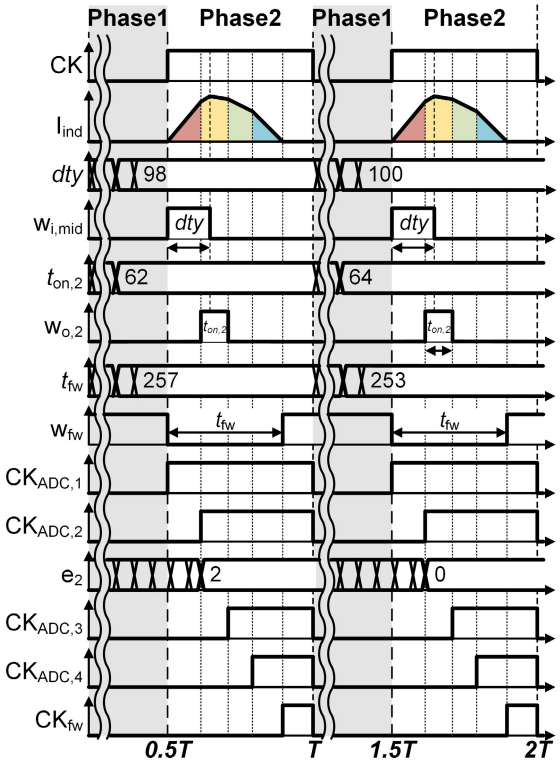

Fig. 12. Timing diagram of the proposed controller's PWM operation.

where k is the time index, $K_{P,\mathrm{dty}}$ is a proportional gain, and $K_{I,\mathrm{dty}}$ is an integral gain for the duty cycle.

In addition, the controller calculates the output switch turn-on time ($t_{\mathrm{ON},1}$ to $t_{\mathrm{ON},4}$) based on its own ADC output and the other three ADC outputs [11], [13]. The PI control law equations are as follows:

$$t_{\mathrm{ON},i}[k] = I_{\mathrm{ON},i}[k] + K_{P,\mathrm{ON}} \cdot e_{\mathrm{sum},i} \tag{5}$$

$$I_{\mathrm{ON},i}[k] = I_{\mathrm{ON},i}[k-1] + K_{I,\mathrm{ON}} \cdot e_{\mathrm{sum},i} \tag{6}$$

$$e_{\mathrm{sum},i}[k] = \alpha \cdot e_i[k-1] - \beta \cdot \left(\sum_{i \neq j} e_j[k] \right) \tag{7}$$

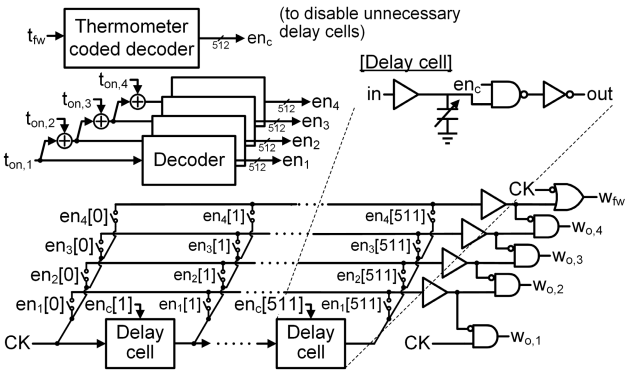

Fig. 13. Schematic of digitally controlled inverter-based delay lines.

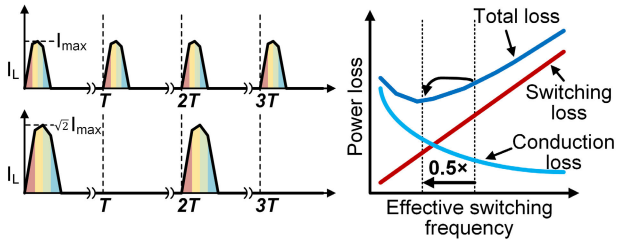

Fig. 14. Conduction and switching loss across the switching frequency.

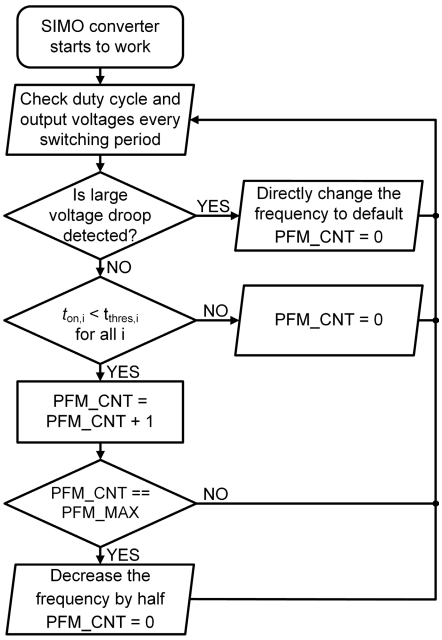

Fig. 15. Flowchart for the PFM operation.

where α and β are the positive weight parameters for error calculation, and $K_{P,\mathrm{ON}}$ and $K_{I,\mathrm{ON}}$ are the proportional and integral gains, respectively. The above equations calculate only the first three output switches' turn-on times.

The last output's switch turn-on time is determined by the FW switching timing (t_{fw}). The controller calculates the FW switching timing based on the following equation:

$$t_{\mathrm{fw}}[k] = I_{\mathrm{fw}}[k] + K_{P,\mathrm{fw}} \cdot e_{\mathrm{fw}} \tag{8}$$

$$I_{\mathrm{fw}}[k] = I_{\mathrm{fw}}[k-1] + K_{I,\mathrm{fw}} \cdot e_{\mathrm{fw}} \tag{9}$$

where $K_{P,\mathrm{fw}}$ and $K_{I,\mathrm{fw}}$ are the proportional and integral gains, respectively. Here, all the controller gains are parameters that can be programmable.

5) Switch Control Logic: In the second phase (when CK is high), the switch control logic grabs those calculation results and produces signals for input switches ($w_{i,\mathrm{top}}$, $w_{i,\mathrm{mid}}$, and $w_{i,\mathrm{bot}}$), output switches ($w_{\mathrm{o},1}$–$w_{\mathrm{o},4}$), and FW switch (w_{fw}).

Digitally controlled inverter-based delay lines generate these signals. Fig. 13 shows the schematics. The parameters (dty, $t_{\mathrm{ON},1}$–$t_{\mathrm{ON},4}$, and t_{fw}) (calculated in the first phase) are converted to the thermometer codes and fed into the delay lines. At first, the delay lines make the ADC's clock ($\mathrm{CK}_{\mathrm{ADC},1}$–$\mathrm{CK}_{\mathrm{ADC},4}$) and the inductor current detection comparator clock ($\mathrm{CK}_{\mathrm{fw}}$). Next, the XOR outputs of each adjacent two clock signals become the switches' final signals in the following cycle. The domino ADC is always triggered every cycle, even though the switch turn-on time is zero. In addition, the delay cells after the cell enabled for the FW switch are disabled to save power. The unit delay of these cells is configurable by the programmable capacitor bank, thus making the actual switch turn-on time (such as $T_{\mathrm{ON},i}$) properly.

The voltage of the inductor terminal connected to the output switches increases up to the maximum voltage of our loads (1.8 V). Therefore, the thick-oxide transistors must be used for output switches and the FW switch, specifically the pMOS transistor for $V_{\mathrm{I/O}}$ and the nMOS transistor for V_{CORE}, V_{BOOST}, and V_{MEM}. Thus, generated waveforms for those switches are fed into the level converter first, and these voltage swings increase from V_{DDL} to V_{DDH}.

As a result, the proposed SIMO converter draws a static current of as low as 733 nA. It includes the power switches' leakage current and the current of all blocks.

6) PFM Control: The proposed controller also performs PFM to improve PCE in the light load condition [30]. It decreases the switching frequency (CK) if the output power is small. Fig. 14 shows the optimal switching frequency changes as a function of the output power level.

To perform PFM, the controller monitors the output switch turn-on time ($t_{\mathrm{ON},1}$–$t_{\mathrm{ON},4}$). Suppose all of the turn-on times are small for several consecutive clock cycles. In that case, the controller assumes the load current level is low, thereby scaling the frequency by 2× using an embedded clock divider.

Fig. 15 shows the detailed flowchart of the PFM operation. It compares the calculated output switch turn-on time to a predetermined threshold value at every clock cycle. If every turn-on time is smaller than the threshold value, it increases PFM_CNT by 1; if not, it resets PFM_CNT to 0. If the PFM_CNT reaches a predetermined value PFM_MAX, the controller scales down its clock frequency by dividing the input clock. It can divide the input clock ($\mathrm{CK}_{\mathrm{UNDIV}}$) by up to 1024×. Note that the clock divider can generate a wide range of discrete levels of switching frequency while consuming a small amount of power.

7) Feedforward Control: If a digital processor wakes from the sleep mode, it can suddenly draw a large current, causing a voltage droop. Also, if the processor goes to sleep, the load

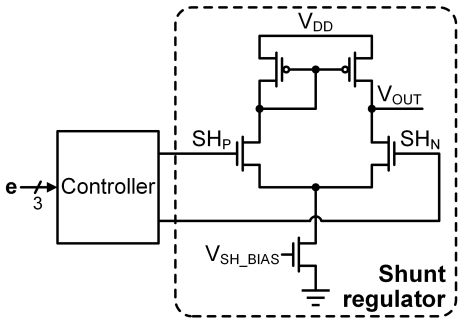

Fig. 16. Schematic of the feedforward controller and the shunt regulator.

current can abruptly decrease, causing a voltage overshoot. The feedback control is typically too slow to fully deal with such droops and overshoots. Therefore, we add feedforward control hardware. It can quickly enable a shunt regulator to provide or remove a charge to a supply rail if it detects a large voltage droop or overshoot.

Fig. 16 shows the proposed feedforward controller. Each controller receives the domino ADC output of the output. If the error value is larger than $+1$, that is, a voltage droop event, the controller sets SH_P high for a certain amount of time, supplying charge to V_{OUT} through the pMOS transistor. On the other hand, if the error value is smaller than -1, that is, a voltage overshoot event, it sets SH_N high, discharging V_{OUT}. We can control the amount of charge by setting $V_{\mathrm{SH\_BIAS}}$. If this voltage is too small, the shunt regulator provides a small current, thus it cannot improve the transient response. On the other hand, if the voltage is large, large current flows from the regulator and degrades the stability of the system. From the simulation and testing, we found that 0.5–0.6-V bias voltage shows the transient response improvement without any stability issues.

III. Integrated RISC-V Microprocessor

Fig. 17 shows the RISC-V processor we integrate with the SIMO converter in the test chip. The RISC-V processor can be a good candidate for verifying the performance of power management architecture. Many features are required for power management architectures to properly and efficiently operate the RISC-V processor. RISC-V processor's active mode and sleep mode power significantly vary, thus the dynamic range of power converters is very important. In addition, the large voltage droop can freeze the processor's operation, while the large overshoot can decrease the processor's efficiency.

The processor includes an RISC-V core, low-voltage i-cache, two 6T-SRAM-based memories (instruction memory (IMEM) and DMEM), a bus (AMBA), and an I/O module. The system is partitioned into dedicated four voltage domains for energy optimization: 1) $V_{\mathrm{I/O}}$ (1.8 V) for the I/O driver; 2) V_{CORE} (0.5–0.7 V) for the core, AMBA, and GPIO; 3) V_{BOOST} (0.8–0.9 V) for the i-cache; and 4) V_{MEM} (0.9–1.0 V) for the instruction and data memory.

The core is based on the open-source Ibex processor [31]. The Ibex is a 32-bit processor using the open RISC-V instruction set architecture (ISA) [32]. It has a two-stage pipeline: 1) instruction fetch (IF) stage and 2) instruction decode and execute (ID/EX) stage.

We have added an i-cache to the IF stage. The cache is based on the custom-designed ten-transistors (10T) SRAM (see Fig. 18 and [33]). We use ultralow leakage transistors for the bitcell to reduce leakage power. Also, the spatiotemporally wordline boosting technique is employed to compensate access time penalty of the ultralow leakage bitcell. The wordline boosting technique requires an additional voltage rail, which is 150–200 mV larger than the core voltage. The SIMO converter provides this voltage. The tag size is 23×128, and the data storage size is 64×128.

The processor also employs 8-kB IMEM and DMEM. We implemented them using the foundry SRAM. Among multiple types of SRAM, we choose the LP, low-leakage, single-port SRAM structure for LP. It requires a 1.2-V supply voltage and cannot use the core supply voltage (0.5 V). The SIMO converter provides this voltage.

In addition, the processor employs the ARM AMBA [34] to communicate with DMEM and GPIO. The GPIO and the I/O top module can support off-chip communication. Fig. 19 shows the block diagram of the I/O top block. We implemented an 8-bit GPIO register based on the open-source hardware [35]. The I/O voltage $V_{\mathrm{I/O}}$ is 1.8 V. We can program the GPIO direction.

IV. Measurement Results

A. Test-Chip Organization

The test chips for the proposed SoC have been prototyped in a 65-nm LP CMOS process. Fig. 20 shows the chip micrograph. The active area is 1.38 mm^2. The SIMO converter utilized a 10-μH off-chip inductor and a 10-nF flying capacitor. It also employs the decoupling output capacitors (20 nF) and the flying capacitors (10 nF) for the SC converters. The 20-nF output capacitor value for each output is chosen to integrate the capacitor on the chip. Considering the MIM capacitor density, four of the 20-nF MIM capacitors are sufficiently integrated into our active area (1.38 mm^2). However, to increase the testability of the chip, we use the off-chip capacitors. In addition, the chip-on-board (COB) method is utilized to reduce the parasitic effect.

B. Measurement Results

Fig. 21 shows the measured steady-state waveforms. All outputs produce the targeted voltages (in 0.5–1.8 V) with a ripple size of less than 10% of the output voltage. As the proposed converter operates in DCM mode, all the output voltage charging is done before the clock cycle is completed. Fig. 21 shows that the proposed SIMO converter works properly, and no critical charge balance problem is observed.

Fig. 22 shows the measured PCE across different conditions and settings. Fig. 22(a) shows the measured PCE across different output voltages. We fix the first output voltage ($V_{\mathrm{OUT},1}$) to 1.8 V and sweep the other three outputs. The peak PCE is 72.8% at $V_{\mathrm{IN}} = 4.2$ V and $V_{\mathrm{OUT},2-4} = 0.9$ V. This measurement includes the power consumption of the internal power rail generator. We compared these PCEs with the two

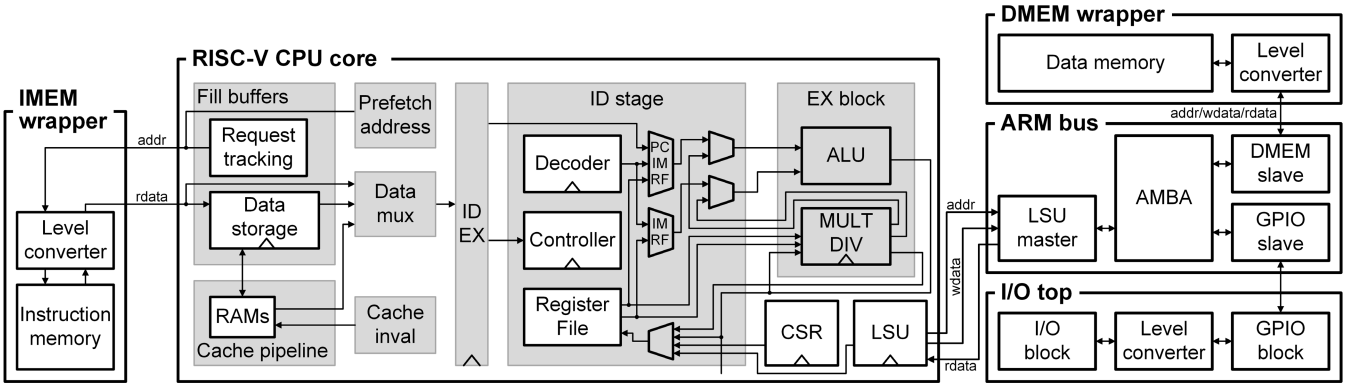

Fig. 17. Detailed block diagram of the RISC-V core and low-voltage i-cache, two 6T-SRAM-based memories, AMBA and GPIO blocks for communication, and off-chip I/O driver.

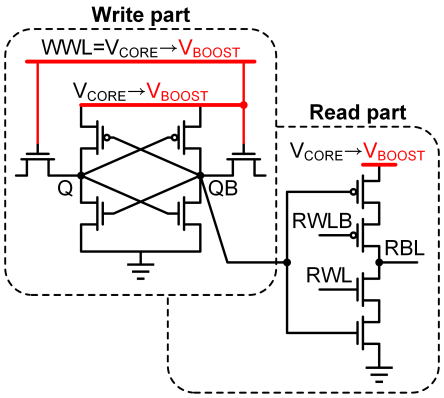

Fig. 18. Custom-designed 10T-based memory bitcell for the instruction cache.

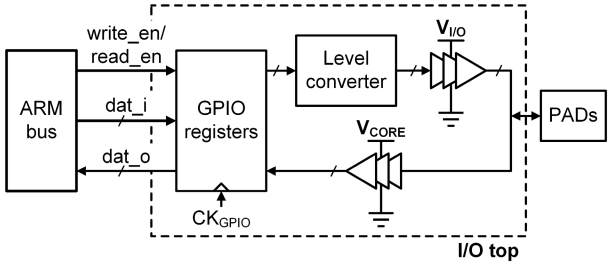

Fig. 19. Block diagram of the I/O top block.

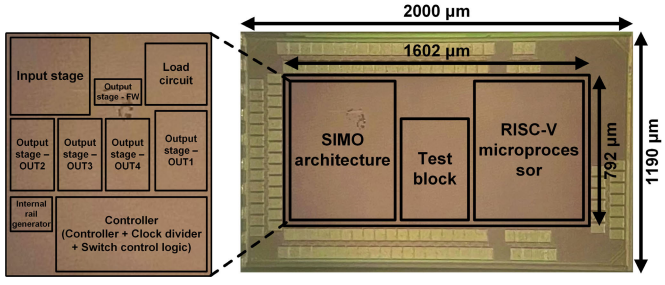

Fig. 20. Chip micrograph.

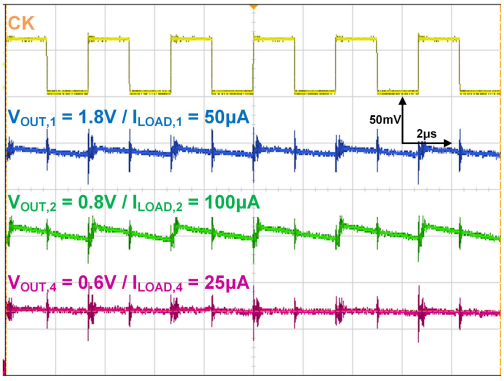

Fig. 21. Steady-state waveforms.

alternative power management architectures: 1) LDO only and 2) a buck converter followed by LDOs. We assume the PCE of the buck converter to be 95%. The PCE of the proposed SIMO converter is up to 46.3% better than the PCE of the LDO only and 20.6% better than the PCE of the buck-LDO architecture, respectively.

In addition, Fig. 22(b) shows the measured PCE across different load currents. The PFM technique enables the proposed SIMO to support a wide range of load currents from 0.8 μA to 0.8 mA at a reasonably high PCE of 56.0%–72.8%. Here, we only plot the PCE when the ripple size of all outputs is less than 10% of the output voltage. The minimum frequency increases when the load current increases. Finally, Fig. 22(c) shows the measured PCE across different V_{IN}. The proposed converter can function well across 3.8–4.4-V V_{IN}. As V_{IN} decreases, the PCE improves.

Fig. 23 shows the loss breakdown of the SIMO converter when it achieves the peak PCE. The conduction and switching losses account for 52.7% of the total loss. Also, the driver loss is 29.7% of the total loss. The controller only consumes 6.7% of the total loss.

We also measure the functionality of the PFM control. Fig. 24 shows the waveforms when all the load currents scale from 100 to 50 μA. After the output voltages become stable, the controller counts the SIMO cycles (PFM_CNT), where all the output switch turn-on times are less than a predetermined threshold value. Then, we observe that the controller accordingly decreases the switching frequency from 300 to 150 kHz. The PFM improves the PCE from 60.1% to 69.6%. We set the deadzone as 40 mV for the measurement. Here, the dc voltage shift exists at $V_{OUT,2}$, but the voltage is

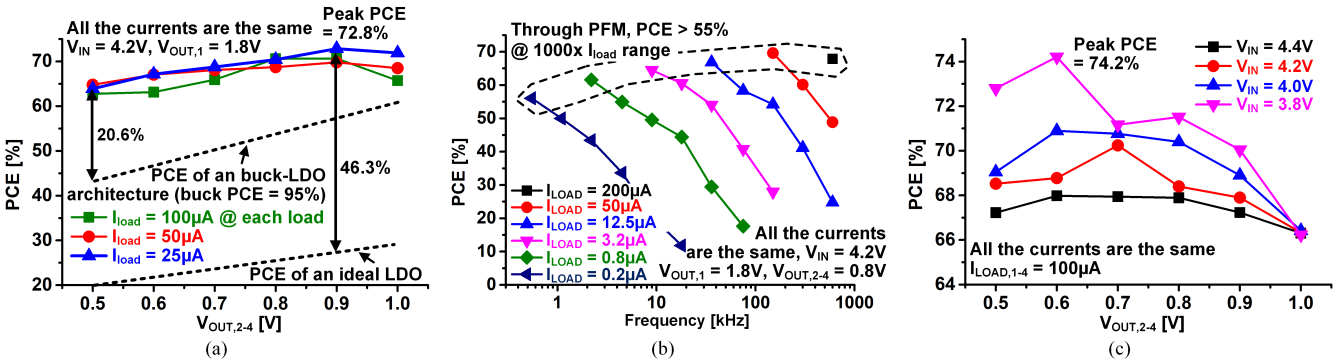

Fig. 22. Measured PCE across (a) different output voltages, (b) different load currents, and (c) different V_{IN}.

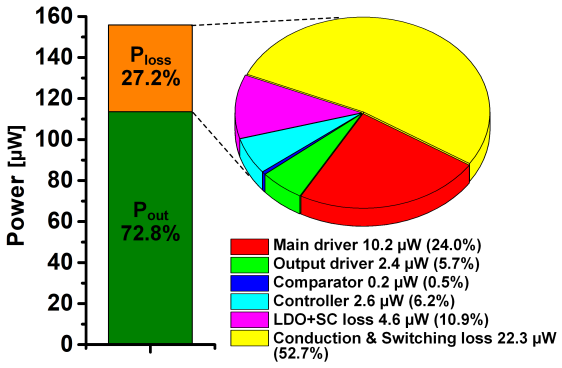

Fig. 23. Loss breakdown of the SIMO converter at the peak PCE.

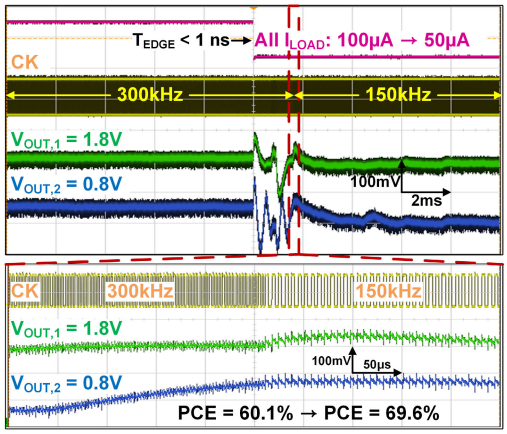

Fig. 24. SIMO output waveforms with enabling PFM.

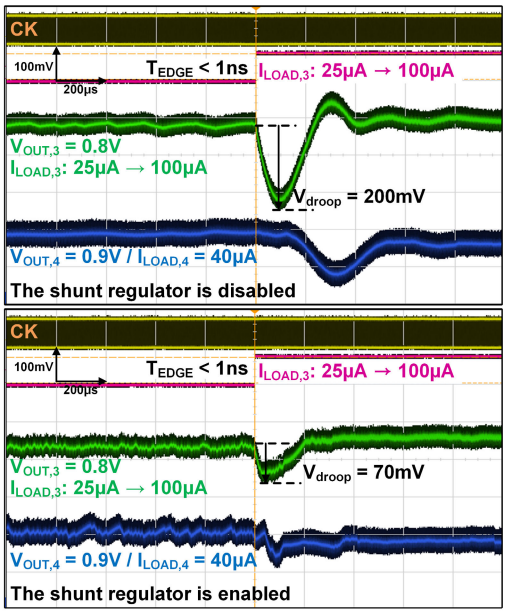

Fig. 25. Transient response waveforms with and without enabling the shunt regulators.

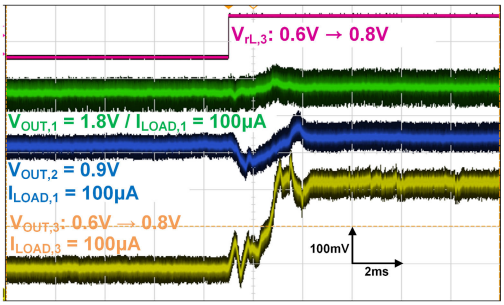

Fig. 26. DVS waveforms.

in the deadzone and the controller does not react to this shift. Also, it takes 300 cycles to settle the output voltages. Even though the duty cycle and four output switches turn on a time scale with the switching frequency, it requires additional time to reach the optimal values.

We also measure the transient performance of the converter. We measure the voltage droop for a load step from 25 to 100 μA in 1-ns edge time. As shown in Fig. 25, the feedforward control reduces the droop from 200 to 70 mV even with small output capacitors (20 nF). The recovery is completed in 60 cycles. Also, the converter exhibits no significant cross-regulation effects. In addition, we measure the performance of changing output voltage to support fast dynamic voltage scaling (DVS). Fig. 26 shows the measurement results, where it takes about 3 ms to increase $V_{OUT,3}$ from 0.6 to 0.8 V. The proposed PI control scheme is for simple and LP implementation. In addition to this, we lower the switching frequency to support the μA-scale load current. Thus, the support for transient response is not our primary goal and its transient performance is relatively low. To improve transient response time, new techniques such as strengthening feedforward controllers and utilizing adaptive gain control can be applied.

TABLE I
COMPARISON WITH LI-ION BATTERY-COMPATIBLE CONVERTERS

	This work	JSSC 2016 [5]	TPE 2018 [36]	JSSC 2019 [26]	JSSC 2020 [37]	TVLSI 2024 [19]
Process	65 nm	180 nm	180 nm	28 nm	180 nm	65 nm
Converter type	3-level SIMO buck	SC	SIMO buck	4-level buck	4-level buck	SIMO buck
Inductor	10 μH	N/A	10 μH	3 nH	220 nH	2.2 μH
Capacitor	20 nF	2.24 nF	10 μF	Not reported	1 μF	4.7 μF
Frequency	0.55-600 kHz	80-2700 kHz	1 MHz	200 MHz (Maximum)	2-10 MHz	1 MHz
V_{IN}	3.8-4.4 V	3.4-4.3 V	2.7-3.7 V	2.8-4.2 V	3.0-5.0 V	2.8-3.3 V
V_{OUT}	0.5-1.8 V	$>$ 0.45 V	1.0-1.8 V	0.6-1.2 V	0.3-1.2 V	0.8, 1.1, 1.8 V
External rails for drivers	No	No	No	Yes	No	No
# of outputs domains	4	1	4	1	1	3
V_{OUT} ripple	10% of V_{OUT}	Not reported	30 mV	12 mV	40 mV	Not reported
Load current/power[1]	0.66-960 μW 1454.5$\times$	300μA (Maximum)	40-330 mW 8.25$\times$	0.01-40 mW 4000$\times$	0.1-2.5 A 25$\times$	3.7-925 mW 250$\times$
Peak PCE @ V_{IN} & V_{OUT} (average)	72.8% @ 4.2 V & 1.05 V	72.0% @ 4.0 V & 0.9 V	73.0% @ 3 V & 1.45 V	78.0% @ 3.6 V & 1.0 V	90% @ 4.2 V & 1.1 V	95% @ 3.0 V & 1.23 V
Peak LDO-only PCE & improvement over it	25.0% 47.8% improvement	22.5% 49.5% improvement	48.2% 24.8% improvement	27.8% 50.2% improvement	26.2% 63.8% improvement	26.2% 54% improvement
Transient load step	75 μA (75% of Max I_{LOAD})	50 μA (16.7% of Max I_{LOAD})	100 mA (100% of Max I_{LOAD})	0.99 mA (8.3% of Max I_{LOAD})	Not reported	120 mA (63% of Max I_{LOAD})
Transient load regulation (Dynamic droop)	70 mV	Not reported	100 mV	Not reported	Not reported	55 mV
DVS support	Yes	Yes	No	No	Yes	No
Required time for DVS	3 ms	34 ms	Not reported	Not reported	1.5 μs	Not reported

[1] The load current/power where the PCE is higher than 50%.

TABLE II
COMPARISON WITH PRIOR PROCESSORS WITH INTEGRATED POWER MANAGEMENT ARCHITECTURE

	This work	JSSC 2009 [1]	JSSC 2017 [38]	JSSC 2021 [39]	JSSC 2022 [13]
Process	65 nm	65 nm	28 nm	28 nm	65 nm
Converter type	3-level SIMO buck	SC	SC	SC	SIMO buck
V_{IN}	3.8-4.4 V	1.2 V	1.0-1.8 V	1.8 V	1.8 V
V_{OUT}	0.5-1.8 V	0.3-0.6 V	0.45-0.9 V	0.4-0.8 V	0.6-1.0 V
Maximum conversion ratio (CR)[1]	8.4	4.0	4.0	4.5	3.0
# of voltage domains	4	1	1	3	4
Load domains	(1) I/O (2) RISC-V μP (3) i-cache (4) 2 SRAMs	(1) RISC μP & SRAM	(1) RISC-V μP & Vector accelerator & 3 SRAMs	(1) Cortex M0DS (2) ULP SRAM (3) HD SRAM	(1) Cortex M0 + MEM (2) Cortex M0 + MEM (3) SHA (4) FIR
Direct Li-ion batter input	Yes	No	No	No	No
Load power	0.66-960 μW 1454.5$\times$	10-250 μW 25$\times$	1.2-231 mW 192.5$\times$	0.4-411 μW 49$\times$	60-220 mW 3.7$\times$
Peak PCE @ V_{IN} & V_{OUT} (average)	72.8% @ 4.2 V & 1.05 V	75.0% @ 1.2 V & 0.5 V	88.7% @ 1.8 V & 0.9 V	76.3% @ 1.8 V & 0.55 V	84.1% @ 1.8 V & 0.87 V
Typical PCE @ CR (average)	65.0% @ CR=5.4	75.0% @ CR=2.4	88.7% @ CR=2.0	76.3% @ CR=3.27	84.1% @ CR=2.07
Typical buck-LDO PCE & improvement over it	41.2% 23.8% improvement	N/A	N/A	N/A	N/A
Typical LDO-only PCE & improvement over it	18.6% 46.4% improvement	42.0% 33.0% improvement	50.0% 38.7% improvement	30.6% 45.7% improvement	48.3% 35.8% improvement

[1] Maximum conversion ratio = V_{IN} / Minimum V_{OUT}.

Finally, we measure the converter's PCE when it supports the RISC-V processor as a load. As shown in Fig. 27, in the active mode, the processor runs at 1 MHz and consumes 31.2 μW. The SIMO converter consumes 16.8 μW, marking 65.0% PCE. In the sleep mode, the processor consumes 1.76 μW and the converter 1.09 μW, marking a PCE of 61.7%. The proposed techniques such as the digital control and PFM successfully maintain the PCE across the load current range.

C. Comparisons and Discussion

Table I compares the recent Li-ion battery-compatible power converters. Compared to relevant SIMO converters that utilize continuous comparators and high-power analog controllers, the proposed converter utilizes a fully digital controller with synchronous flash ADCs to minimize power consumption. Thus, this work demonstrates the lowest load power supported with a wide dynamic range. It also has a large number of outputs and shows a wide output voltage range. Finally, it shows sufficiently high PCE and supports both transient and DVS regulation.

In addition, Table II compares the recent processors with integrated power management. Most prior works integrating power management architecture and processors chose the conventional SC converter topology, so they cannot support a high and diverse conversion ratio, and their V_{IN} cannot

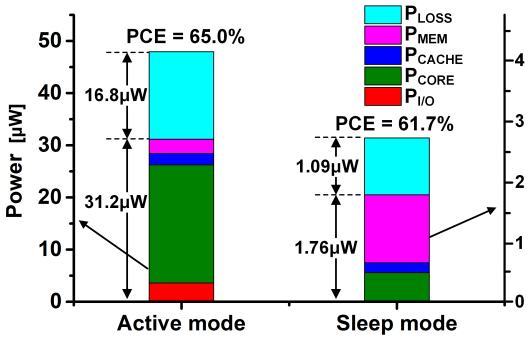

Fig. 27. PCE measurement of the RISC-V processor.

be increased. However, thanks to the three-level buck topology, the proposed work demonstrates the largest V_{IN}, the widest V_{OUT}, and the largest conversion ratio. It also has the widest load current range, thus fulfilling the power management need of the sub-mW processor at a sufficiently high PCE.

The measured PCE, however, seems to be lower than expected. Therefore, we try to investigate the root cause of the low PCE. Fig. 23 shows the switching and conduction loss and the driver loss are large, and we suspect that it is due to large parasitic capacitance and resistance from bond wires [36]. Especially, the parasitic capacitance from the bond wires cannot be negligible in LP operation. The voltage at the inductor terminals changes from 0 to $V_{\text{IN}}/2$ or $V_{\text{OUT},1}$ at every switching cycle. We estimated the parasitic capacitance of this node, including PADs and COB package, is ∼1 pF. Thus, the switching loss from two inductor terminals at 300-kHz clock frequency would be 2.5 μW.

In addition, we suspect that the thick-oxide transistors negatively affect the PCE. We found that the thick-oxide transistor does not offer good conductance. Stacking thin-oxide transistors might be a better choice to improve PCE [14]. It also makes the proposed converter work for 4.2-V batteries even if a deeper process does not provide thick-oxide transistors. Finally, we can also apply new techniques such as soft switching for PCE improvement.

V. Conclusion

This article presents a three-level SIMO converter integrated with the sub-mW 32-bit RISC-V processor. The SIMO converter supports a 1000× load current range (0.8 μA–0.8 mA) while achieving a PCE of 56.0%–72.8%. Supporting the integrated RISC-V processor, the converter achieves a PCE of 65.0% in the active and 61.7% in the sleep mode. The ideal buck-LDO (LDO-only) architecture would achieve the PCE of 41.2% (18.6%) for the same processor in active mode.

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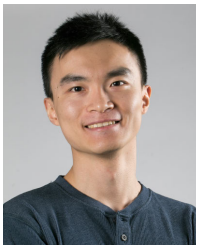

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