A Four-Element True-Time-Delay Slice-Based Receiver Array for FR3 Upper Mid-Band Wireless

Hesam Abbasi, *Graduate Student Member, IEEE*, Adam Slater, *Graduate Student Member, IEEE*, Foad Beheshti, *Graduate Student Member, IEEE*, Sreeni Poolakkal, *Graduate Student Member, IEEE*, and Subhanshu Gupta, *Senior Member, IEEE*

***Abstract*—A continuous beam angle resolution enables precise beam steering and prevents beam squinting, especially in dense environments where large arrays create narrow beams to maximize capacity. This work proposes a continuous beam angle reconfigurable four-element receiver (RX) for the FR3 frequency band. The implemented vector modulator (VM) phase-shifting mechanism is based on the slice-based RX for the coarse stage and phase-shifting polyphase filters (PPFs) in the local oscillator (LO) paths for the fine stage to overcome the limited phase resolution. The beamformer is equipped with current-mode true-time delay (TTD) units to further assist with better linearity performance and signal-to-noise ratio (SNR) improvement at the band edges. Fabricated in TSMC 65-nm complementary metal-oxide–semiconductor (CMOS), the prototype occupies an area of 1.65 mm^2, consuming 14 mA/element centered at 7.5 GHz. The measured maximum single-channel gain is 22 dB, with a minimum noise figure (NF) of 7.48 dB while having an $S_{11} < -10$ dB across 7.28–7.78-GHz input frequency span. A root mean square (rms) phase error of 0.76° is achieved while showing continuous phase shifting over 360°. The TTD units improve the beamformed down-converted 100-MHz wideband (WB) up to 1.5-dB gain at the band edge. Moreover, over-the-air (OTA) measurements show the reception of a single-tone signal at a 297.88-cm distance between RX and a horn antenna.**

***Index Terms*—Analog beamforming, continuous phase shift, polyphase filters (PPFs), true-time delay (TTD), vector modulator (VM).**

I. Introduction

IN THE unendingly shifting realm of wireless communications, the efficient spatial coverage of the beam space is critical to establish a robust high-throughput connection.

Received 20 December 2024; revised 7 April 2025 and 29 May 2025; accepted 29 June 2025. This article was approved by Associate Editor Minoru Fujishima. This work was supported in part by the National Science Foundation (NSF) Faculty Early Career Development Program Award (CAREER) under Award 1944688; in part by the Center for Design of Analog-Digital Integrated Circuits (CDADIC); in part by the Murdock Foundation; in part by the Air Force Research Laboratory as conducted through the Flexible Hybrid Electronics Manufacturing Institute, NextFlex under Grant FA8650-20-2-5506; and in part by Washington Research Foundation (WRF). *(Corresponding author: Hesam Abbasi.)*

Hesam Abbasi, Foad Beheshti, Sreeni Poolakkal, and Subhanshu Gupta are with the School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA 99164 USA (e-mail: hesam.abbasi@wsu.edu).

Adam Slater is with the Charles L. Brown Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, VA 22904 USA.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2025.3585532.

Digital Object Identifier 10.1109/JSSC.2025.3585532

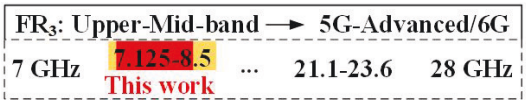
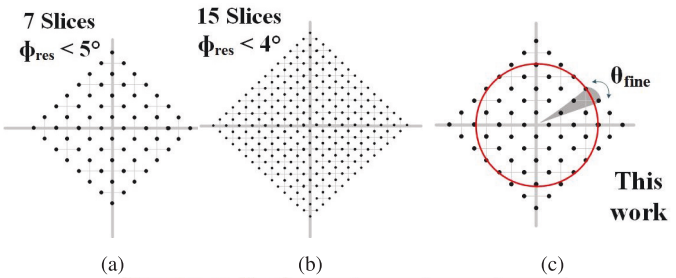


Fig. 1. Frequency spectrum allocation for the FR3 frequency band.

Recently, the FR3 band in the upper mid-band spectrum, as shown in Fig. 1, has emerged as a critical frequency range for enabling high-speed, low-latency connectivity in next-generation networks such as 6G and beyond. The FR3 band offers a balance between coverage and capacity, making it ideal for supporting a wide range of applications, from enhanced mobile broadband to massive machine-to-machine communications. However, congested networks, such as in dense urban environments, introduce challenges such as signal degradation, interference, and phase misalignment. To address these issues, analog and digital beamformers are gaining attention for their ability to leverage spatial signal processing to enhance signal directionality, spatial filtering, and improved link quality by dynamically controlling the phase at each element of the array [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13]. Digital arrays provide excellent phase accuracy, tunability (>12 bits), scalability, and signal-to-noise ratio (SNR), but at the cost of higher power consumption and area [9], [10], [11], [12], [13]. Analog beamformers, on the contrary, offer advantages in energy efficiency and area, making them a suitable choice for narrowband applications. However, they are limited by the lower phase resolution, flexibility, and SNR. In [7], continuous phase resolution was demonstrated, but its complexity and high power consumption make it unsuitable for low-size, weight, and power-cost (SWaP-C) applications. In [4], a 3.8° phase shift was realized, but the need for a quadratic increase in the number of phase shifters makes it less scaling-friendly.

Low-loss passive phase shifters have been successfully demonstrated in higher frequency bands [15] but are limited by in-band coverage and, more importantly, occupy a large area at lower frequencies [16]. Being scalable and less complex, baseband (BB) vector modulators (VMs) are thus highly attractive. In [5] and [6], slice-based VMs were demonstrated, showing wide adaptability, high linearity, low power, and inherent vector modulation capability with small phase control steps. However, the lack of continuous beam



Number of slices	3	7	15	31
Phase resolution	< 30°	5°~7°	~4°	~2°

(d)

Fig. 2. Phase constellation and phase resolution (Φ_{res}) in slice-based RX with (a) seven slices ($\Phi_{res} < 5°$), (b) 15 slices ($\Phi_{res} < 4°$), and (c) seven slices with continuous phase shift with fine-tuned LO phase shift θ_{fine} (this work) [14]. (d) Theoretically feasible Φ_{res}.

angle resolution yields suboptimal coherent signal combining for wide bandwidth (BW) applications, especially with a large number of antenna elements. Increasing the number of slices, the phase resolution gets better, i.e., down to 2°, as shown in Fig. 2(d) (theoretically feasible). However, at higher frequencies, mitigating quadrature mismatches in local oscillator (LO), filtering the foldable third- and fifth harmonics of the LO generated by the mixer switches, and the increase in complexity of clock distribution result in significant power consumption and area penalty. By realizing a dual-function tunable polyphase filters (PPFs) in the LO path [14], a process, voltage, and temperature (PVT)-resilient energy-area efficient approach was demonstrated that achieved continuous phase shift over 360°. However, only narrowband operation in a two-element configuration was demonstrated.

This work demonstrates the continuous beam coverage approach with a four-element wideband (WB) receiver (RX) array as shown in Fig. 3, alleviating SNR loss due to wide BW with a highly area- and energy-efficient architecture suited for FR3 bands. Analysis of phase shift true-time delay (TTD) compensation provides insights into not only alleviating beam-squint loss, but also compensating for antenna and trace mismatches and tuning over a wide aperture and BW. Detailed over-the-air (OTA) characterization is performed, embedding four patch antennas in the backplane of the assembled board to demonstrate WB beamforming with precision phase shifts.

Specifically, the following are the key contributions.

1) Section II presents the system design considerations with a highly energy- and area-efficient architecture enabling phase shifter and TTD (PS–TTD) compensation with a continuous beam coverage. In addition, detailed qualitative and quantitative comparisons of state-of-the-art phase-shifter architectures with the coarse-fine phase-shifting mechanism integrated with fine LO-based phase tuning and TTD are presented, which influences accurate calibration.
2) Section III presents the implementation details for the unit slice and the clock distribution in the slice-based array.
3) Section IV presents an exhaustive analysis of the impact of PS–TTD compensation on RX characteristics, including gain, noise figure (NF), and linearity.
4) Section V presents a comprehensive measurement setup and validation for OTA characterization leveraging PS–TTD calibration in the proposed architecture, overcoming issues with gain droop, and consequently loss in SNR at the band edge. The results demonstrate efficient methods for array calibration necessary for precision beamforming, incorporating antenna and trace mismatches using integrated TTD elements.
5) Finally, Section VI concludes this article with a discussion on future works.

II. System Design of the Slice-Based Array Architecture

This section presents an overview of the system design considerations for the proposed TTD slice-based RX architecture, followed by implementation details of the system subcircuits in Section III.

A. Phase Shift and TTD Compensation in Arrays

The conventional analog beamforming arrays, as shown in Fig. 4(a), using solely phase shifters for time delay approximation, exhibit beam-squint errors. These errors present as frequency-dependent beam direction shifts, leading to inaccuracies in beam steering and positioning. Here, the gain is affected by the frequency, the number of elements, and the angle-of-arrival (AoA). The normalized beamforming gain (NBFG) for such a system is shown in Fig. 5 for three different numbers of elements of 4 and 64 versus frequency and three different AoAs of $\theta_1 = 7°$, $\theta_2 = 15°$, and $\theta_3 = 30°$. These results illustrate that the larger number of elements and higher AoA limit the phased-array's BW. On the other hand, only implementing TTD to compensate for the element delay, as shown in Fig. 4(b), still results in phase imperfection [5], [17], [18]. In contrast, a phase shift (either at radio frequency (RF), LO, and BB) with a BB TTD not only leads to a perfect delay compensation but also comes with several benefits including better area and power, ease of digital reconfigurability, and is mathematically equivalent to the RF TTD as illustrated in Fig. 4(c) [19], [20], [21], [22], [23], [24]. In this work, each RX provides coarse phase shifts, controlled by 12 serial peripheral interface (SPI) bits, fine phase shifts controlled by PPF digitally controlled currents, and tunable BB TTD units controlled by another 10 SPI bits.

B. Phase Shift and TTD Compensation Mechanism

Fig. 6 conceptually illustrates the phase shifter and TTD (PS–TTD) mechanism for linear array in this work. Here, an arbitrary AoA of θ makes each element experience an inter-element delay of τ_{unit} with respect to the previous element. This contributes to a delay of $\tau_{RF,i} = (i-1)\tau_{unit}$ for the ith element, $i = 1, \ldots, n$, resulting in the RF signal $S_{RF,i}(t) = \cos[\omega_{RF}(t-\tau_{RF,i})]$ for that element. On the other hand, applying a phase shift of $\phi_{LO,\,i}$ on the LO path of the i_{th} element gives

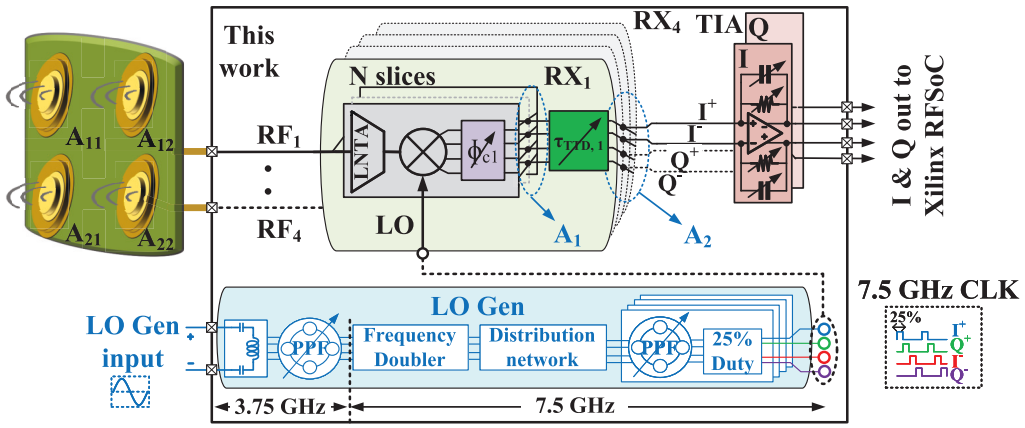


Fig. 3. Proposed four-element RX array implementing slice-based combination (A_1) followed by TTD delay compensation, (A_2) beamforming, and TIA with the on-chip LO distribution including frequency-doubling, distribution, and quadrature generation. ϕ_{c1} is the coarse phase and $\tau_{TTD,1}$ is the TTD for the first RX.

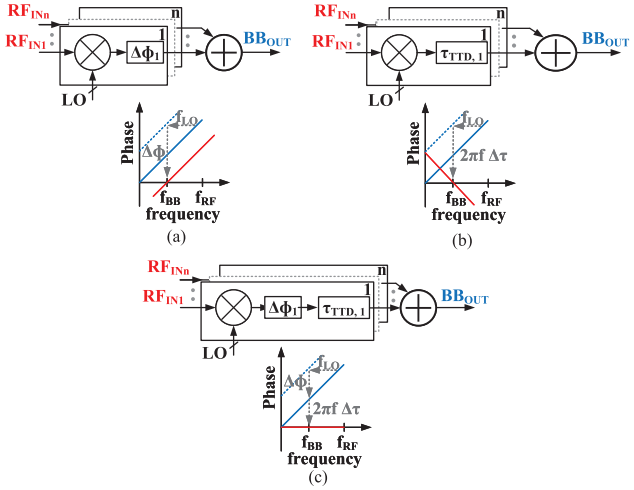


Fig. 4. Delay compensation with (a) phase shift, (b) time delay, and (c) phase shift with time delay.

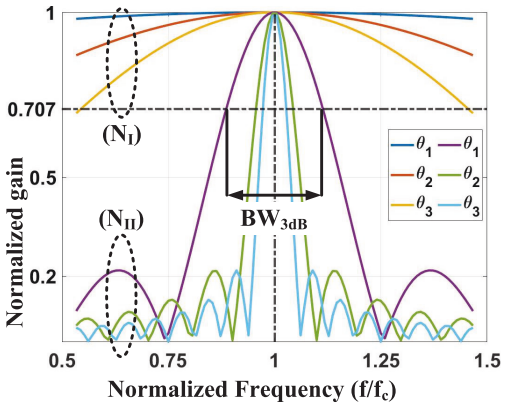


Fig. 5. NBFG for two different numbers of elements of $N_I = 4$ and $N_{II} = 64$ considering three AoAs of $\theta_1 = 7°$, $\theta_2 = 15°$, and $\theta_3 = 30°$.

the LO signal of that element as $S_{LO,i}(t) = \cos(\omega_{LO}t + \phi_{LO,\,i})$. Therefore, the BB signal resulting from the down-conversion is extracted as follows:

$$S_{BB,i}(t) = \text{LPF}\left\{S_{RF,i}(t) \times S_{LO,i}(t)\right\}$$

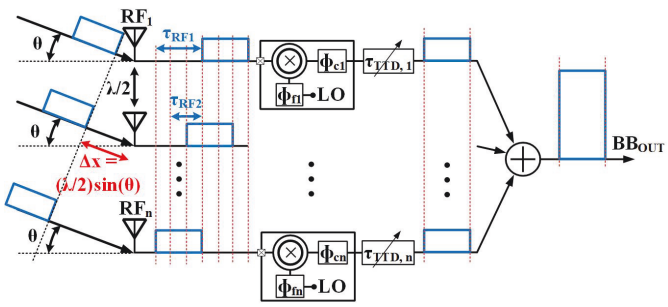


Fig. 6. RX model with phase and delay units.

$$\begin{aligned} S_{BB,i}(t) &= \text{LPF}\left\{\cos\left[\omega_{RF}\left(t-\tau_{RF,i}\right)\right] \times \cos\left(\omega_{LO}t + \phi_{LO,\,i}\right)\right\} \\ &= \frac{1}{2}\cos\left[\omega_{RF}\left(t-\tau_{RF,i}\right) - \left(\omega_{LO}t + \phi_{LO,\,i}\right)\right] \\ &= \frac{1}{2}\cos\left[\left(\omega_{RF}-\omega_{LO}\right)t - \omega_{RF}\tau_{RF,i} - \phi_{LO,\,i}\right]. \end{aligned} \tag{1}$$

By replacing $\omega_{RF} - \omega_{LO} = \omega_{BB}$ and $\omega_{RF} = \omega_{LO} + \omega_{BB}$, the above equation can be rearranged as below

$$\begin{aligned} S_{BB,i}(t) &= \frac{1}{2}\cos\left[\omega_{BB}t - \left(\omega_{LO}+\omega_{BB}\right)\tau_{RF,i} - \phi_{LO,\,i}\right] \\ &= \frac{1}{2}\cos\left[\omega_{BB}\left(t-\tau_{RF,i}\right) - \left(\omega_{LO}\tau_{RF,i} + \phi_{LO,\,i}\right)\right] \end{aligned} \tag{2}$$

where it shows the RF delay $\tau_{RF,i}$ and the LO phase shift $\phi_{LO,i}$ directly translate to BB with positive and negative signs, respectively. This is while a new phase shift of $\omega_{LO}\tau_{RF,i}$ is also added to the BB due to the mixing behavior. Applying a unique TTD for each element in the BB results in the following delayed BB signal:

$$\begin{aligned} S^{d}_{BB,i}(t) = \frac{1}{2}\cos\Big[&\omega_{BB}\left(t-\tau_{RF,i}-\tau_{TTD,i}\right) \\ &- \left(\omega_{LO}\tau_{RF,i} + \phi_{LO,\,i}\right)\Big]. \end{aligned} \tag{3}$$

In the above equation, $\tau_{RF,i} + \tau_{TTD,i} = \tau_{BB,i}$ and $\omega_{LO}\tau_{RF,i} + \phi_{LO,i} = \phi_{BB,i}$ are, respectively, the total BB delay and total BB phase shift each consisting of two terms wherein both the first term is inherent and the second term is manually applied. Therefore, to constructively combine the delayed BB

TABLE I
QUALITATIVE COMPARISON OF HYBRID PHASE SHIFTING ARCHITECTURES

Phase Shifting	**RF Path Loss**	**LO Power & Distribution**	**Area**	**Implementation Complexity**	**# Blocks (Array)**	**Overall Power**
RF	High	Low	Low	Moderate	Low	Moderate
LO	Low	High	High	High	High	High
IF/BB	Low	Moderate	High	Low	High	Low
(This work) LO+IF	Low	Moderate	Low	Moderate	Moderate	Moderate

TABLE II
COMPARISON TO STATE-OF-THE-ART PHASE SHIFTERS

Work	ISCAS'22 [25]	RFIC'18 [26]	TCAS-I'20 [27]	TMTT'24 [28]	TCAS-I'24 [29]	JSSC'24 [30]	**This work**
Process	65nm	65nm	65nm	40nm	40nm	130nm SiGe	**65nm**
Method	VM	Resonance + VM	STPS + VM	Hybrid + VM	VM	Hybrid + VM	**VM + PS-PPF + TTD**
Area(mm^2)	NR	0.45[1]	0.14[1]	0.11	0.056[1]	NR	**0.013(PPF) + 0.067(RX)**
RF frequency(GHz)	23.4-28.5	24	56-66	22.5-33.5	90-98	23	**7.28-7.78**
Phase resolution(°)	1.4	0.04	5.625	5.625	5.625	NR	**Continuous**
Power(mW/element)	NR	147.5[2]	47.6[2]	15	135[2]	NR	**22**

[1] Estimated based on die photo; [2] Includes other receiver/transmitter elements; NR - Not Reported

signals from different elements, they need to have the same amount of delay and phase shift. The very first solution for this fundamental challenge is to make the delay and phase of each element equal to those of the last element in the linear array which has the largest inherent delay and phase shift of $(N-1)\tau_{\text{unit}}$ and $(N-1)\omega_{\text{LO}}\tau_{\text{unit}}$, respectively, as below

$$\begin{cases}\tau_{\text{BB,i}} = \tau_{\text{BB,N}} \\ \phi_{\text{BB,i}} = \phi_{\text{BB,N}}\end{cases} \Rightarrow \begin{cases}\tau_{\text{RF,i}} + \tau_{\text{TTD,i}} = \tau_{\text{BB,N}} \\ \omega_{\text{LO}}\tau_{\text{RF,i}} + \phi_{\text{LO,i}} = \phi_{\text{BB,N}}\end{cases} \tag{4}$$

$$\Rightarrow \begin{cases}(i-1)\,\tau_{\text{unit}} + \tau_{\text{TTD,i}} = (N-1)\,\tau_{\text{unit}} \\ (i-1)\,\omega_{\text{LO}}\tau_{\text{unit}} + \phi_{\text{LO,i}} = (N-1)\,\omega_{\text{LO}}\tau_{\text{unit}}\end{cases} \tag{5}$$

$$\Rightarrow \begin{cases}\tau_{\text{TTD,i}} = (N-i)\,\tau_{\text{unit}} \\ \phi_{\text{LO,i}} = (N-i)\,\omega_{\text{LO}}\tau_{\text{unit}}.\end{cases} \tag{6}$$

According to the above, in a four-element array, the amount of BB TTD and LO phase shift for each element to align the signals in BB are as follows:

$$\begin{cases}\tau_{\text{TTD,1}} = 3\tau_{\text{unit}}, \tau_{\text{TTD,2}} = 2\tau_{\text{unit}} \\ \tau_{\text{TTD,3}} = 1\tau_{\text{unit}}, \tau_{\text{TTD,4}} = 0 \\ \phi_{\text{LO,1}} = 3\omega_{\text{LO}}\tau_{\text{unit}}, \phi_{\text{LO,2}} = 2\omega_{\text{LO}}\tau_{\text{unit}} \\ \phi_{\text{LO,1}} = 1\omega_{\text{LO}}\tau_{\text{unit}}, \phi_{\text{LO,4}} = 0.\end{cases} \tag{7}$$

The spacing between the linear antenna elements is $d = (\lambda/2)$ resulting in a delay of τ_{unit} as below

$$\tau_{\text{unit}} = \frac{d\sin(\text{AoA})}{c} = \frac{\frac{\lambda}{2}\sin(\text{AoA})}{\lambda f} = \frac{\sin(\text{AoA})}{2f}. \tag{8}$$

Therefore, in our system, implementing tunable $\phi_{\text{LO,i}} = \phi_{\text{c,i}} + \phi_{\text{f,i}}$ and tunable BB-TTD units in each RX chain helps align all the signals before the adder, leading to perfect signal amplification, i.e., BB_{OUT} shown in Fig. 6, and addresses the problem of beam squinting.

C. Design Considerations With Coarse-Fine PS and TTD

The proposed TTD slice-based RX array is shown in Fig. 3. By implementing the constant-Gm VM, we realized the phase-shifting mechanism for the RX. This approach provides high phase accuracy by consistently maintaining a constant total transconductance across all the phase constellation points [6]. The beamformer chip includes four RXs and a clock generation circuitry. Each RX has four tunable TTD units for the differential quadrature currents placed before the transimpedance amplifier (TIA). All four are controlled with the same 10 bits from the on-chip SPI, which is not shown in the figure for better readability. Finally, the currents are summed at the TIA inputs, and the differential quadrature output voltages are ready for further processing on the Xilinx SoC board. Each RX incorporates two phase shift mechanisms realizing coarse and fine phase shifts to cover 360°, as depicted in Fig. 2(c). The coarse phase tuning is realized by orthogonal current summation in each slice-based RX with seven slices chosen to alleviate clock distribution complexity (A_1 in Fig. 3). The slices, shown in Fig. 7, are binary-weighted, which means that seven slices are broken into three groups of one, two, and four slices, each group controlled using one SPI bit. Then, the currents are summed at the TTD unit input, where it also acts as a low-pass filter (LPF), as will be shown later in (9), which helps with the folded harmonics issue mentioned earlier. The maximum magnitude of each output differential quadrature current is seven times the magnitude of a unit-slice output current. The total number of feasible phase points is $2^{2\times3}$ [5]. In this case, the quadrature output currents of the total number of slices in one quadrant are $I = \alpha I_s$ and $Q = \beta I_s$, where $0 \le \alpha,\beta \le 2^3 - 1$, while $\alpha + \beta = 2^3 - 1$, and I_s is the unit-slice output current, the achievable coarse phase shift can be expressed as $\phi_{\text{coarse}} = \tan^{-1}(\beta/\alpha)$. The achievable phase resolution with seven slices is <7°, as shown in the table in Fig. 2(d). The LO circuit, shown in Fig. 3 adapted from the authors' prior work in [14], begins with a balanced frequency-doubler before distribution, which includes a tunable PPF for robust operation over PVT. In addition, there is a tunable PPF for LO phase shifting and a 25% duty cycle (DC) conversion local to each RX element as discussed in Section III. Table I provides a qualitative comparison of state-of-the-art phase-shifters' complexity, while Table II presents deeper insights

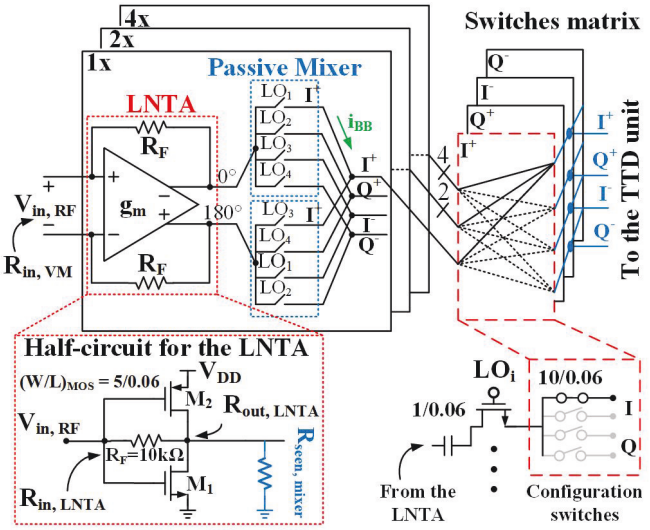


Fig. 7. Unit-slice architecture including LNTA, four-phase mixer, and configuration switches.

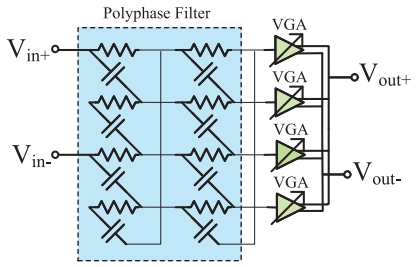


Fig. 8. VM with PPF for quadrature generation.

into the quantitative comparison to recent state-of-the-art. These architectures include resonant structures, switched-type phase shifters (STPSs), VM, hybrid couplers, and TTD units, often combined for broader performance. Resonant structures alone offer a limited phase shift range but can achieve a full 360° range when combined with quadrature-selection stages [26]. Quadrature-selection or polarity-inverting stages can be considered subsets of VM architectures, which leverage multi-phase signals and variable-gain amplifiers (VGAs) to realize phase shifting through vector scaling and summation [25], [29]. STPSs use arrays of switched passive elements for fine-tuning, sometimes combined with quadrature selection for coarse adjustments [27]. Similarly, hybrid couplers alone have limited range and require cascading or combination with other methods to achieve a full 360° shift [28], [30]. Many recent transceiver phase shifters integrate quadrature generators, as illustrated in Figs. 8 and 9. While resonant and hybrid coupler architectures generally occupy large areas even at millimeter-wave (mmW) frequencies [26], [28], VM architectures using VGA arrays typically suffer from higher power consumption [28]. In contrast, the architecture proposed in this work uses a low-power, coarse-tuning VM approach, transferring fine-tuning capability into the PPF as described in [14]. This strategy effectively reduces both area and power consumption. In addition, integrated TTD units are included to significantly mitigate beam squint.

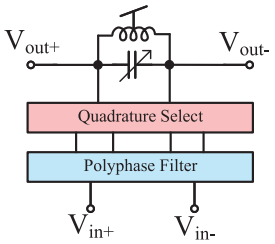


Fig. 9. Quadrature selection combined with a resonant structure to achieve a wide shifting range.

III. Slice-Based Array Circuit Implementation

A. Unit-Slice Implementation

Fig. 7 shows the unit-slice implementation and its RX configuration. At first, the input RF voltage is transformed to current and amplified by the self-biased low-noise TIA (LNTA). Then, the currents are down-converted through the passive mixers. The mixers' switches are controlled using 25% DC LO signals. The slices are binary-grouped into one, two, and four slices, and then their currents are summed in the TTD unit's input to perform vector modulation. For simplicity, only the I^+ path is shown here. Current-mode RXs with 25% DC LO achieve superior linearity performance compared with the voltage-mode RXs [31] provided the impedance at each RX node is low, allowing the signal currents to flow through to the following stage. The single-ended LNTA circuit, shown in Fig. 7, has been optimized for noise performance. R_F is selected to be large (10 kΩ) to minimize the noise voltage and maximize LNTA gain. With the matched input (the input-matching criteria are discussed later), the LNTA's output resistance is $R_{\text{out, LNTA}} \approx ((R_F/2) \parallel R_{\text{out,M1}} \parallel R_{\text{out,M2}})$, which should be significantly larger than the mixer input impedance, $R_{\text{in, mixer}}$, to maximize signal transfer to the next stage.

B. Proposed TTD Unit

TTD techniques become attractive in these systems, as mentioned earlier, allowing time-domain delays to compensate for frequency-dependent phase variations [20]. BB TTD is preferable over RF because of lower losses [12], [20], [32]. Combining the BB TTD with continuous phase shifting leads to optimal delay compensation independent of the BB frequency [19]. We illustrated this in Fig. 6. As elaborated in Section II-A, by tuning $\phi_{\text{c,i}}$, $\phi_{\text{f,i}}$, and $\tau_{\text{d,i}}$ for each RX, the inter-element delay can be compensated in the entire frequency band independent of the BB frequency [19], [20].

Fig. 10 shows the proposed current-mode TTD unit cell. As shown in (9), the TTD cell behaves like an LPF, which can be used to suppress unwanted harmonics and out-of-band noise

$$H(s) = \frac{I_{\text{out}}}{I_{\text{in}}} = \frac{1}{1 + C_{\text{Tune}} \cdot R_{\text{in,TTD}} \cdot s}. \tag{9}$$

The group delay can further be defined as

$$\tau_g = -\frac{\partial \angle H(\omega)}{\partial \omega} = \frac{R_{\text{in,TTD}} \cdot C_{\text{Tune}}}{1 + \left(R_{\text{in,TTD}} \cdot C_{\text{Tune}} \cdot \omega\right)^2} \tag{10}$$

where $R_{\text{in,TTD}} \approx 1/(g_{m1} + g_{m7})$ and $C_{\text{Tune}} = C_1 + C_2$. The group delay is approximately constant if $(R_{\text{in,TTD}} \cdot C_{\text{Tune}} \cdot \omega)^2 \ll 1$. The

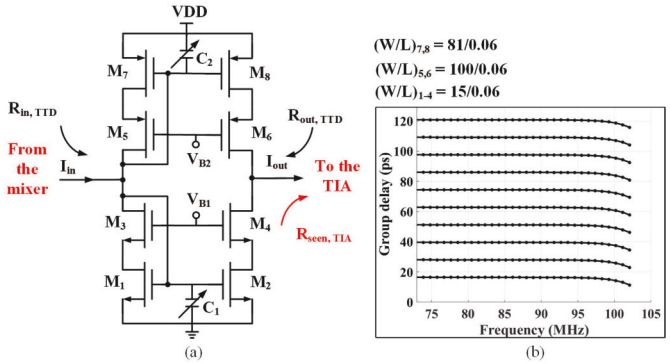


Fig. 10. (a) Current-mode tunable continuous TTD unit cell. (b) Simulated unit delay range/steps.

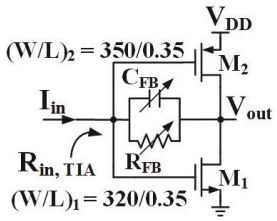


Fig. 11. Self-biased TIA.

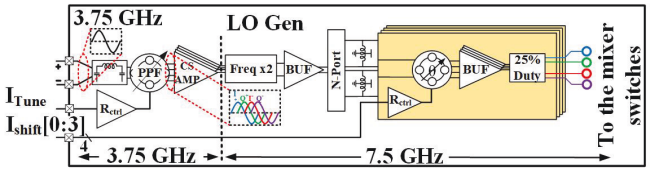


Fig. 12. Clock generation architecture. LO signal processing includes frequency-doubling, distribution, quadrature generation, fine phase-shifting, drivers, and 25% DC conversion.

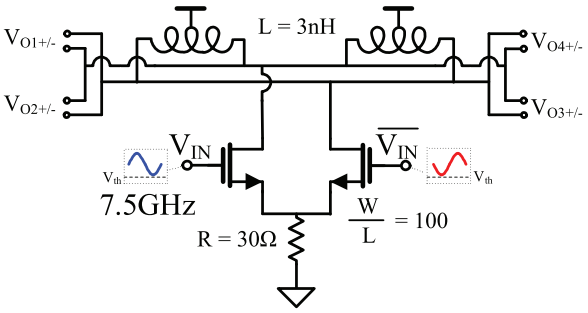


Fig. 13. Clock distribution schematic[14].

TTD unit group delay simulation results in Fig. 7 (inset) show that the maximum achievable delay is 120 ps with a resolution step of 11.6 ps, which is achieved with a 10-bit thermometer code provided by the SPI to tune the capacitors C_1 and C_2. C_{Tune} increment is 50 fF, and $R_{\text{in,TTD}}$ is designed to be 245 Ω, as will be explained in Section III-C. To address the BW delay tradeoff, multiple TTD units with smaller individual delays can be cascaded. This approach reduces the TTD's input capacitance, thereby increasing the BW. However, it is important to consider that cascading stages can incur greater insertion loss, complicate routing, and amplify mismatch errors.

C. TIA Circuit

Self-biased gm-cells are used to realize the TIA, as shown in Fig. 11. A common-mode feedback circuitry is used to fix the DC of the output at 500 mV. Using a 3-bit control to tune C_{FB} and R_{FB}, the TIA gain and BW can be reconfigurable. The open-loop gain of the TIA is large enough that its input resistance, $R_{\text{in,TIA}}$, would be much lower than the preceding stage.

D. Clock Generation

The clock generation circuit provides fine-tuned phase shifting, complementing the coarse vector modulation and TTD in the RX path, allowing for continuous beam angle resolution with a range of 360°. The clock signals must provide low jitters to ensure high image-rejection ratio (IRR) and, hence, adequate error vector magnitude (EVM) [33]. This is implemented using a phase-shifting quadrature generator and LO signal processing circuit detailed in [14]. The LO architecture, shown in Fig. 12, achieves a low quadrature mismatch with an IRR of >58 dB, consuming <0.25 mW, and simulated phase noise of <-130 dBc/Hz at a 10-kHz offset. The design leveraged from [14] also includes circuits for frequency-doubling, clock distribution, LO drivers, and 25% DC conversion. The input reference clock at 3.75 GHz is first converted into quadrature using a PPFs followed by a push–push frequency-doubler, achieving a balanced frequency-doubled output. Distributing the clock signal to each RX in the chip is achieved with a current-mode N-port. The N-port is terminated with inductors for inductive peaking, reducing the gain requirements of the frequency-doubler. The clock distribution circuit in [14] is shown in Fig. 13. This circuit distributes the LO as a differential sine wave through a current-mode T-network, which is scalable to 2^N elements. The distribution layout is shown in Fig. 14. There is a quadrature generator local to each RX element. The layout of the final quadrature transmission network is illustrated in Fig. 15. Fig. 16 depicts the phase-shifting quadrature generator that acts as a fine-tuned phase shifter and avoids the NF degradation associated with adding another phase shifter to the signal path. The phase control circuit is also shown in Fig. 16 (inset). As the reference current through M_{REP} changes, the op-amp forces the voltage across the replica to track V_{REF}, which alters the second-stage PPFs pole, providing fine phase shift.

IV. Circuit Analysis

This section briefly analyzes the RX array, including input matching, conversion gain, noise, and linearity performance.

A. Input Matching

Passive mixers are transparent, which means that the BB impedance, i.e., $Z_{\text{in,TTD}}$, is up-converted to the LNTA output.

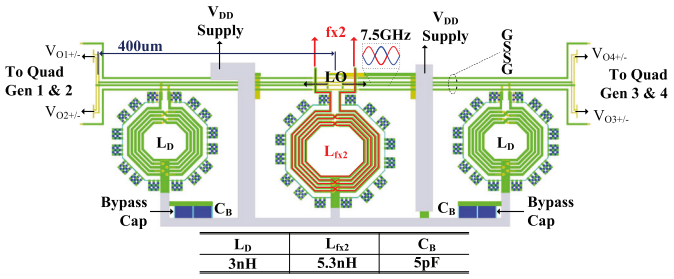


Fig. 14. Clock distribution layout integrated with frequency-doubler load.

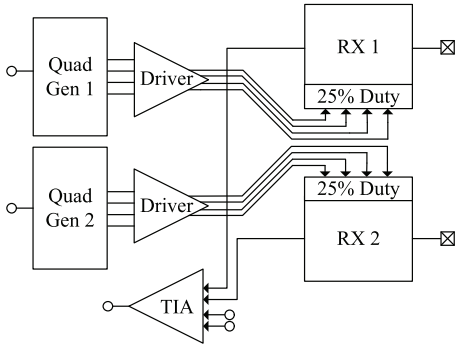


Fig. 15. Quadrature transmission floor plan [14].

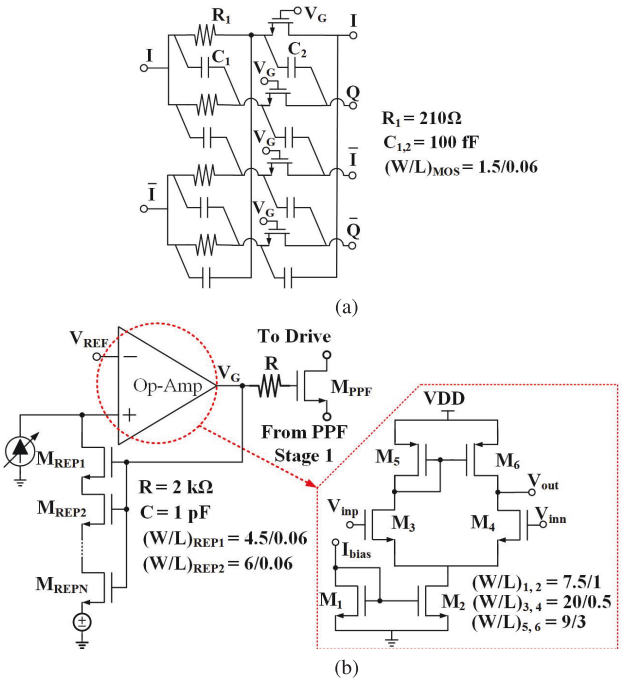


Fig. 16. (a) Multi-stage PPFs for both quadrature generation and phase shifting. Continuous control is achieved with FETs operated in triode, replacing the resistors that are traditionally in the second stage. (b) Error correction opamp.

With seven slices, the impedance seen before the mixer switches, shown in Fig. 7 (inset), is

$$R_{\text{seen,mixer}} = \left(\frac{\text{sinc}^2\left(\frac{1}{M}\right)}{M} R_{\text{BB}} \right) \tag{11}$$

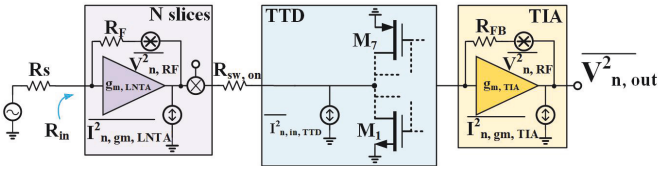


Fig. 17. Equivalent circuit for noise.

where $M = 4$ for a four-phase mixer, and R_{BB} includes the ON resistance of the configuration switches. The LNTA input impedance is thus

$$R_{\text{in,LNTA}} = R_{\text{F}} / \left(1 + (g_{\text{m1}} + g_{\text{m2}})\, R_{\text{out}}\right) \tag{12}$$

where $R_{\text{out}} \approx R_{\text{seen,mixer}}$ since $R_{\text{seen,mixer}} \ll R_{\text{out,LNTA}}$. Shown in Fig. 7, since seven slices are connected in each VM, $R_{\text{in,VM}} = (1/7)R_{\text{in,LNTA}}$. Therefore, using (11) and (12) it can be shown that

$$R_{\text{in,VM}} = \frac{1}{7}\left(\frac{R_F}{1 + (g_{\text{m1}} + g_{\text{m2}})\, \frac{\text{sinc}^2\left(\frac{1}{M}\right)}{M} R_{\text{BB}}} \right) \tag{13}$$

where $M = 4$ and $R_{\text{BB}} = R_{\text{on,SW}} + R_{\text{in, TTD}}$.

B. Gain

After the down-conversion by the 25% LO-driven passive mixer, the BB current, illustrated in Fig. 7, is

$$i_{\text{BB}} = \frac{1}{4}\left(\text{sinc}^2\left(\frac{1}{M}\right)\right) i_{\text{in,RF}} \tag{14}$$

where $i_{\text{in,RF}} = g_{\text{m,LNTA}} V_{\text{in,RF}}$. With seven slices, the TTD unit input current, i.e., $i_{\text{in,TTD}}$ in Fig. 10, is

$$i_{\text{in,TTD}} = 7\left(\frac{1}{4}\right) \cdot \text{sinc}^2\left(\frac{1}{4}\right) \cdot i_{\text{in,RF}}. \tag{15}$$

To calculate the overall conversion gain, the TTD unit's current gain must also be considered. As shown in Fig. 10, having $R_{\text{out,TTD}} \gg R_{\text{in,TIA}}$, the current gain is

$$G_{\text{TTD}} = \left(\frac{1}{g_{\text{m1}} + g_{\text{m7}}} \right) \cdot (g_{\text{m2}} + g_{\text{m8}}). \tag{16}$$

Here, the TTD unit acts like a current mirror with $g_{\text{m1}} = g_{\text{m2}}$ and $g_{\text{m7}} = g_{\text{m8}}$, making G_{TTD} ideally equal to 1. Finally, all the BB currents from the four RXs are summed at the TIA's input, and the differential gain is

$$\text{CG}_{\text{diff}} = 2\,(7) \cdot \text{sinc}^2\,(1/4) \cdot g_{\text{m, LNTA}} \cdot G_{\text{TTD}} \cdot R_{\text{FB}} \tag{17}$$

where R_{FB} is TIA's feedback resistor shown in Fig. 11.

C. Noise Performance

This section analyses the RX's noise performance. Fig. 17 illustrates the equivalent circuit used for the noise calculation. Note that only one element is considered for the noise. As mentioned before, the LNTA dominates the noise performance as the first block in the RX chain. However, we model the noise sources for the LNTA, unit delay cell, and the TIA for analysis including: 1) the drain current noise of the LNTA transistors and its feedback resistor; 2) the input transistors of

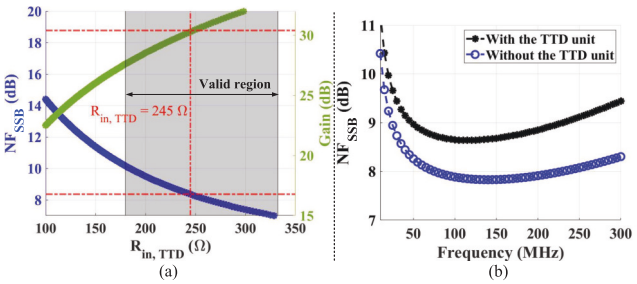


Fig. 18. (a) Effect of $R_{in,\,TTD}$ on the RX noise and gain at f_{BB} = 150 MHz simulated in MATLAB. (b) RX noise with and without the TTD unit simulated in Cadence.

the unit delay cell; and 3) drain current noise of the transistors and the noise of the TIA's feedback resistor.

The single-element noise factor can be obtained as

$$F = 1 + \frac{1}{\alpha^2}\left(\frac{R_{in}+R_s}{R_{in}}\right)^2 \left(\left(\frac{\gamma}{N\cdot g_{m,LNTA}\cdot R_S} + \frac{1}{4N\cdot g_{m,LNTA}^2\cdot R_s\cdot R_F}\right) + \left(\frac{4\left(g_{m1,TTD}+g_{m7,TTD}\right)}{R_s\cdot N^2\cdot g_{m,LNTA}\cdot \mathrm{sinc}^2\left(\frac{1}{4}\right)}\right) + \left(\frac{4R_{FB}+4\gamma\left(g_{m1,TIA}+g_{m2,TIA}\right)\left(R_{out,TIA}\right)^2}{R_s\cdot g_{m,LNTA}^2\cdot R_{FB}^2\cdot N^2\cdot \mathrm{sinc}^2\left(\frac{1}{4}\right)G_{TTD}^2}\right)\right) \quad (18)$$

where α indicates gain reduction when we move away from the corner points toward the biggest circle fit into the constellation plot to have the same gain, as indicated in Fig. 2(c). The first term after $(1/\alpha^2)(R_{in}+R_s/R_{in})^2$ is the LNTA's contribution, the second term is the TTD unit's contribution, and the third term is the TIA's contribution to the noise, N is the number of slices, and $R_{out,TIA} = (R_{FB}+R_{out,TTD})/((g_{m1,TIA}+g_{m2,TIA})\cdot R_{outTTD}+1)$. We set G_{TTD} = 1 in this design. In our current-mode RX, according to Fig. 10, the following two criteria should always be considered.

1) $R_{in,\,TTD} \ll R_{seen,\,mixer}$

$$\longrightarrow \frac{1}{(g_{m1}+g_{m7})} \ll \frac{1}{N}\left(\frac{R_{F,LNTA}}{2}\left(\frac{M}{\mathrm{sinc}^2\left(\frac{1}{M}\right)}\right)+R_{on,sW}\right)$$

2) $R_{seen,\,TIA} \ll R_{out}$, TTD

$$\longrightarrow \frac{4R_{FB,\,TIA}}{A_{TIA}} \ll (g_{m4}R_{out\,2}R_{out\,4})\,||\,(g_{m6}R_{out\,6}R_{out\,8}) \quad (19)$$

where M = 4 for a four-phase mixer, N is the number of slices, and A_{TIA} is the open-loop gain of TIA.

To get more gain out of the TTD unit, i.e., $G_{TTD} > 1$, either we should have larger $(g_{m2}+g_{m8})$ or smaller $(g_{m1}+g_{m7})$ according to (16); however, either of the criteria in (19) may not be valid, leading to gain and noise degradation. Fig. 18(a) shows the valid region for $R_{in,\,TTD}$ at f_{BB} = 150 MHz. We first designed for the TTD criteria and then optimized for the noise. $R_{in,\,TTD}$ is set to 245 Ω after the optimization. Fig. 18(b) shows the NF_{DSB}(dB) simulated results. The RX noise only increased by ≈0.9 dB in the center of the BB BW.

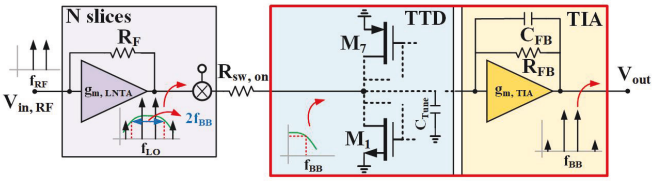


Fig. 19. Equivalent circuit for linearity analysis.

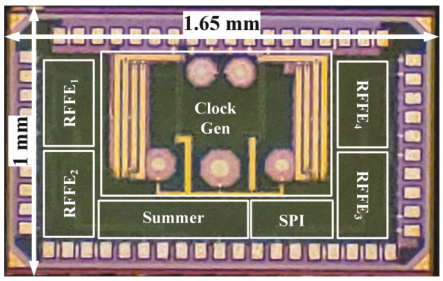


Fig. 20. Chip micrograph.

D. Linearity

In the RX depicted in Fig. 3, the TIA dominates the overall system linearity. The RX is designed to have a low voltage swing at each node, i.e., low impedance at each node, to maintain a good linearity. However, our system benefits from the TTD unit, which behaves like an LPF. Because of the transparency of the passive mixer, the LPF response is up-converted to the RF and acts like a bandpass filter (BPF) [34], [35], [36]. To comply with the criteria established in (19), the input impedance of the TTD unit is larger than that of the TIA. This gives the filter a relatively sharper roll-off, which helps suppress the unwanted blockers and tones created after the LNTA and improves the RX OIP3 compared with when there is no TTD unit, as depicted in Fig. 19.

V. Experimental Results

The chip was fabricated using TSMC 65-nm technology to prove the concept. The total chip area is 1.65 mm^2, which is packaged in a 48-pin QFN and is shown in Fig. 20. Fig. 21(a) and (b) shows the custom-designed two-layer and four-layer FR4 printed circuit boards (PCBs) to demonstrate the chip performance without and with the antenna, respectively. Four patch antennas are designed and placed at critical wavelength spacing on the four-layer PCB backplane for the OTA characterization, as shown in Fig. 21(c). Keysight ADS RFpro is used for the EM simulation of the PCB traces with antennas. Each antenna is associated with one of the four RF RXs. The feed lines to the antennas are length-matched to minimize the phase error. Fig. 21(d) shows the radiation pattern for the antenna board simulated in ADS. Fig. 22 illustrates the 2 × 2 antenna array spacing and dimension with more detail. The patch antennas are rotated 90° to each other for better isolation. Several techniques exist for increasing antenna BW, such as designing antennas with multiple resonant frequencies spaced sufficiently apart [37] or implementing multi-feed, multi-layer structures [38]. Four external baluns are used to provide differential inputs to the RF RX. An EVAL-ADF4372

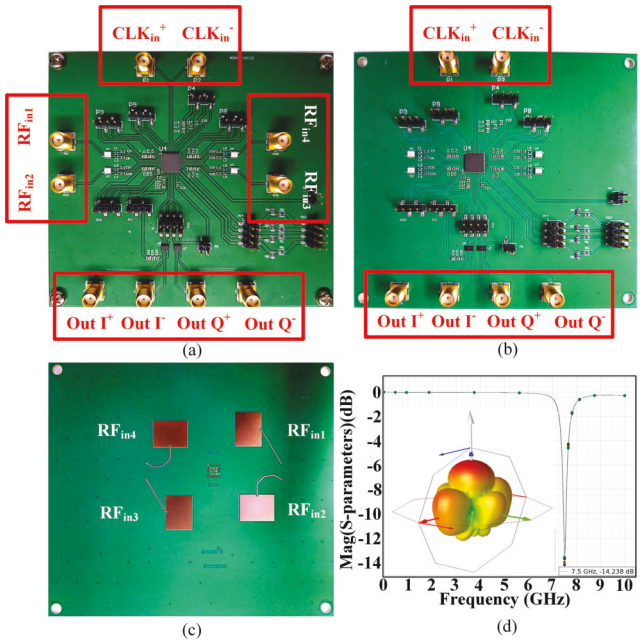


Fig. 21. PCB boards for the tests (a) two-layer with SMA inputs, (b) four-layer with antennas as inputs, (c) four-layer backplane, and (d) antennas S_{11} and far-field radiation simulation results in ADS.

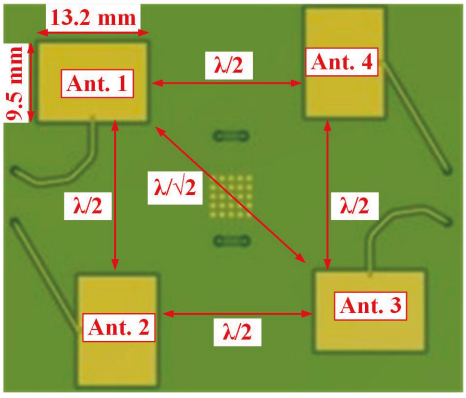


Fig. 22. 2×2 antenna array spacing and dimension.

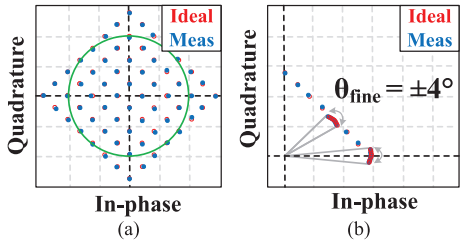


Fig. 23. (a) Ideal phase constellation with coarse phase shift. The green circle shows the maximum constant gain. (b) Measured phase constellation with fine phase shift [14].

board is used to provide a differential sinusoidal pair with a frequency of 3.75 GHz for on-chip 7.5-GHz clock generation and distribution. A Tektronix real-time spectrum analyzer and a Xilinx RFSoC ZCU216 were used to capture the down-converted quadrature signals. All the used SMA cables are length-matched to minimize both amplitude and phase error.

TABLE III
BIT ALLOCATION FOR SYSTEM TUNING

Parameter	Total Bits	Bits per RX
Coarse Phase Tuning	48	12
TTD Unit Tuning	40	10
TIA Feedback Tuning	6	-
SPI Functionality Verification	3	-

TABLE IV
CALIBRATION PROCEDURE FOR FOUR-ELEMENT BEAMFORMER

Step	Description
1	Measure all feasible phase constellation points for each RX by sweeping SPI phase codes and plotting I/Q outputs.
2	Fit the largest circle centered at the origin to identify constant-gain phase points as shown in Fig. 23. Select these as calibrated phase states.
3	Map and store SPI phase codes corresponding to calibrated phase points for beamforming use.
4	Configure all RX channels to their maximum gain using calibrated SPI settings.
5	Apply a single-tone signal to RF1 and program RX1 with a known delay τ_1 based on the TTD lookup table.
6	Set RX2–RX4 phase shifters to 180° offset relative to RX1 using coarse phase bits. Do not apply any TTD delay yet.
7	Sequentially feed the same tone to RX2–RX4 (one at a time) while monitoring the beamformed output. RX1 remains active.
8	For each RX (2–4), sweep its TTD delay settings and identify the SPI code that minimizes the beamformed gain (ideally to the noise floor). (The inter-element mismatch was found to be nearly equivalent to a single TTD resolution unit.).
9	Store calibrated TTD offsets relative to RX1's delay τ_1 for future beamforming compensation.

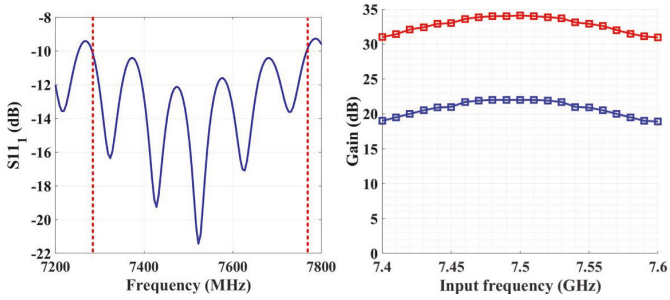


Fig. 24. Measured. (a) One-channel S_{11} [14]. (b) One-/four-channel gain.

The multiple tuning knobs in this work provide the opportunity for accurate calibration required in precision beamforming. To enable this, we first create a lookup table and apply this using the on-chip SPI with 97 control bits as shown in Table III. We summarize the calibration steps in Table IV. Fig. 23 illustrates all the measured phase constellation points.

An HP8510 network analyzer is used to measure the reflection coefficient, S_{11}, of the RX's inputs. An external π LC network enables each RX input to provide the best matching for the input frequency range. Fig. 24(a) shows the measured S_{11} of <-10 dB over the input RF frequency range of 7.28–7.78 GHz centered at an LO of 7.5 GHz. The ripples in S_{11} are primarily from the PCB traces which connect the SMA connectors to the device under test (DUT) inputs.

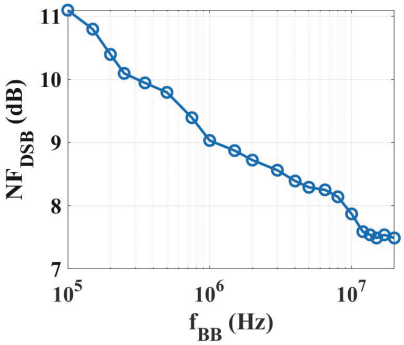


Fig. 25. Measured NF_{DSB} versus f_{BB} at f_{LO} of 7.5 GHz.

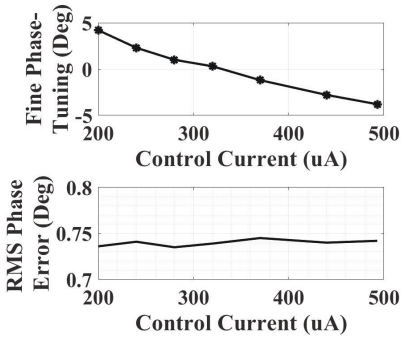


Fig. 26. Measured (top) fine phase tuning and (bottom) rms phase error.

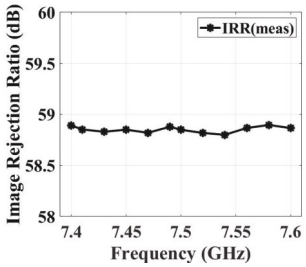


Fig. 27. Measured IRR over 200-MHz RF BW [14].

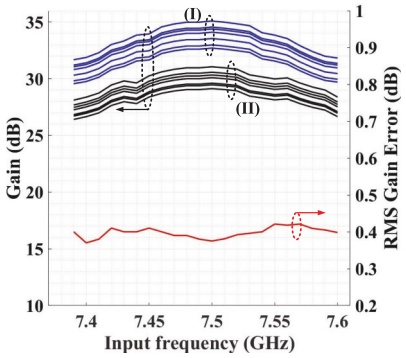


Fig. 28. (Pri. axis) Four-element gain with coarse phase-tuning step set to (I) 0° and (II) 37°, respectively, varied over the fine phase-tuning range. (Sec. axis) rms gain error.

These ripples can be suppressed using fixture compensation techniques such as de-embedding, as explained on [40, p. 23]. The configuration switches are set for the corners of the phase cancellation points to achieve the maximum RX conversion gain. In this case, for a single-channel measurement, differential quadrature current pairs are seven times a single unit-slice output current, i.e., $7I^+$, $7I^-$, $7Q^+$, and $7Q^-$, and are summed at the TIA's input, having the TIA's tuning bits set for the maximum gain. Fig. 24(b) illustrates the measured gain with the aforementioned setting, which is 22 dB for a single element and improves by +12 dB when all the four elements are engaged for the −3-dB input BW. In addition, the minimum single-channel NF_{DSB} is measured as 7.48 dB and is depicted in Fig. 25. However, for coherent beamforming, all the four beams should experience the same gain while compensating for the delay caused by the angle of arrival. For that, we suggest setting all the configuration switches in all the RF front ends (RFFEs) for the same gain, meaning using the points in the phase constellation that are close to the circle with the largest radius fit into the constellation diagram. As shown in Fig. 2(c), the largest fit circle's radius, i.e., the sum of I and Q vectors, is $1/\sqrt{2}$ of the maximum achievable corner point. This means that if we move toward the circle, the maximum achievable gain drops, and the NF degrades. Therefore, depending on the beam direction, the NF degrades according to the change in the RX gain. However, having a 4/1 multiple-input single-output (MISO) RX, the SNR is improved by a factor of 4, resulting in a 6-dB increase.

All the four elements are engaged to show the effect of the LO phase shift on the gain. Note that the configuration switches are set for the maximum gain. The TIDA-01525 DAC is configured to set the reference and tuning currents for the DUT. To characterize the fine phase shifting in the LO path, the PPF control current, i.e., I_{shift}, is swept from 200 μA to 500 μA, and the relative phase shift of $\pm 4°$ is measured at 7.5 GHz as depicted in Fig. 26 (top). The measured LO phase shift achieves a root mean square (rms) phase error of 0.74°, as shown in Fig. 26 (bottom). The rms phase error is calculated based on the simulated and measured phase shifts provided by the fine phase step while tuning the PPF's control current, as shown in [14, Fig. 26]. The measured image-rejection ratio (IRR) over 200-MHz RF BW, caused by quadrature mismatches, shows a uniform value of >58 dB, as depicted in Fig. 27. Fig. 28 shows the conversion gain using the fine phase shift when configuration switches are set for incidence angles of (I) 0° and (II) 36°. The total beamforming gain drops since we chose the phase points that are the closest to the biggest fit circle inside the phase constellation points, i.e., the green circle illustrated in Fig. 23. An amplitude rms error of 0.4 dB is achieved when operating at 7.5 GHz. The measured 1-dB compression point (P1dB) is −9 dBm for a one-channel RX, as shown in Fig. 29(a). The two-tone test achieves an in-band OIP3 of 20.6 dBm, as highlighted in Fig. 29(b).

To gauge the TTD's performance, the Keysight M8195A arbitrary waveform generator (AWG), shown in Fig. 30(a), is used to generate four 200-MHz WB signals centered at 7.5 GHz and fed to each of the four elements. The incidence angle should be different from the broadside to require delay compensation. Therefore, the AoA is set to 37°, and

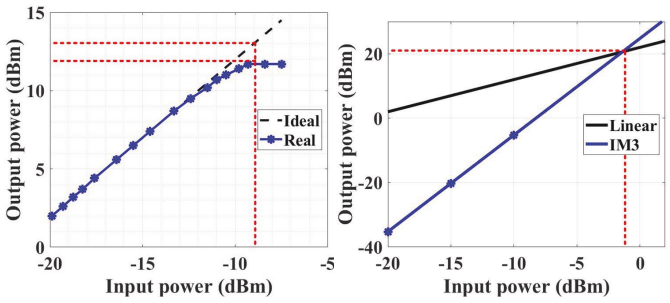


Fig. 29. Measured one-channel (a) P1dB and (b) OIP3 [14].

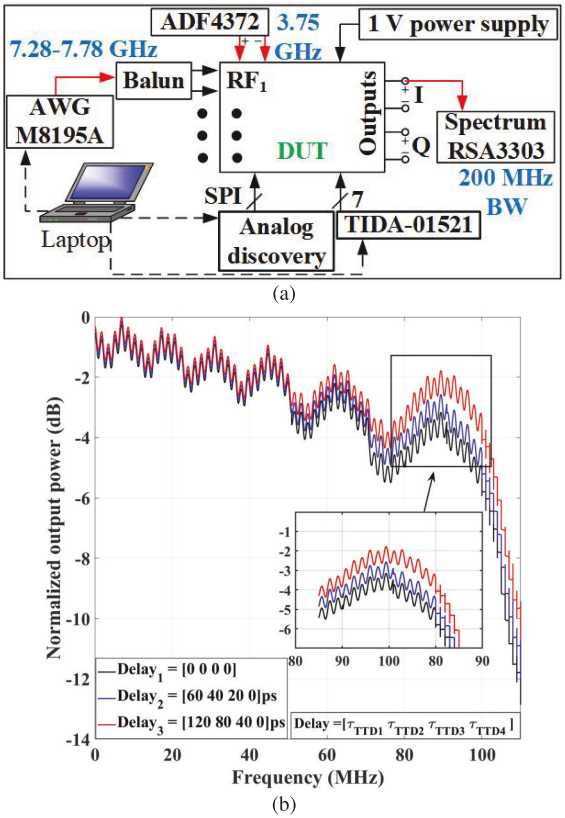


Fig. 30. (a) Test setup for characterizing TTD performance. (b) Measured beamformed output power in the presence of an input signal with 100-MHz BW with squint effect.

the configuration switches in each RX front end, i.e., the switches matrix shown in Fig. 7, are set to compensate for the needed phase shift. We can only compensate for the delays for narrowband signals using fine and coarse phase shift mechanisms. However, we have to use the TTD for signals with wider fractional BW. Fig. 30(b) shows that the measured down-converted normalized output power deviates from what it should be, especially at the signal edges, i.e., 100 MHz, when the TTD is not activated. The measured normalized output power for two cases of 60- and 120-ps time delay (maximum achievable delay using the TTD cell) shown in Fig. 30(b) indicates a better WB signal alignment and the improvement of the received WB signal power up to ≈1.5 dB

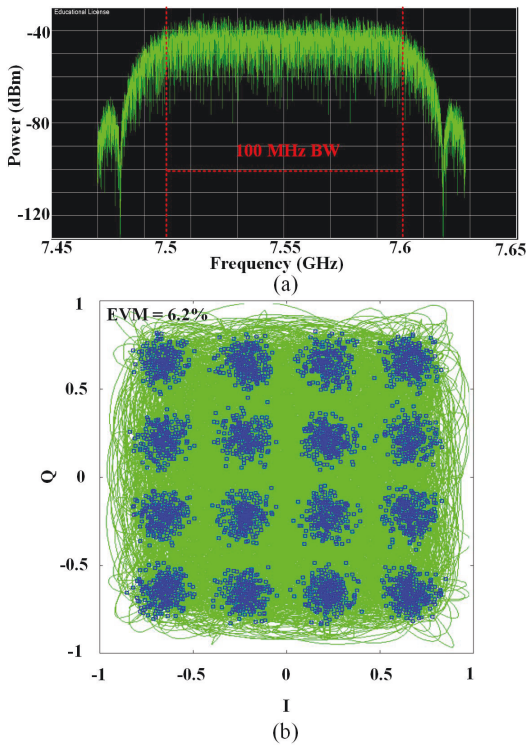


Fig. 31. (a) ≈74.07 MSymbols/s 16-QAM input signals with a root-raised cosine pulse shaping filter with α = 0.35 centered at 7.55 GHz and (b) measured output EVM.

at the band edges. Note that the signal droop is due to the 3-dB BW of the RX.

The same setup as TTD in Fig. 30(a) is used to measure the EVM but with zero AoA. Four WB modulated ≈74.07 MSymbols/s 16-quadrature amplitude modulation (QAM) signals with a root-raised cosine pulse shaping filter with α = 0.35 were generated centered at 7.55 GHz and fed to the beamformer using the AWG. This will give a 50-MHz WB quadrature signal centered at 50 MHz at BB. Using the Keysight vector signal analyzer, the output power and the EVM of one of the demodulated quadrature outputs, for simplicity, are depicted in Fig. 31(a) and (b), respectively. Using our coarse- and fine-phase shift results in an EVM of 6.2%. Readers can refer to Appendix A for detailed link budget analysis.

Fig. 32 shows the OTA setup with the RX board mounted on a DAMS 7000 antenna measurement system,[1] providing the accurate setting for AoA tests. The AWG generates a single-tone 7.53-GHz input signal and is connected to a broadband gain horn antenna (PE9888-11) for OTA transmission. The spacing between the horn antenna and the RX is 297.9 cm placed in the far-field radiation zone.

Fig. 33 (inset) shows the detailed setup. The down-converted signal is successfully received at broadside 30-MHz offset from the carrier, as shown in Fig. 33. The normalized radiation pattern for three AoAs of -30°, 0°, and 30° is shown in Fig. 34. With a single-tone, the TTD is not required, and hence, only

[1]DAMS 7000 has a rotation resolution of up to 0.0625° steps azimuth and 0.10° steps elevation.

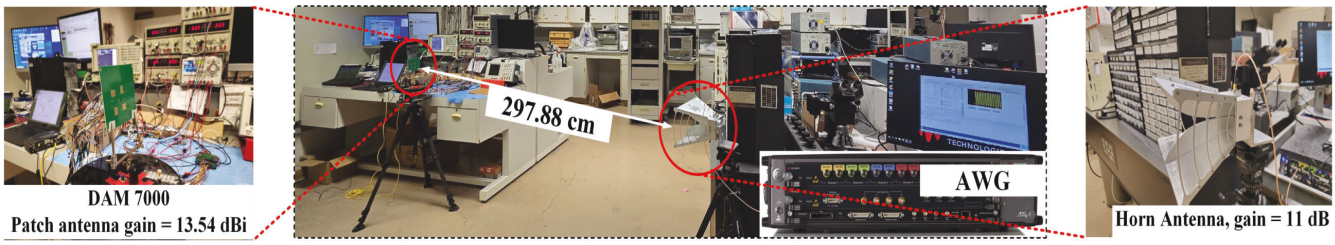


Fig. 32. (Left) PCB board mounted on the DAMS antenna measurement system. (Center) OTA test bench. (Right) Horn antenna.

TABLE V
COMPARISON TO STATE-OF-THE-ART BEAMFORMERS

Work	RFIC'16 [16]	JSSC'17 [4]	JSSC'17 [5]	JSSC'21 [6]	JSSC'23 [7]	**This work**
Process	65nm CMOS	65nm CMOS	65nm CMOS	22nm FD-SOI	45nm SOI CMOS	**65nm CMOS**
Array elements	4/1 MIMO	4/4 MIMO	4/1 MISO	4/4 MIMO	4/4 MIMO	**4/1 MISO**
Method	VM	VM	VM	VM	VM	**VM + PPF + TTD**
Blocks	Beamformer	Beamformer + LO CLK[1]	Beamformer + LO CLK[1]	Beamformer + LO CLK[1]	Beamformer + LO CLK[2]	**Beamformer + LO CLK[3]**
Area(mm^2)	3.8	2.25	1	0.8	7.54	**1.65**
RF frequency (GHZ)	10	0.1–3.1	1–2.5	0.7–5.7	26–33	**7.28-7.78**
Per element Gain (dB)	14	43	12	41 (total gain)	28	**22**
Min. single-element $NF_{\mathrm{DSB}}(dB)$	9.5	5.8	6	11.1	7.7	**7.48**
In-Band OIP3 (dBm)	NA	+1	+13	+22	NA	**+20.6**
Phase resolution (bits)	6	3.8	4	4	NA	**Continuous[4]**
RMS phase error (°)	2.7[5]	2	0.8	1.3	NA	**0.74**
Gain phase error (dB)	0.5[5]	0.2	0.17	0.28	NA	**0.4**
Time Delay Range (ps)	NA	NA	NA	NA	NA	**120**
Supply(V)	1.3–1.6	1.2	1	0.8	NA	**1**
Power/element (mW)	145	116–147 (4 Elements)	9	77–139 (4 Elements)	66	**14**
FOM[6]	0.16	11.4	1.6	3.7	NA	**15.14**

[1] LO frequency divider (÷2) + distribution; [2] 2-Stage Transformer-Based Quadrature LO Generation; [3] LO frequency doubler + distribution.
[4] PPF resolution limited by the 16-bit Texas Instruments TIDA-01525 DAC in the test setup. [5] Best case.
[6] FOM $= \frac{f_c \cdot \mathrm{Gain} \cdot \mathrm{BW} \cdot \mathrm{Resolution}}{\mathrm{RMS\_Phase\_error} \cdot \mathrm{RMS\_Gain\_error} \cdot P_c \cdot (\mathrm{NF}-1)}$

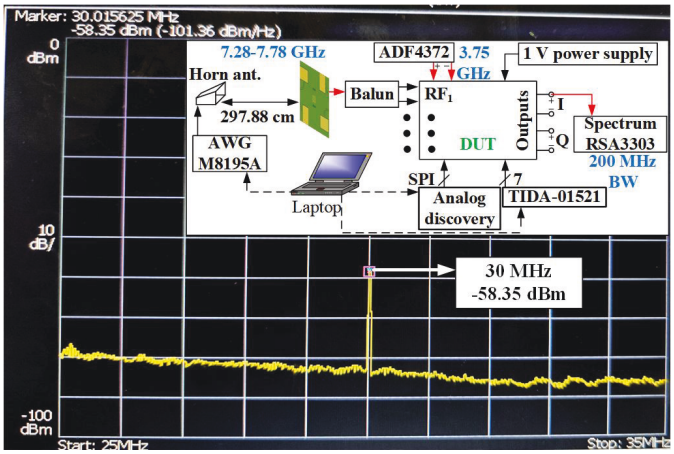


Fig. 33. Received signal OTA for an incidence angle of 0°. OTA test bench diagram (inset).

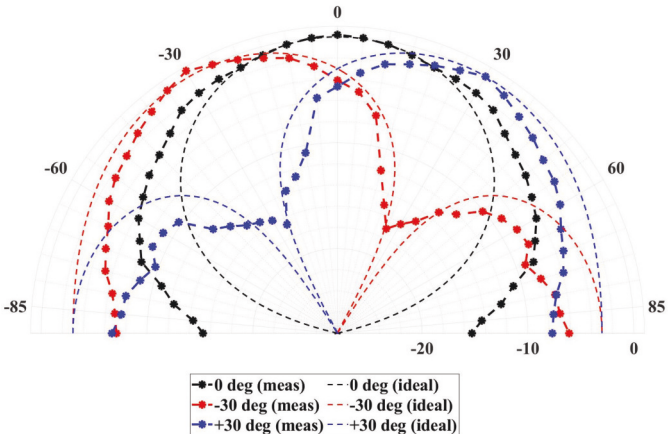


Fig. 34. Normalized ideal and measured radiation patterns for three AoAs of −30°, 0°, and 30°.

the coarse- and fine-phase tuning mechanisms were engaged for phase compensation of non-zero incidence angles. The TTD's role is merely to apply consistent delay shifts for beam alignment, not to alter the waveform. Thus, the constellation integrity is preserved, and the EVM remains unaffected.

Table V shows comparison of the performance of the proposed RX array to state-of-the-art works. Compared with previously reported slice-based architectures [5], [6], this design achieves continuous 360° coverage using fewer slices, enhanced by fine-resolution phase shifting and integrated TTD units, enabling precise calibration and accurate beamforming. The implementation of passive elements for LO matching and frequency-doubling for signal peaking results in a relatively larger area compared with arrays operating at lower RF frequencies. Nevertheless, this design demonstrates improved gain and linearity compared with [5], despite slightly higher

power consumption due to operation at nearly 3× higher frequency and the additional inclusion of PS–TTD compensation. Importantly, its power consumption remains lower than that of [6]. In comparison, [4] consumes higher power at lower frequencies and offers inferior phase resolution. In addition, the architecture in [16], designed for spatial cancellation using four inputs, features lower BW, higher noise figure (NF), significantly greater power consumption, and a larger chip area. Although [7] achieves continuous phase resolution, it demands substantially greater power and chip area compared with our implementation. Furthermore, all the aforementioned references solely rely on phase shifters, making them susceptible to beam-squint errors. To facilitate a comprehensive comparison, the figure-of-merit (FoM) from [40] has been calculated and included in the table.

VI. Conclusion and Future Works

In this article, a precisely adjustable phase-delay tuned beamforming RX array was presented for the emerging applications in upper mid-band wireless. The design incorporates two separate fine and coarse phase-tuning steps, allowing comprehensive scanning across all the four quadrants. To mitigate beam squint having WB signals, BB TTD cells are implemented, offering a delay range of up to 120 ps. The TTD cells act like LPFs. The transparency of passive mixers helps have BPFs right after the LNTA, which in return provides RFFEs with enhanced out-of-band blocker rejection, relaxing the dynamic range of the preceding ADCs. With the TTD in place, an in-band OIP3 of 20.6 dBm is achieved while exhibiting a maximum single-channel gain of 22 dB. By cascading more TTD units, we can extend the delay range, making this beamformer IC more suited for higher data-rate links in densely populated networks.

Appendix A.
Appendix A Link Budget Analysis

In the appendix, we analyze the link budget relating to EVM together with the NF. Assuming our system is only noise-limited, according to [41], the SNR can be extracted as

$$\mathrm{SNR} = -\left[\mathrm{PAPR} + 20\mathrm{Log}_{10}\left(\mathrm{EVM}\%/100\right)\right] \qquad (20)$$

where PAPR is the peak-to-average-power-ratio for a modulated signal. Having an EVM of 6.2% and assuming a PAPR of ≈7, based on (20), the four-channel SNR is

$$\mathrm{SNR}_{4-ch} = -\left[7 + 20\mathrm{Log}_{10}\left(6.2/100\right)\right] = 17.15\mathrm{dB}. \qquad (21)$$

Therefore, for a single-channel, the SNR will be $\mathrm{SNR}_{1-ch} = \mathrm{SNR}_{4-ch} - 6 = 11.15\mathrm{dB}$. We illustrate the link budget as Fig. 35. All the parameters are shown in Table VI.

In this case, $P_{\mathrm{sensitivity}}$ is ≈-76.2 dBm. Note that P_{received} is limited to $P_{1\mathrm{dB}}$ and the PAPR and is calculated as $P_{\mathrm{received,max}} = P_{1\mathrm{dB}} - \mathrm{PAPR} \approx -16\,\mathrm{dBm}$ leading to the above-mentioned dynamic range. With the AWG supplying a transmit power of approximately $P_{\mathrm{transmit}} \approx -3\,\mathrm{dBm}$, and considering a 2-dB loss from the on-board baluns, the received input power is estimated to be $P_{\mathrm{received}} \approx -40\,\mathrm{dBm}$. In addition, we measured the SMA cable loss to be 6 dB, which was accounted for when directly connecting to the AWG rather than operating OTA.

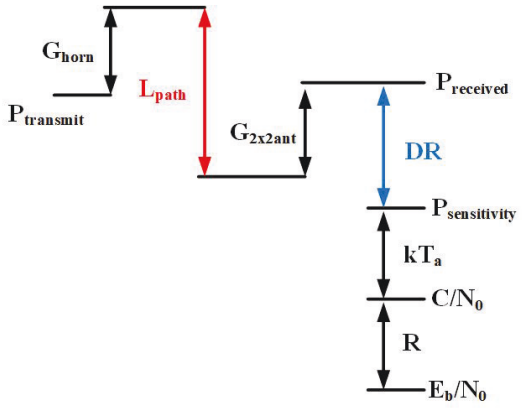


Fig. 35. Link budget for the proposed system.

TABLE VI
Link Budget Parameters

Parameter	P_{transmit} (dBm)	G_{horn} (dBi)	L_{path} (dB)	$G_{2\mathrm{x}2\mathrm{ant}}$ (dBi)	E_b/N_0 (dB)	R (MS/s)	T_a (K)	DR (dB)
Value	-3	11	-59.42	13.54	6.43	296.3	1333	60.2

Acknowledgment

The authors would like to thank Keysight for their help with OTA characterization, providing a multichannel AWG M8195A. They also acknowledge Prof. Tutku Karacolak at WSU Vancouver for providing the DAMS 7000 antenna measurement systems and Ted Dabrowski and Kalsi Kwan at Boeing Additive Printing Group for initial floor planning of the PCBs.

References

[1] L. Zhang, A. Natarajan, and H. Krishnaswamy, "Scalable spatial notch suppression in spatio-spectral-filtering MIMO receiver arrays for digital beamforming," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3152–3166, Dec. 2016.

[2] S. Mondal, R. Singh, A. I. Hussein, and J. Paramesh, "A 25–30 GHz fully-connected hybrid beamforming receiver for MIMO communication," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1275–1287, May 2018.

[3] B. Sadhu et al., "A 28-GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3373–3391, Dec. 2017.

[4] L. Zhang and H. Krishnaswamy, "Arbitrary analog/RF spatial filtering for digital MIMO receiver arrays," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3392–3404, Dec. 2017.

[5] M. C. M. Soer, E. A. M. Klumperink, D. van den Broek, B. Nauta, and F. E. van Vliet, "Beamformer with constant-gm vector modulators and its spatial intermodulation distortion," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 735–746, Mar. 2017.

[6] S. Golabighezelahmad, E. A. M. Klumperink, and B. Nauta, "A 0.7–5.7 GHz reconfigurable MIMO receiver architecture for analog spatial notch filtering using orthogonal beamforming," *IEEE J. Solid-State Circuits*, vol. 56, no. 5, pp. 1527–1540, May 2021.

[7] T.-Y. Huang, B. Lin, N. S. Mannem, B. Abdelaziz, and H. Wang, "A time-modulated concurrent steerable multibeam MIMO receiver array with spectral–spatial mapping using one beamformer and single-wire interface," *IEEE J. Solid-State Circuits*, vol. 58, no. 5, pp. 1228–1240, May 2023.

[8] S. Mohin, S. Araei, M. Barzgari, and N. Reiskarimian, "A blocker-tolerant mm-wave MIMO receiver with spatial notch filtering using non-reciprocal phase-shifters for 5G applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2024, pp. 15–18.

[9] S. Jang, J. Jeong, R. Lu, and M. P. Flynn, "A 16-element 4-beam 1 GHz IF 100 MHz bandwidth interleaved bit stream digital beamformer in 40nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1302–1312, May 2018.

[10] R. Lu, C. Weston, D. Weyer, F. Buhler, D. Lambalot, and M. P. Flynn, "A 16-element fully integrated 28-GHz digital RX beamforming receiver," *IEEE J. Solid-State Circuits*, vol. 56, no. 5, pp. 1374–1386, May 2021.

[11] D. Peña-Colaiocco, C.-H. Huang, K.-D. Chu, J. C. Rudell, and V. Sathe, "An optimal digital beamformer for mm-Wave phased arrays with 660 MHz instantaneous bandwidth in 28nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, Feb. 2022, pp. 1–3.

[12] K. Spoof, M. Tenhunen, V. Unnikrishnan, K. Stadius, M. Kosunen, and J. Ryynänen, "True-time-delay receiver IC with reconfigurable analog and digital beamforming," *IEEE Access*, vol. 10, pp. 116375–116383, 2022.

[13] D. Dosluoglu, K.-D. Chu, D. Pena-Colaiocco, I. Zhao, V. Sathe, and J. C. Rudell, "A reconfigurable digital beamforming V-band phased-array receiver," in *Proc. IEEE 48th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2022, pp. 493–496.

[14] A. Slater, H. Abbasi, S. Poolakkal, F. Beheshti, and S. Gupta, "Enhancing continuous beam angle resolution for next generation wireless systems: A multi-stage phase-shifting polyphase filters approach," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 71, no. 11, pp. 5200–5210, Nov. 2024.

[15] M. Abbasi and W. Lee, "A low-loss passive D-band phase shifter for calibration-free, precise phase control," *IEEE J. Solid-State Circuits*, vol. 59, no. 5, pp. 1371–1380, May 2024.

[16] S. Jain, Y. Wang, and A. Natarajan, "A 10 GHz CMOS RX frontend with spatial cancellation of co-channel interferers for MIMO/digital beamforming arrays," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2016, pp. 99–102.

[17] C.-C. Lin, Q. Xu, H. Hu, and S. Gupta, "Design considerations of time-interleaved discrete-time beamformers toward wideband communications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 11, pp. 4068–4072, Nov. 2023.

[18] M. Soer, "Switched-RC beamforming receivers in advanced CMOS: Theory and design," Ph.D. thesis, Dept. Elect. Eng., Math. Comput. Sci. (EEMCS), Univ. Twente, Enschede, The Netherlands, 2012.

[19] S. Jang, R. Lu, J. Jeong, and M. P. Flynn, "A 1-GHz 16-element four-beam true-time-delay digital beamformer," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1304–1314, May 2019.

[20] E. Ghaderi, A. Sivadhasan Ramani, A. A. Rahimi, D. Heo, S. Shekhar, and S. Gupta, "An integrated discrete-time delay-compensating technique for large-array beamformers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 9, pp. 3296–3306, Sep. 2019.

[21] Q. Xu, C.-C. Lin, A. Wadaskar, H. Hu, D. Cabric, and S. Gupta, "A 10ns delay range 1.5GHz BW true-time-delay array-based passive-active signal combiner with negative-cap stabilized RAMP for fast precise localization," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2024, pp. 227–230.

[22] F. Beheshti, R. Li, S. Gupta, and D. Cabric, "Early-late correlation for wideband interference AoA estimation and suppression in analog uniformly spaced linear TTD arrays," in *Proc. 58th Asilomar Conf. Signals, Syst., Comput.*, Oct. 2024, pp. 639–646.

[23] Q. Xu et al., "A TTD-based fast precise localization enabled by passive–active signal combiner with negative-capacitance stabilized ramp," *IEEE J. Solid-State Circuits*, early access, Mar. 18, 2025, doi: 10.1109/JSSC.2025.3546958.

[24] A. Wadaskar et al., "Demonstration of fast OTA chirp-based beam training using analog TTD array with millimeter wave testbed for applications in radar systems," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2025, pp. 1–8.

[25] Q. Zhang et al., "A 23.5–28.5 GHz high-gain CMOS transceiver based on LO phase-shifting architecture with broadband LO/IF for 5G communications," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2022, pp. 2501–2505.

[26] J. Pang et al., "A 28GHz CMOS phased-array transceiver featuring gain invariance based on LO phase shifting architecture with 0.1-degree beam-steering resolution for 5G new radio," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 56–59.

[27] M. Yaghoobi, M. H. Kashani, M. Yavari, and S. Mirabbasi, "A 56-to-66 GHz CMOS low-power phased-array receiver front-end with hybrid phase shifting scheme," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 11, pp. 4002–4014, Nov. 2020.

[28] C. Fang et al., "A 22.5–33.5-GHz hybrid phase shifter with low phase and amplitude error for 5G and satellite communication," *IEEE Trans. Microw. Theory Tech.*, vol. 72, no. 5, pp. 3001–3015, May 2024.

[29] J. Zhou, B. Yang, Y. Shu, and X. Luo, "A W-band 2 × 2 phased-array transmitter with digital gain-compensation technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 71, no. 4, pp. 1558–1571, Apr. 2024.

[30] K. Ding et al., "A 23-GHz TX/LNA front-end module for inter-satellite links with 27.8% peak efficiency in the TX path and 3.1-dB NF in the RX path," *IEEE J. Solid-State Circuits*, vol. 59, no. 11, pp. 3644–3654, Nov. 2024.

[31] A. Ghaffari, E. A. M. Klumperink, and B. Nauta, "Tunable N-path notch filters for blocker suppression: Modeling and verification," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1370–1382, Jun. 2013.

[32] S. K. Garakoui, E. A. M. Klumperink, B. Nauta, and F. E. van Vliet, "Compact cascadable gm-C all-pass true time delay cell with reduced delay variation over frequency," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 693–703, Mar. 2015.

[33] D. Kar, S. Mohapatra, M. A. Hoque, and D. Heo, "A 14 GHz integer-N sub-sampling PLL with RMS-jitter of 85.4 fs occupying an ultra low area of 0.0918 mm^2," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 71, no. 2, pp. 595–605, Feb. 2024.

[34] B. van Liempd et al., "A 0.9 V 0.4–6 GHz harmonic recombination SDR receiver in 28nm CMOS with HR3/HR5 and IIP2 calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1815–1826, Aug. 2014.

[35] A. Mirzaei, H. Darabi, and D. Murphy, "Architectural evolution of integrated M-phase high-Q bandpass filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 1, pp. 52–65, Aug. 2012.

[36] J. Borremans et al., "A 40nm CMOS 0.4–6 GHz receiver resilient to out-of-band blockers," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1659–1671, Jul. 2011.

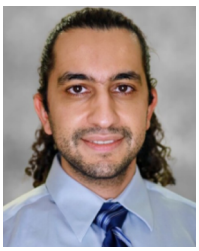
[37] R. B. Waterhouse, "Design of probe-fed stacked patches," *IEEE Trans. Antennas Propag.*, vol. 47, no. 12, pp. 1780–1784, Dec. 1999.

[38] B. Jamadi, W. Lee, and J. Walling, "Multi-feed multi-layer in-antenna power combining approach," in *Proc. IEEE Radio Wireless Symp. (RWS)*, Jan. 2025, pp. 29–32.

[39] *IEEE Standard for Electrical Characterization of Printed Circuit Board and Related Interconnects at Frequencies Up to 50 GHz*, Standard 370-2020, 2021.

[40] D. Pepe and D. Zito, "Two mm-Wave vector modulator active phase shifters with novel IQ generator in 28nm FDSOI CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 344–356, Feb. 2017.

[41] E. Acar. (2021). *How Error Vector Magnitude (EVM) Measurement Improves Your System-level Performance*. [Online]. Available: https://www.analog.com/en/resources/technical-articles/how-evm-measurement-improves-system-level-performance.html



Hesam Abbasi (Graduate Student Member, IEEE) received the M.Sc. degree in electrical engineering from the Amirkabir University of Technology, Tehran, Iran, in 2021. He is currently pursuing the Ph.D. degree with the SoC Laboratory, Washington State University, Pullman, WA, USA.

His research interests include low-noise and highly linear and efficient phased-array wideband transceivers.

Adam Slater (Graduate Student Member, IEEE) received the B.S. degree from Western Washington University, Bellingham, WA, USA, in 2015, and the M.S. degree in electrical engineering from Washington State University, Pullman, WA, USA, in 2023. He is currently pursuing the Ph.D. degree in electrical engineering with the University of Virginia, Charlottesville, VA, USA.

In 2015, he joined Schweitzer Engineering Laboratories, becoming a Lead Hardware Engineer who developed electronics hardware for real-time automation controllers and monitoring equipment. His research interests include high-speed analog processing, data converters, and photonic integrated circuits.

Mr. Slater was awarded Virginia Space Grant Consortium Graduate STEM Research Fellowship in 2024 and 2025.

Foad Beheshti (Graduate Student Member, IEEE) received the B.Sc. degree in electronics and electrical engineering from the University of Tabriz, Tabriz, Iran, in 2013, and the M.Sc. degree in circuits and systems, electronics, and electrical engineering from the University of Tehran, Tehran, Iran, in 2016. He is currently pursuing the Ph.D. degree in electrical engineering with Washington State University, Pullman, WA, USA.

As an Analog Integrated Circuit Design Researcher, he worked on the integrated impedance measurement analog front end for deep brain stimulation (DBS) application with the Bio-Integrated Circuits and Systems Laboratory, University of Tehran, from 2019 to 2022. His current research interests include analog/mixed-signal and wireless IC design and RF transceivers.

Sreeni Poolakkal (Graduate Student Member, IEEE) received the B.Tech. degree from the University of Calicut, Calicut, India, in 2014, and the M.Tech. degree from the IIT Guwahati, Guwahati, India, in 2018. He is currently pursuing the Ph.D. degree with Washington State University, Pullman, WA, USA.

From 2018 to 2021, he worked as a Technologist at Tata Steel, Jamshedpur, Jharkhand, India. His research interests include highly linear wideband phased-array radios, statistical optimization-based hardware design, and AI-assisted RF design.

Mr. Poolakkal was a recipient of the Johnson Electrical Engineering Scholarship and the Harold and Diana Frank Electrical Engineering Fellowship from the School of Electrical Engineering and Computer Science at Washington State University in 2025. He was awarded the Outstanding Research Assistant Award in Electrical and Computer Engineering by Washington State University. In addition, he received the IEEE Solid-State Circuits Society (SSCS) Student Travel Grant Award (STGA) to attend the International Solid-State Circuits Conference (ISSCC) in 2022.

Subhanshu Gupta received the B.E. degree from the National Institute of Technology (NIT), Trichy, India, in 2002, and the M.S. and Ph.D. degrees from the University of Washington, Seattle, WA, USA, in 2006 and 2010, respectively.

He is currently an Associate Professor of electrical engineering and computer science with Washington State University, Pullman, WA, USA. He has held industrial positions at Maxlinear, Irvine, CA, USA, where he worked on SATCOM/infrastructure applications. His research interests include energy-efficient transceivers for wireless and wireline data communications/IoT/sensing applications, wideband large-scale beamformers for phased-array communications and sensing, and cryoelectronics for quantum sensing and communications.

Dr. Gupta has been a member of the Technical Program Committee of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium since 2022. He was a recipient of the 2019 National Science Foundation CAREER Award. He has served as an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I.