10 kV, 250 °C Operational, Enhancement-Mode Ga_2O_3 JFET with Charge-Balance and Hybrid-Drain Designs

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Abstract— We report the first 10 kV Enhancement-mode (E-mode) transistor in ultra-wide bandgap (UWBG) materials. This lateral Ga_2O_3 junction-gate field-effect-transistor (JFET) deploys a highly-doped p-type NiO for E-mode gate, as well as the lowly-doped NiO superjunction and hybrid-drain structures for electric field management. The Ga_2O_3 channel is optimized with a 1.5×10^{18} cm^{-3} doping and two thickness designs of 50 and 160 nm. At 25 °C, both JFETs achieve the E-mode and >10 kV breakdown voltage (BV), with the specific on-resistance ($R_{ON,SP}$) being 92 and 703 mΩ·cm^2 for the thick- and thin-channel designs, respectively. At 250 °C, the thin-channel JFET remains E-mode with a BV over 10 kV at zero gate-source bias (V_{GS}). In contrast, the thick-channel JFET turns into depletion-mode (D-mode) at high temperatures (T) and maintains 10 kV BV only up to 150 °C, due to the insufficient gate control to counter the drain-induced barrier lowering (DIBL) effect. This implies a trade-off between $R_{ON,SP}$ and high-T stability. Both devices survive the high-T gate bias (HTGB) and 3 kV high-T reverse bias (HTRB) reliability tests. Overall, our device presents not only the best figure-of-merits (FOMs) in all >3 kV UWBG transistors, but also the first 250 °C operation and 3 kV reliability data in all high-voltage transistors beyond Si and SiC. The unveiled device physics and trade-off can also guide the development of future high-voltage, high-T power transistors.

I. Introduction

Medium-voltage (1-35 kV) power electronics is ubiquitous in grid and renewable energy applications. The availability of high-voltage (HV) devices can significantly reduce the device count, simplify the circuit topology, and improve the system form factor and reliability. Today's commercial HV devices are dominated by Si IGBTs up to 6.5 kV; SiC MOSFET are available in engineering samples up to 10 kV [1]. Different from these two vertical devices, lateral GaN HEMTs with BV of 5~10 kV have also been demonstrated recently [2-5]. While vertical structure has a higher current capacity, lateral structure is attractive for HV, low-current devices as required in many applications, e.g., high voltage DC power supply [6].

UWBG devices are now under extensive research for HV and harsh environment applications, for which the superior properties of UWBG materials can be exploited. Among them, Ga_2O_3 possesses a 4.8 eV bandgap (E_G), high critical electric field (E-field), large-wafer (6-inch) availability, and it can be grown from the melt. Moreover, in UWBG devices, Ga_2O_3 is in a leading position for BV upscaling. Ga_2O_3 MOSFETs with BV from 8 kV up to 10 kV has been recently reported [7-9]. However, these devices are all D-mode and has a $R_{ON,SP}$ 30-80000× higher than similarly-rated SiC MOSFETs. On the other hand, despite the high-temperature (T) operation reported in low-voltage devices, there has been no reports of kilovolt blocking capability at high T in UWBG transistors.

This work fills the gap by demonstrating an E-mode Ga_2O_3 JFET with BV > 10 kV measured up to 250 °C. Here we use p-type NiO (E_G=3.6~4 eV) with tunable acceptor concentration (N_A) [10] to overcome the lack of native p-n junctions in Ga_2O_3. Distinct from prior Ga_2O_3 JFETs [11], our device deploys NiO not only for E-mode gate but also to construct a charge-balance reduce-surface-field (RESURF) structure and a hybrid-drain structure for E-field management. The fabricated Ga_2O_3 JFETs not only achieve the highest FOM in all UWBG transistors with BV > 3 kV, but also demonstrate the 250 °C operation and the HTRB/HTGB reliability data, for the first time, in all HV power transistors beyond Si IGBT and SiC MOSFET. In addition to performance, the key device design trade-off is also unveiled through the comparison of two devices fabricated in this work.

II. Device Design and Fabrication

As shown in Fig. 1a, the Ga_2O_3 JFET comprises an n-Ga_2O_3 channel (donor concentration N_D and thickness t_D), a p^{++}-NiO gate, a p-NiO RESURF structure (thickness t_A and N_A=N_A^R), and a p$^+$-NiO hybrid drain (N_A=N_A^{Dr}). A spacing between two NiO regions avoids the NiO punch-through and allows for distinct N_A^R and N_A^{Dr}. The device design mainly considers:

a) E-mode operation sets an upper limit of t_D for a given N_D:

$$V_{TH} = V_{bi} - qN_Dt_D^2/2\varepsilon - Q_{it}t_D/\varepsilon > 0 \quad (1)$$

where V_{TH} is threshold voltage, V_{bi} is the NiO/Ga_2O_3 built-in potential, ε is Ga_2O_3 permittivity, Q_{it} is the NiO/Ga_2O_3 interface charge density. Fig. 1b shows the calculated t_D and N_D ranges.

b) Charge-balance between p-NiO RESURF and n-Ga_2O_3 channel enables a superjunction-effect, i.e., uniform E-field due to net zero charge. This can be written for a ±15% tolerance:

$$N_A^Rt_A - Q_{it} = (0.85\sim1.15)N_Dt_D \quad (2)$$

TCAD simulations calibrated with experimental devices in [12] are used to optimize the E-field management (Fig. 2). The NiO RESURF is verified to enable a uniform E-field (Fig. 2c), which is favorable for upscaling BV with the gate-drain distance (L_{GD}). The peak E-field remained near the drain is suppressed by a hybrid-drain, similar to the design in Infineon's GaN GIT [13], and N_A^{Dr} is optimized to be ~1.5×10^{18} cm^{-3} (Fig. 2d). With these designs, N_D cannot be too high; otherwise, crowded E-field will emerge near the NiO spacing and limit the BV (Fig. 2e).

c) R_{ON} reduction requires the maximization of N_D·t_D. Besides, $N_D > N_A^R$ is preferable to make the vertical depletion under the RESURF to occur less in n-Ga_2O_3 (and less impact device R_{ON}).

Prior work showed the N_A of NiO is tunable from 8×10^{17} to >10^{19} cm^{-3} [10]. Hence, N_A^R is selected as 8×10^{17} cm^{-3}. Then

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the N_D and t_D design space is traversed for maximizing the FOM ($BV^2/R_{ON,SP}$) while keeping the E-mode, where BV and $R_{ON,SP}$ are extracted from simulations (Fig. 3a). This process identifies an optimized N_D of ~1.5×10^{18} cm^{-3} (Fig. 3b). Two t_D designs of 50 nm and 160 nm are then determined from Eqn. (1). The first design is conservative assuming no Q_{it}, and the second design is more aggressive considering the reported negative Q_{it} [14].

Two Ga_2O_3 samples are grown by MBE, which consists an n-Ga_2O_3 layer and a UID Ga_2O_3 layer grown on (010) semi-insulating substrate. The N_D and t_D of n-Ga_2O_3 are measured by electrochemical C-V, which are very close to the target designs.

The device fabrication (Fig. 4) starts with Si implantation, activation, and Ohmic contact formation for source and drain. N implantation is used for device isolation. The N_A of NiO is tuned by O_2 partial pressure in sputtering [10]. The hybrid-drain, p^{++}-gate, and RESURF are made sequentially with the NiO sputtered under an Ar/O_2 flow rate of 58/3 sccm, 40/20 sccm, and 60/0 sccm, respectively, resulting in a N_A of 1.5×10^{18},$>10^{19}$, and ~8×10^{17} cm^{-3}, respectively. Devices fabricated on the t_D=50nm sample and t_D=160nm sample are denoted as #A and #B, respectively. On each sample, devices have varying t_A and L_{GD} with an identical gate length (L_G) of 2 µm. The top-view SEM image of the fabricated device is shown in Fig. 4b.

III. Device Characteristics

Fig. 5 shows the output and transfer I-V characteristics of devices #A and #B at 25 °C with L_{GD} of 47 µm and an optimal t_A for respective device to reach BV>10 kV (to be detailed later). Both devices are E-mode with V_{TH} of 1.9 V and 1.5 V for #A and #B, respectively. The E-mode in device #B suggests the existence of negative Q_{it}. The $R_{ON,SP}$ is 703 and 92 mΩ·cm^2 in devices #A and #B, respectively. The 7× higher R_{ON} in device #A, despite a 3.2× thinner t_D, implies a significant contribution of R_{ON} from the gated channel, where the non-depleted Ga_2O_3 channel for current conduction under the gate is much narrower in device #A. For both devices, the V_G operation range is up to 3.5~4 V as limited by the gate leakage current, which is similar to that of the GaN GIT [13], suggesting good compatibility of this Ga_2O_3 JFET with the RC-interface gate driver.

Fig. 6 show the output and transfer characteristics of devices #A and #B at high T. At 250 °C, device #A remains the E-mode with V_{TH} of 0.7 V; the R_{ON} is 1.6 times higher than that at 25 °C. The T-coefficient of R_{ON} is smaller than that reported in 10 kV SiC MOSFET [15], suggesting a lower conduction loss at high T. In contrast, device #B exhibits the inferior thermal stability. Its V_{TH} turns negative at 100 °C and drops to -3.3 V at 150 °C. At T > 175 °C, the gate control becomes insufficient.

Figs. 7a and b show the BV characteristics of devices #A and #B with 47-µm L_{GD} and varying NiO thickness t_A, all tested at V_G=0 V and 25 °C. For each device, BV increases with the increasing t_A, reaching >10 kV at an optimal t_A, and starts to decrease at larger t_A. This behavior shows the BV modulation by charge balance. This is further illustrated by the inverted U-shape in the box plot of BV versus the charge imbalance percentage calculated from the adapted Eqn. (2). BV > 10 kV is achieved near the charge balance condition in both samples.

Fig. 8a and b show the BV versus L_{GD} in both devices, revealing a good BV scalability of 4346/3516 V, 8560/7275 V, and >10 kV in the device #A/#B with L_{GD} of 20, 35, and 47 µm, respectively. The average lateral E-field at BV is 1.75~2.45 MV/cm. Fig. 8c shows the BV of both devices with 47 µm L_{GD} at high T. The BV of device #A maintains >10 kV at T up to 250 °C and V_{GS} = 0 V. The BV of device #B can maintain >10 kV only up to T of 150 °C, and a negative V_{GS} of -10 V is required.

IV. Device Reliability and Physics

Fig. 9 shows the Stress-Measurement-Stress scheme for the reliability tests at 150 °C with two stressors, i.e., V_{GS} = 4 V and V_{DS} = 3 kV. Output & transfer characteristics are intermittently swept in the stress test to monitor the parametric shifts, with the stress time exponentially grown from 1s to 1000s. The device #A and #B both survive the overvoltage HTGB test and show similar behaviors. The V_{TH} and R_{ON} shifts are within 0.32 V and 35 % (Fig. 10a-c), respectively, and they are fully recoverable.

Both devices also survive the 3-kV HTRB test. Device #A shows a V_{TH} and R_{ON} shifts within 0.2 V and 34% (Fig. 10d-e), respectively, while device #B shows a relatively large V_{TH} shift of near -3 V (Fig. 10f). These parametric shifts are fully and mostly recoverable in devices #A and #B, respectively.

For device #B, its negative V_{TH} shift and BV degradation at high T can be explained by the DIBL effect. Fig. 11 shows the simulated potential barrier under the gate at V_D up to 3 kV in devices #A and #B. The thick channel in device #B leads to a lower barrier and punch-through at high V_D. This DIBL can be deteriorated by the Q_{it} and its accelerated de-trapping at high T. This is supported by the negative V_{TH} shift in device #B during the HTRB test. These results suggest a tight gate electrostatic control is essential for HV devices to operate at high T, which may require trading off the $R_{ON,SP}$ like in device #A.

V. Benchmark and Summary

Fig. 12 benchmarks $R_{ON,SP}$ *vs.* BV of our Ga_2O_3 JFETs with other UWBG transistors with BV > 2 kV. The FOM of devices #A and #B with BV >10 kV is at least 142 and 1086 MW/cm^2, respectively, setting a new record in all UWBG transistors with BV > 3 kV. Device #A is also the first E-mode device reported in all >3kV UWBG transistors. Table I lists the key metrics of 5-10 kV transistors reported in SiC [1], GaN [2-5], Ga_2O_3 [7-9], and AlN [16]. Our device demonstrates the highest average E-field, as well as the first report of 250 °C operation and 3 kV reliability data in a HV transistor beyond SiC.

In summary, we demonstrate a 10 kV E-mode Ga_2O_3 JFET with NiO RESURF and hybrid-drain, which can operate up to 250 °C. In addition to performance advance, the comparison between devices #A and #B illustrates the importance of DIBL suppression at high T and kilovolt blocking, which can guide the development of future HV, high-T power transistors.

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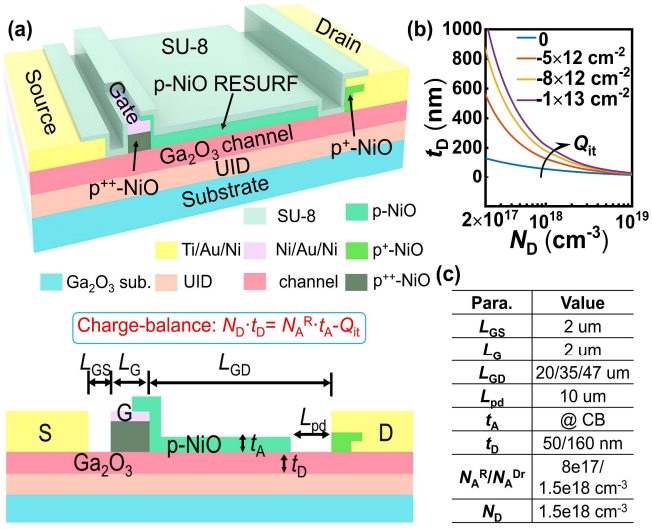
Epi and Device Design and Device Fabrication



Para.	Value
L_{GS}	2 um
L_G	2 um
L_{GD}	20/35/47 um
L_{pd}	10 um
t_A	@ CB
t_D	50/160 nm
N_A^R/N_A^{Dr}	8e17/ 1.5e18 cm^{-3}
N_D	1.5e18 cm^{-3}

Fig. 1. (a) 3-D schematic of the Ga_2O_3 JFET with the p-NiO RESURF and hybrid drain designs. The SU-8 passivation layer is partially removed to show the internal structure. Cross-section view is shown below to illustrate the key geometric parameters and charge-balance (CB) condition. (b) The max channel thickness (t_D) as a function of N_D to achieve the E-mode, for Q_{it} density from 0 to -10^{13} cm^{-2}. (c) The list of key device parameters and values.

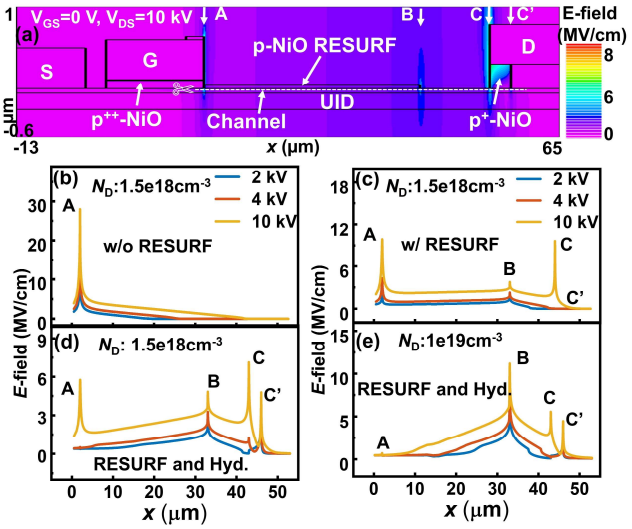


Fig. 2. (a) Simulated E-field contour of the Ga_2O_3 JFET with charge-balance (CB) RESURF and hybrid drain at blocking voltage of 10 kV at V_{GS}=0 V. E-field distributions along cutline of 10 nm below channel surface at different blocking voltages are shown for Ga_2O_3 JFETs (b) without RESURF design, (c) with CB RESURF design, (d) with both CB RESURF and hybrid drain design, all with N_D of 1.5×10^{18} cm^{-3}. The result for a device with the same structure as (d) but with a higher N_D of 10^{19} cm^{-3} is shown in (e). The peak E-fields have the lowest magnitude and are best balanced in structure (d).

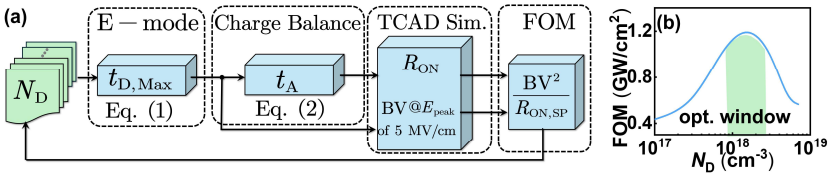


Fig. 3. (a) Flow chart of device optimization by iterating N_D to maximize the device FOM. (b) FOM as a function of N_D. To maximize FOM, an optimized N_D of ~1.5×10^{18} cm^{-3} is derived.

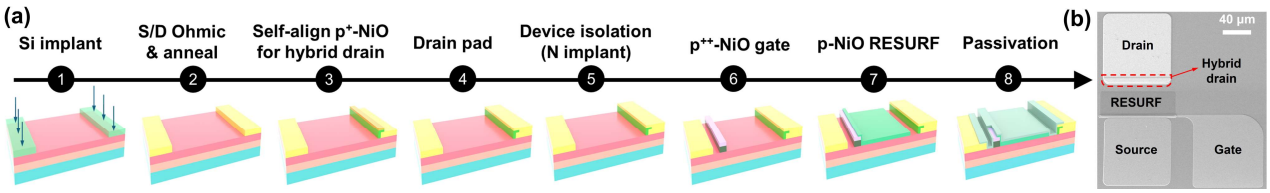


Fig. 4. (a) Schematic illustration of fabrication process flow of the Ga_2O_3 JFET. (b) Top-view SEM image of the fabricated Ga_2O_3 JFET.

Forward Characteristics at Room and High Temperatures

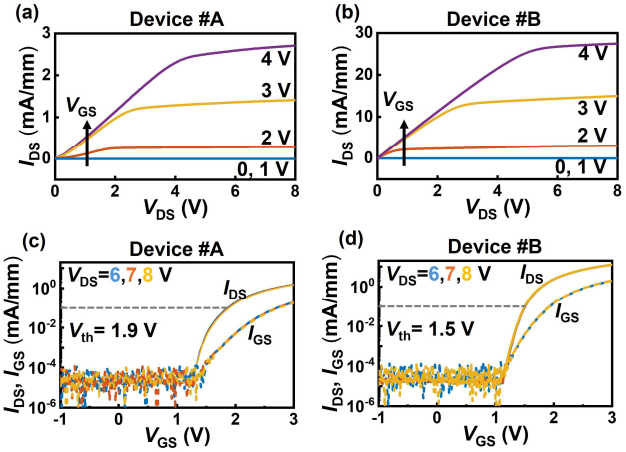


Fig. 5. Output I-V characteristics of devices (a) #A and (b) #B at V_{GS} of 0~4 V at 25 °C. The R_{on} is extracted to be 1302 and 170 Ω.mm, respectively. Transfer I-V characteristics of devices (c) #A and (d) #B at V_{DS} of 6~8 V at 25 °C. V_{TH} is extracted at I_{DS} =0.1 mA/mm. L_{GD} is 47 μm for both devices.

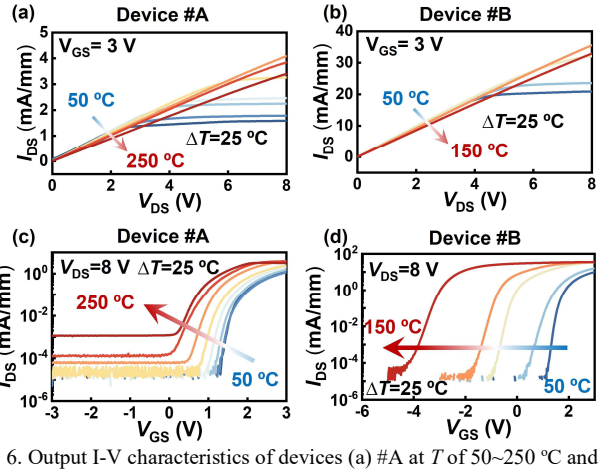


Fig. 6. Output I-V characteristics of devices (a) #A at T of 50~250 °C and (b) #B at T of 50~150 °C at V_{GS}= 3 V. Transfer I-V characteristics of (c) device #A at T of 50~250 °C and (d) device #B at T of 50~150 °C, all measured at V_{DS}= 8 V. Device #A remains the E-mode at 250 °C. L_{GD} is 47 μm for both devices.

Blocking Characteristics at Room and High Temperatures

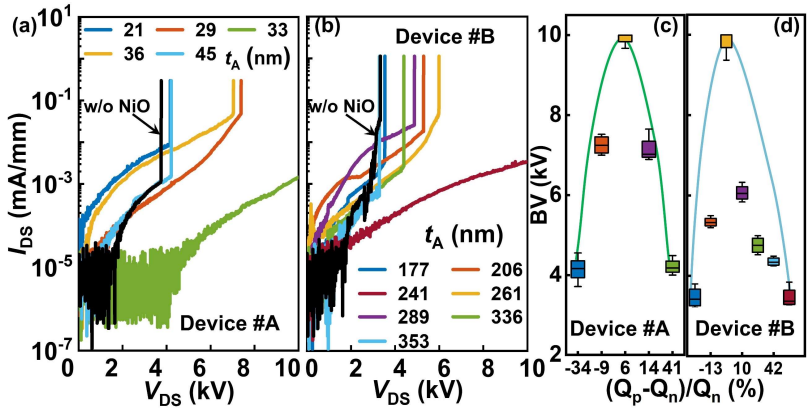


Fig. 7. Off-state I_{DS}-V_{DS} characteristics of devices (a) #A and (b) #B without NiO RESURF and with various NiO RESURF thickness at L_{GD}=47 μm and V_{GS} =0 V. The box plot of BV versus the charge imbalance percentage for devices (c) #A and (d) #B. The measurement limit is 10 kV.

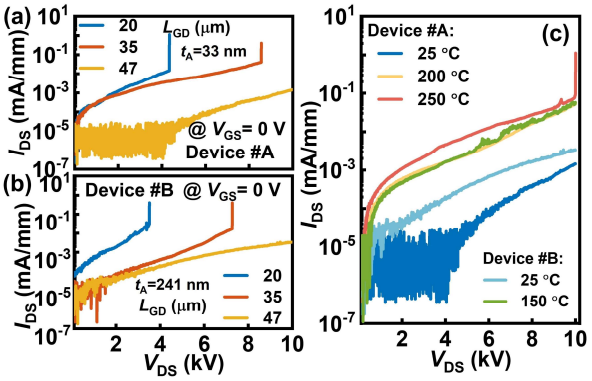


Fig. 8. (a) Off-state I_{DS}-V_{DS} characteristics of devices (a) #A and (b) #B for various L_{GD} under charge-balance and (c) at high temperatures (T). Device #A shows BV > 10 kV up to T=250 °C at V_{GS}= 0 V. Device #B shows BV > 10 kV up to T=150 °C at V_{GS}= -10 V.

Device Reliability and Physical Mechanism

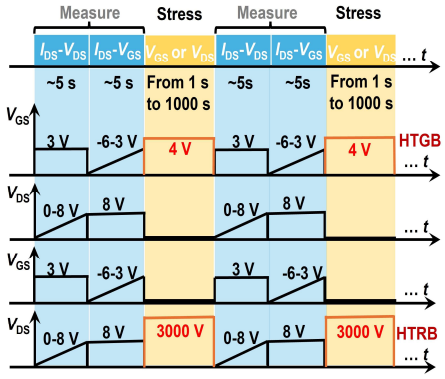


Fig. 9. Schematic illustration of gate and drain reliability stress tests. The HTGB test is stressed at V_{GS}= 4 V, and the HTRB test is stressed at V_{DS}=3 kV, both at T = 150 °C. V_{GS} for I_{DS}–V_{DS} sweep is 3 V, and V_{DS} for I_{DS}–V_{GS} sweep is 8 V.

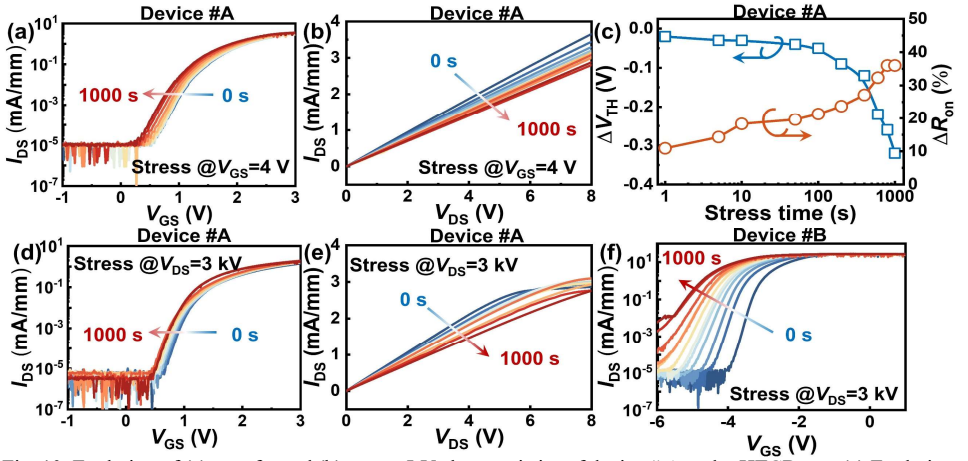


Fig. 10. Evolution of (a) transfer and (b) output I-V characteristics of device # A under HTGB test. (c) Evolution of ΔV_{TH} and ΔR_{on} versus stress time under HTGB test. Evolution of (d) transfer and (e) output I-V characteristics of device # A and (f) transfer I-V characteristics of device # B under the 3 kV HTRB test.

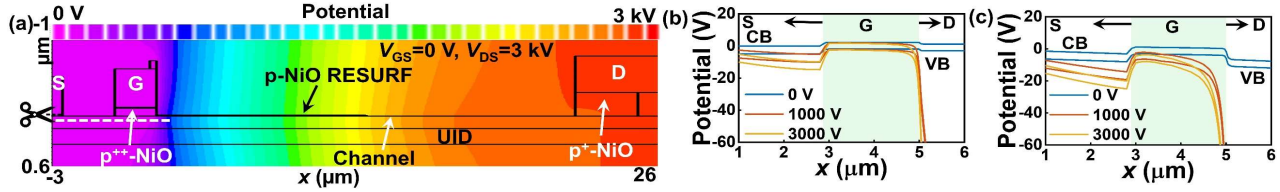


Fig. 11. (a) Simulated potential contour of device #B at V_{DS}= 3 kV and V_{GS}= 0 V. Potential distribution along the cutlines in the Ga_2O_3 channel for devices (b) # A and (c) # B, respectively, at the V_{DS} of 0, 1 kV, and 3 kV. The Q_{it} is also considered in the simulation. Device #B is shown to suffer from the DIBL at high V_{DS}.

Benchmark

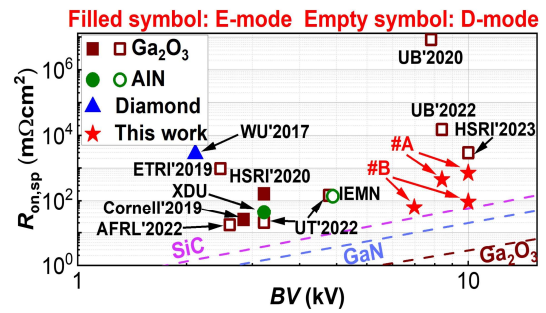


Fig. 12. $R_{ON,SP}$ *vs.* BV benchmark of our Ga_2O_3 JFET and state-of-the-art UWBG power transistors with BV > 2 kV.

TABLE I. Comparison of the state-of-the-art WBG and UWBG power transistors with BV > 5 kV.

Device	Ref.	Key Device	BV (kV)	BV/L_{GD} (MV/cm)	$R_{ON,SP}$ (mΩ·cm²)	D/E-mode, V_{TH}	High-temp.	FOM (MW/cm²)	Reliability
Ga_2O_3 JFET	This work	charge-balance (CB), hybrid drain	>10	1.75~2.45	703 (#A), 92 (#B)	E, 1.9 V (#A)	250°C: $R_{ON,SP}$ 1.6× BV>10kV	142 (#A) 1086 (#B)	HTGB,HTRB (1ks, 150°C)
Ga_2O_3 MOSFET	[7]	field plate	>10	1.1	2922	D, -8V	-	34.2	-
	[8]		8.56	1.43	14954	D, -23V	-	4.9	-
	[9]		8.03	1.15	8.4×10⁶	D, -10V	-	0.0077	-
AlN HEMT	[16]	field plate	4.5	1.13	~150	D, -20V	-	~135	-
SiC MOSFET	[1]	vertical	>10	-	~100	E, 2.2V	200°C: $R_{ON,SP}$ 2.8× [15]	1200	HTGB,HTR (1khr, 150°C)
GaN HEMT	[2]	multi-channel, CB	>10	1.24	40	E, 1.5V	-	2840	-
	[3]	field plate	8	0.8	58	D, -20V	-	1100	-
	[4]	RESURF	6.5	0.85	33.6	D, 0.8	-	1290	-
	[5]	GaN sub	5	1	18	D, -3V	-	1380	-