(Ultra-)Wide-Bandgap Heterogeneous Superjunction: Design, Performance Limit, and Experimental Demonstration

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***Abstract*— Superjunction (SJ) breaks the performance limit of conventional power devices via multidimensional electrostatic engineering. Following a commercial success in Si, it has been recently demonstrated in wide bandgap (WBG) and ultra-WBG (UWBG) semiconductors, including SiC, GaN, and Ga_2O_3. Different from the legacy SJ design based on native p-n junctions, the vertical SJ devices reported in GaN and Ga_2O_3 were built on heterogenous junctions that comprise a foreign p-type material. This hetero-SJ is particularly promising for UWBG materials, in which bipolar doping is difficult. Here, we comprehensively discuss the performance limit, design, and characteristics of the emerging hetero-SJ devices. After a generic performance limit analysis, we use the UWBG Ga_2O_3/NiO SJ diode as an example to showcase the design guideline, fabrication, and performance of hetero-SJ devices. The emphasis is placed on a self-align process to deposit p-NiO around n-Ga_2O_3 pillars and the impact of the p-NiO thickness inhomogeneity on the device breakdown voltage (*BV*). Such process and device physics are uniquely relevant to hetero-SJ devices. The fabricated SJ diode achieves a *BV* over 2 kV and a specific ON-resistance of 0.7 m$\Omega \cdot$ cm^2, the tradeoff of which is among the best in kilovolt Schottky barrier diodes (SBDs). These results provide key references for the future development of hetero-SJ devices in diverse material systems.**

***Index Terms*— Breakdown voltage (*BV*), Ga_2O_3, GaN, NiO, power electronics, superjunction (SJ), ultra wide bandgap (UWBG), wide bandgap (WBG).**

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I. Introduction

POWER semiconductor devices, which have a market size over U.S. $40 billion [1], are utilized as solid-state switches in power electronics systems. The overarching design target of a unipolar power device is to achieve a low specific ON-resistance ($R_{ON,SP}$), a high breakdown voltage (BV), and a low switching power loss. The performance advance of power devices relies on innovations in semiconductor materials or device architectures and, ideally, their synergistic combinations. The use of wide bandgap (WBG) and ultra-WBG (UWBG) materials, such as SiC, GaN, Ga_2O_3, AlN, and diamond [2], [3], in conjunction with the multidimensional architectures, such as superjunction (SJ), multichannel, and multigate [1], is the most promising pathway to improve the $BV \sim R_{ON,SP}$ tradeoff of unipolar power devices.

To date, SJ is arguably one of the most successful multidimensional power devices. It is built on the alternative p-type and n-type regions in charge balance [Fig. 1(a)], resulting in a net zero charge. Such zero charge enables a more uniform electric field (E-field), which is favorable for BV scaling with device length or depth, and allows for increasing the doping concentration in the n- or p-type region, whichever conducts current in the device ON-state to lower $R_{ON,SP}$ [4], [5]. Vertical SJ devices enable an $R_{ON,SP}$ limit linearly increase with BV, which is superior to the $R_{ON,SP} \propto BV^{2\sim2.6}$ limit of conventional 1-D devices. Lateral SJ devices, despite having an $R_{ON,SP} \propto BV^2$ limit, can still outperform the 1-D counterparts due to the more uniform E-field and higher doping [5].

The SJ devices in Si have reached commercialization in the late 1990s [6], [7], and its market is now over U.S. $1 billion [5]. On the other hand, the theoretical performance limit of SJ devices, regardless of the form factor, can be improved by deploying the materials with a higher $\varepsilon\mu E_c^{2\sim3}$, where ε,

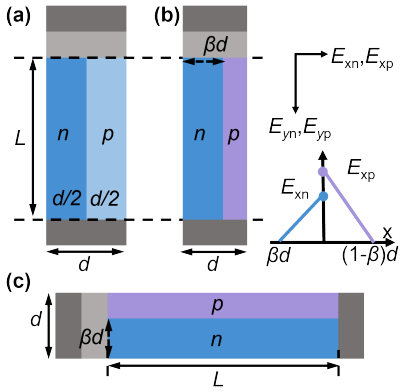


Fig. 1. Schematic of a unit cell of (a) vertical homogeneous, symmetric SJ, (b) vertical heterogeneous, asymmetric SJ, and (c) lateral heterogeneous, asymmetric SJ. The lateral E-field in the vertical hetero-SJ is shown in (b).

μ, and E_C are the permittivity, majority carrier mobility, and critical E-field, respectively [1]. This has motivated extensive research on developing SJ devices in WBG and UWBG materials. Since 2016–2018, vertical SiC SJ devices have been widely reported with the performance exceeding the 1-D SiC limit [8], [9], [10], [11], [12], [13], [14]. In 2022–2023, vertical SJ devices have also been demonstrated in GaN [15], [16] and Ga_2O_3 [17]. Meanwhile, lateral SJ devices building on diverse forms of charge balance (e.g., impurity dopants and polarization) have been reported in GaN [18], [19], [20], [21], [22], [23] and Ga_2O_3 [24], [25] with the performance exceeding the 1-D lateral devices based on the respective material.

The legacy SJ devices in Si and SiC are built on native p-n junctions formed by epitaxial regrowth or ion implantation, or their combinations. Differently, heterogeneous p-n junctions were adopted in the recent demonstration of vertical SJs in GaN and Ga_2O_3 [15], [16], [17]. This is due to the difficulties in selective-area p-type doping in GaN through either regrowth [26] or implantation [27], as well as the absence of effective p-type doping in Ga_2O_3 [28]. Alternatively, a WBG p-type oxide, nickel oxide (NiO), was deployed to construct the hetero-SJs with n-GaN and n-Ga_2O_3. The NiO was selected primarily due to its WBG (3.4–4 eV) and high E_C up to 3.8–6.3 MV/cm [29], tunable acceptor concentration (N_A) from $\sim 5 \times 10^{17}$ and $>10^{19}$ cm^{-3} [29], [30], [31], and its capability to form nonleaky p-n junctions on nonplanar GaN and Ga_2O_3 structures. In addition, robust avalanche and surge current robustness have been demonstrated in Ga_2O_3/NiO heterojunction [32].

This new approach opens the door for implementing SJ in other UWBG materials beyond Ga_2O_3, which are all difficult to achieve the intrinsic bipolar doping [3]. For example, the n-Ga_2O_3/p-diamond [33], [34] and n-GaN/p-diamond hetero-SJ devices [35] were recently proposed with simulations. However, several knowledge gaps stand between these device ideas and their development: 1) what are the performance limit and design guideline of hetero-SJ devices? 2) how to fabricate them? and 3) are there process-induced nonideal device characteristics?

Here, we answer these questions based on the learnings from the development of hetero-SJs in GaN and Ga_2O_3. Due to the difficulties to precisely match the donor concentration (N_D) and N_A in distinct materials, the hetero-SJ geometry is expected to be asymmetric [Fig. 1(b) and (c)]. To this end, we first extend the SJ theory to the asymmetric hetero-SJ. We then use Ga_2O_3/NiO SJ diodes as a case study to illustrate the practical design procedure, self-align fabrication process, and device characteristics that are widely applicable to diverse hetero-SJ devices. In particular, the breakdown mechanism as modulated by charge imbalance and impacted by process nonidealities is analyzed. Note that this article is considerably different from our prior conference paper [17] by discussing the theory and experiments in a more generic manner; in comparison, [17] also contains circuit-test results of the Ga_2O_3/NiO hetero-SJ diode.

II. Performance Limit

Fig. 1(b) and (c) shows the unit-cell schematic of a vertical and lateral hetero-SJ, respectively. d is the cell pitch, and β is the ratio between the n-pillar width and cell pitch ($0 < \beta < 1$). Upon charge balance, β is determined by N_D and N_A

$$\beta = N_A/(N_A + N_D). \tag{1}$$

The breakdown of hetero-SJ devices is limited by the n-type or p-type material with the lower εE_c. The modeling below first considers the breakdown to be limited by the n-type material ($\varepsilon_n E_{cn}$). For simplicity, the JFET effect and doping-dependent mobility are not considered. Their impacts can be applied to hetero-SJs similar to homogeneous SJs [36].

In the vertical SJ, as shown in Fig. 1(b), the peak lateral E-field in the n-type pillar, E_{xn}, is given by

$$E_{xn} = \alpha E_{cn} = \frac{qN_D\beta d}{\varepsilon_n}, \quad (0 < \alpha < 1) \tag{2}$$

where ε_n is the permittivity of the n-type material, and α is the ratio between E_{xn} and E_c. The vertical E-field in the n-pillar, E_{yn}, is

$$E_{yn} = E_{cn}\sqrt{1-\alpha^2}. \tag{3}$$

The BV of the vertical SJ can be derived as

$$\begin{aligned} BV &= \frac{1}{2}\alpha E_{cn}\beta d + \frac{1}{2}\frac{\alpha E_{cn}\varepsilon_n}{\varepsilon_p}(1-\beta)d + E_{yn}L \\ &\approx E_{yn}L = E_{cn}L\sqrt{1-\alpha^2} \end{aligned} \tag{4}$$

where ε_p is the permittivity of the p-type material and L is the SJ length. The ideal $R_{ON,SP}$ of the SJ region can be written as

$$R_{ON,SP} = \frac{L}{qN_D\mu_n}\frac{1}{\beta} \tag{5}$$

where μ_n is the mobility of n-type material. From (2), (4), and (5), the figure-of-merit (FOM) of the vertical SJ is

$$\begin{aligned} \text{FOM} &= \frac{BV}{R_{ON,SP}} = \frac{\alpha\sqrt{1-\alpha^2}\mu_n\varepsilon_n E_{cn}^2}{d} \\ \alpha &= \frac{qN_D\beta d}{\varepsilon_n E_{cn}}. \end{aligned} \tag{6}$$

TABLE I
ANALYTICAL EQUATIONS FOR $R_{ON,SP}$, FOM, AND OPTIMAL DESIGN OF VERTICAL AND LATERAL SJ

Type of device		$R_{ON,SP}$	FOM	α and optimal design
vertical homo SJ	symmetric	$\frac{BV}{\alpha\sqrt{1-\alpha^2}\mu_n\varepsilon {E_c}^2}d$	$\frac{BV}{R_{ON,SP}}=\frac{\alpha\sqrt{1-\alpha^2}\mu_n\varepsilon_n {E_c}^2}{d}$	$\frac{qN_Dd}{2\varepsilon E_c}=\frac{1}{\sqrt{2}}$
vertical hetero SJ	asymmetric, n-limited	$\frac{BV}{\alpha\sqrt{1-\alpha^2}\mu_n\varepsilon_n {E_{cn}}^2}d$	$\frac{BV}{R_{ON,SP}}=\frac{\alpha\sqrt{1-\alpha^2}\mu_n\varepsilon_n {E_{cn}}^2}{d}$	$\frac{qN_D\beta d}{\varepsilon_n E_{cn}}=\frac{1}{\sqrt{2}}$
	asymmetric, p-limited	$\frac{BV}{\alpha\sqrt{1-\alpha^2}\mu_n\varepsilon_p {E_{cp}}^2}d$	$\frac{BV}{R_{ON,SP}}=\frac{\alpha\sqrt{1-\alpha^2}\mu_n\varepsilon_p {E_{cp}}^2}{d}$	$\frac{qN_D\beta d}{\varepsilon_p E_{cp}}=\frac{1}{\sqrt{2}}$
lateral hetero SJ	asymmetric, n-limited	$\frac{BV^2}{\alpha(1-\alpha^2)\mu_n\varepsilon_n {E_{cn}}^3}$	$\frac{BV^2}{R_{ON,SP}}=\alpha(1-\alpha^2)\mu_n\varepsilon_n {E_{cn}}^3$	$\frac{qN_D\beta d}{\varepsilon_n E_{cn}}=\frac{1}{\sqrt{3}}$

Similarly, if the breakdown is limited by the p-type material, the FOM of the vertical SJ can be expressed as

$$\text{FOM}=\frac{\alpha\sqrt{1-\alpha^2}\mu_n\varepsilon_p E_{cp}^2}{d},\quad \alpha=\frac{qN_D\beta d}{\varepsilon_p E_{cp}}. \tag{7}$$

The FOM of a lateral hetero-SJ is $BV^2/R_{ON,SP}$, which can be written as (assuming the breakdown is limited by the n-type material)

$$\text{FOM}=\frac{BV^2}{R_{ON,SP}}=\alpha\left(1-\alpha^2\right)\mu_n\varepsilon_n E_{cn}^3$$
$$\alpha=\frac{qN_D\beta d}{\varepsilon_n E_{cn}}. \tag{8}$$

From (6) to (8), optimal design is attained when the parameter α equals to $1/\sqrt{2}$ and $1/\sqrt{3}$ for the vertical and lateral SJs, respectively. The analytical models for $R_{ON,SP}$, FOM, and optimal design conditions of these hetero-SJs, in comparison with the homogeneous SJ, are summarized in Table I.

As a reference, Fig. 2(a) illustrates the $R_{ON,SP}$ and BV tradeoff of hypothetical SJ devices based on various WBG and UWBG materials, assuming the availability of an ideal, shallow-level bipolar doping in all these materials. The SJ performance limit of each material is a band that can be continuously improved by downscaling the cell pitch.

For a vertical asymmetric hetero-SJ based on the selected materials, its performance depends on three parameters, d, β, and N_D (or equivalently, d, N_A, and N_D). In addition to optimal designs, the SJ performance in the suboptimal regimes is critical, as it determines the processing windows in the practical device fabrication. Here, we consider a common case that an n-type epitaxial structure is predetermined, i.e., a fixed N_D, and look into the geometrical modulation by both d and β.

Fig. 2(b)–(d) depicts the SJ FOM as a function of β across various d for the vertical GaN/NiO, vertical Ga_2O_3/NiO, and lateral Ga_2O_3/NiO hetero-SJs, all with an exemplar N_D of 2×10^{17} cm^{-3}. As E_C of NiO is between that of GaN and Ga_2O_3, the GaN/NiO SJ and Ga_2O_3/NiO SJ represent the hetero-SJs, in which the breakdown is limited by the n-type and p-type materials, respectively.

In vertical SJs with a fixed N_D, for each d, there exists an optimal β to maximize the FOM. The d downscaling

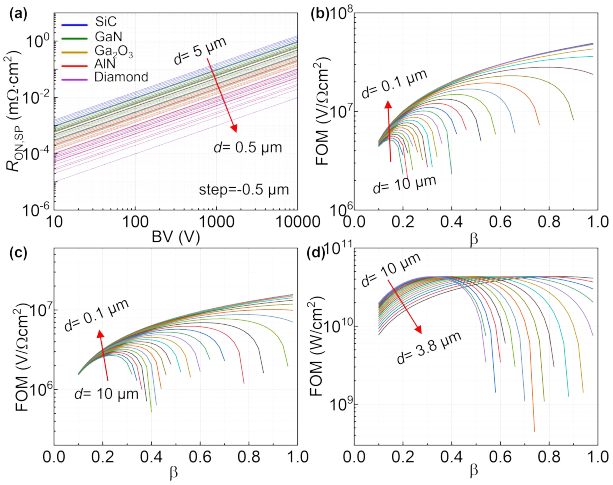


Fig. 2. (a) $R_{ON,SP}$-BV tradeoff of ideal vertical homogeneous SJs based on WBG and UWBG materials for d ranging from 5 to 0.5 μm. The FOM of vertical hetero-SJ as a function of β for different d values for (b) GaN/NiO and (c) Ga_2O_3/NiO hetero-SJs. (d) FOM of lateral Ga_2O_3/NiO hetero-SJ as a function of β for different d values. The E_c values of GaN, NiO, and Ga_2O_3 are assumed to be 3.5, 5, and 8 MV/cm, respectively. The d step is -0.4 μm from 10 to 1 μm and -0.1 μm from 1 to 0.1 μm.

not only improves the SJ FOM but also broadens the design window for β. For example, to achieve >80% of the max FOM, the allowable β range expands at lower d, and the optimal β moves toward unity. This inverse relation between d and the β window suggests an inherent tradeoff between the requirements of processing technologies (e.g., demanding lithography) and the precise control of doping concentration.

For a lateral hetero-SJ, as depicted in Fig. 2(d), the max FOM is independent of d. As d shrinks, the optimal β moves toward unity to meet the $\alpha=1/\sqrt{3}$ condition, suggesting a higher N_A. Similar to vertical hetero-SJ, the β window expands as d shrinks. For example, to achieve 80% of the max of FOM, the β window increases from 0.19–0.43 to 0.51–0.98 when d decreases from 10 to 3.8 μm. This suggests a similar tradeoff between the accuracies required for thickness control and doping control.

Note here that the SJ models do not consider the dopant incomplete ionization, the dependence of mobility and critical electric field on doping concentration, as well as the contact

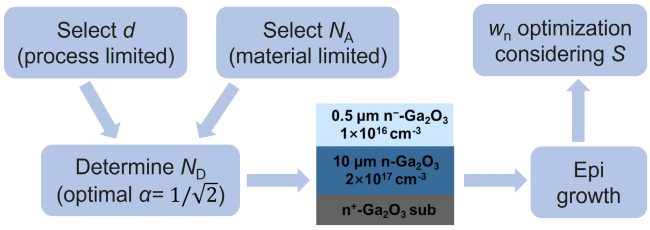


Fig. 3. Practical design flow for the Ga_2O_3/NiO SJ device.

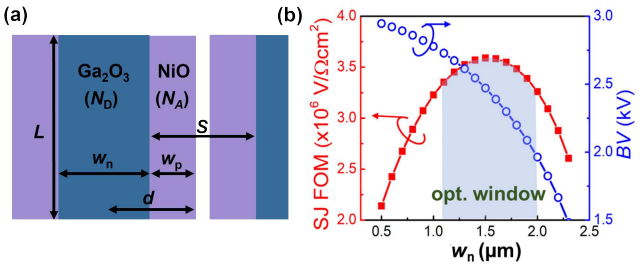


Fig. 4. (a) Schematic of the practical Ga_2O_3/NiO hetero-SJ structure with the n-pillar spacing much larger than the sidewall p-material thickness. (b) Modeled Ga_2O_3/NiO hetero-SJ FOM and BV as a function of w_n. $L = 6.5$ μm.

resistance in practical devices. These factors could become significant for some UWBG materials, such as AlN and diamond, in which the shallow dopant is still lacking. A recent study reveals the strong impact of the dopant energy level on the performance of 1-D power devices based on UWBG semiconductors [37], and such impact is also expected for UWBG SJs. Future work is needed to develop SJ models that are aware of these material and device nonidealities.

III. Practical Design and Fabrication

In this section, we use the vertical Ga_2O_3/NiO SJ Schottky barrier diode (SBD) as a case study to illustrate the practical design guidelines for epitaxial structure and device geometries, as well as a self-aligned fabrication process.

A. Design Procedure

The flowchart of the device and epidesign is shown in Fig. 3. d is first selected to be 2–3 μm considering the lithography capabilities in a university cleanroom and the controllability to etch high aspect ratio trenches with a target depth of 6–7 μm. The second constraint is the available N_A range of p-NiO. Our prior work has found that N_A of NiO can be tuned by the oxygen partial pressure in magnetron sputtering, i.e., $\sim 8 \times 10^{17}$, $\sim 1.5 \times 10^{18}$, $\sim 2 \times 10^{18}$, and $> 10^{19}$ cm^{-3} under four different Ar:O_2 gas flow ratios (pure Ar, 20:1, 8:1, and 2:1), with the resistivity of 84, 6.9, 0.53, and $\sim 10^{-3}$ Ω·m, respectively [29]. Here, we select N_A of 1.5×10^{18} cm^{-3}, which is close to the lower end and maintains considerable conductivity. Note that NiO conductivity is not critical for the SJ conduction, as all current is flowing in the n-pillar; however, a very low conductivity may lead to resistive loss during the hole removal and supply when the device is switched off and on [38].

Once N_A and d are determined, N_D can be calculated to be 1.2×10^{17} cm^{-3} from $\alpha = 1/\sqrt{2}$ and (1) and (7), assuming the SJ breakdown is limited by NiO with an E_c of $\sim$5 MV/cm. This N_D is at least 10 times higher than the usual value used in 1-D vertical Ga_2O_3 devices, showcasing the key feature of SJ. Based on this target N_D, a bilayer Ga_2O_3 epitaxy comprising a 10-μm n-Ga_2O_3 drift region for SJ fabrication and a 0.5-μm n$^-$-Ga_2O_3 cap layer is grown on 2-in (001) n$^+$-Ga_2O_3 substrate by Novel Crystal Technology, Inc. The lowly doped cap layer is designed to lower the tunneling leakage current of the Schottky contact. The electrochemical C–V tests reveal a net N_D of 10^{16} and 2×10^{17} cm^{-3} in the as-grown n$^-$-Ga_2O_3 and n-Ga_2O_3 layers, respectively. Note that a similar design process was employed for our prior GaN/NiO hetero-SJ diodes [15], [16]. From the same N_A and d, the target N_D ($\sim 7 \times 10^{16}$ cm^{-3}) used in the epigrowth is calculated from $\alpha = 1/\sqrt{2}$ and (1) and (6). The only distinction is the breakdown is assumed to be limited by GaN instead of NiO.

The large discrepancy between the determined N_D and N_A suggests that the hetero-SJ is strongly asymmetric. In theory, the widths of n-pillars and p-pillars can be readily calculated, which, however, can be complicated by another processing issue. Our prior work found that the NiO deposition rate at the planar surface is higher than that at the trench sidewall, leading to the risk of early NiO coalescence at the top of trench, which prevents the further NiO deposition onto the pillar sidewall [15]. To address this challenge, a Ga_2O_3 pillar spacing (S) much larger than the target NiO sidewall thickness (w_p) is needed. As shown in Fig. 4(a), the device $R_{ON,SP}$ is modified as

$$R_{ON,SP} = \frac{L}{qN_D\mu_n}\frac{w_n + S}{w_n} \tag{9}$$

where $w_n = 2\beta d$ is the n-Ga_2O_3 pillar width. This modification makes the optimal w_n less explicit and unable to be directly calculated from an optimal α value. Instead, (9) is combined with the adapted (2) and (3) for NiO to numerically calculate the SJ FOM as a function of w_n. Here, a constant S of 1.5 μm is adopted from the processing experience. As shown in Fig. 4(b), the calculation results suggest a continuous drop of BV with the increased w_n but a max FOM at an optimal w_n of $\sim$1.6 μm. A w_n window of 1–2 μm is determined from Fig. 4(b) and adopted in the mask design.

B. Self-Aligned Fabrication Process

The homogenous SJs are primarily fabricated in two methods: 1) multicycles of epitaxy and ion implantation and 2) trench-filling regrowth. For NiO-based hetero-SJs, a new fabrication process similar to trench-filling regrowth has been established, which conformally sputters NiO into deep trenches at room temperature [16], [17]. A challenge of this process is the removal of NiO deposited on the top surface, which is essential to expose the n-type material for contact formation. The dry etch of NiO is known to be difficult, and a precise lithography alignment to n-pillars is also challenging. Alternatively, the chemical mechanical polishing is widely used in removing the overgrown material in the trench-filling

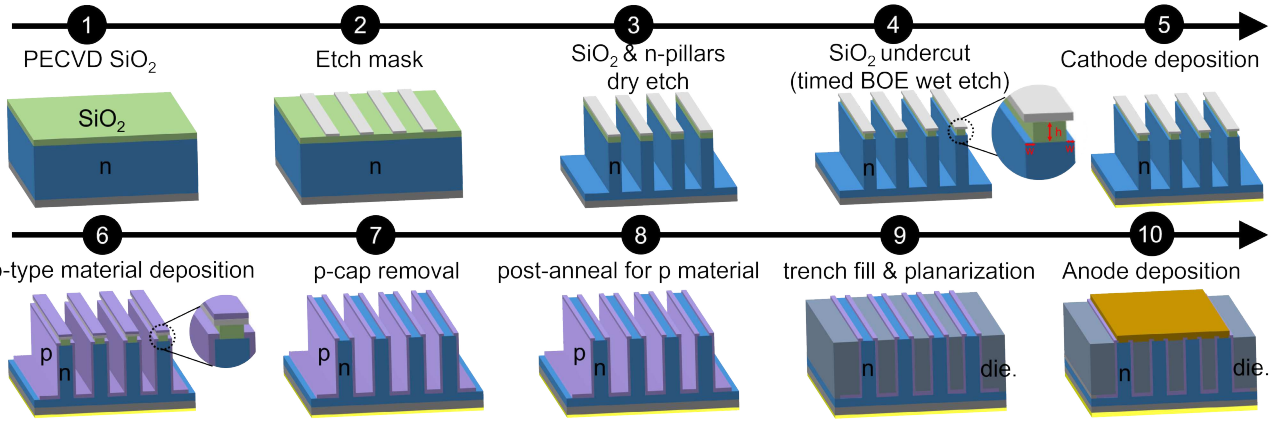


Fig. 5. Main steps in the fabrication process of the hetero-SJ SBD. The process highlights a self-aligned NiO cap removal (step #7) using the SiO_2 with undercut produced in step #4. The insets of steps #4 and #6 show the enlarged view of the undercut before and after the p-type material deposition.

regrowth process [14]. However, it suffers from an inaccurate thickness control and may not be suitable for removing the relatively thin NiO.

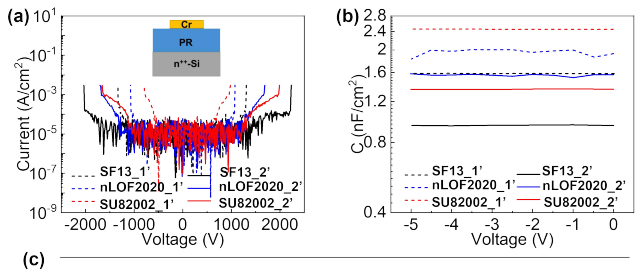
Here, we demonstrate a self-aligned, dry-etch-free, lithography-free process to sputter NiO and remove the NiO cap. Fig. 5 shows the main steps to fabricate a Ga_2O_3/NiO hetero-SJ SBD. A thick SiO_2 layer is first deposited, followed by the deposition of hard mask. The Ga_2O_3 pillars are formed by dry etching. Steps #4, #6, and #7 show the self-align process. An undercut in the SiO_2 is generated by a timed BOE wet etch. After the conformal NiO sputtering under an Ar/O_2 flow rate of 58/3 sccm (and other conditions identical to [29]), a long rinse in BOE lifts off the p-NiO cap. For this process, the width (w) and height (h) of the SiO_2 undercut are critical. Sufficient w and h are required to enable the lift-off process. Nonetheless, an increased w may result in excessive coverage of p-type material atop the n-pillars, elevating the device $R_{ON,SP}$; in addition, a larger h could induce stress and cause the entire SiO_2 layer to delaminate in step #4. In our process, w and h are optimized to be about 200 nm and 500–1000 nm, respectively. The BOE etch time in steps #4 and #7 is 30 s and 10 min, respectively.

Deep plasma dry etching and sputtering of NiO can induce sidewall surface damage, leading to the formation of surface charges at the NiO/Ga_2O_3 interface. These interface charges present significant challenges for both the design and performance assessment of SJ devices. Such charges could disrupt the charge balance within the SJ drift region and induce parasitic leakage currents and premature breakdown. Additionally, the design tolerances for pillar width and doping concentration could be constrained. Therefore, interface charges should be considered for the design optimization and minimized in the device fabrication. In this study, postannealing at 275 °C in an N_2 atmosphere was performed in step #8 to reduce the interface charges.

As S is designed to be much larger than w_p to avoid the surface NiO coalescence, a spacing is left in the trench after the NiO sputter. This spacing region needs to be effectively filled, as it would see high E-field (more specifically, E_y) in the device blocking state. While various dielectrics can be deployed for this passivation, here we show an easy filling process using the photoresist (PR). This process is similar to that previously developed for the power FinFET fabrication [39], [40], [41]. A thick PR is first blanketly coated to fill all trench spacings and cover the wafer surface, followed by a timed planarization etch in O_2 plasma until the top surface of n-pillars are exposed.

Although the E-field in PR is expected to be lower than that in the SJ, a high εE_c is desirable for the PR material. To this end, we measure the breakdown field (E_B) and ε of several candidate PRs, including the SF13, nLOF 2020, and SU8 2002. A test structure consisting of a top metal contact and a PR layer on an n^{++}-Si wafer is used for such measurement. For each PR, two test structures with different PR thicknesses are fabricated, i.e., 1.92/3.6, 1.65/2.35, and 1.47/2.42 μm for SF13, nLOF 2020, and SU8 2002, respectively. Fig. 6(a) and (b) shows the I–V and C–V characteristics of these six test structures. The measured E_B and ε of three PRs are summarized in Fig. 6(c). The nLOF shows the highest εE_B value. Furthermore, nLOF and SU8 can survive the acetone and developer used in the final anode lift-off. In addition, nLOF can be removed by AZ400T, which does not attack NiO, allowing the rework to be flexible performed for this step. Considering these factors, the nLOF 2020 has been selected for our device fabrication.

Fig. 7(a) shows the schematic of the fabricated Ga_2O_3/NiO hetero-SJ SBD. The SJ length, L, is about 6.5 μm. A metal stack of Ni/Au/Ti/Ag is used for the anode, which forms an ohmic contact to NiO and a Schottky contact to Ga_2O_3. The ohmic to NiO guarantees fast hole extraction and supply. Fig. 7(b) shows the scanning electron microscopy (SEM) image after the self-align process, confirming the removal of NiO caps and the exposure of Ga_2O_3 surface. Fig. 7(c) and (d) shows the cross-sectional SEM images of the Ga_2O_3 pillar in the top and bottom regions, respectively. As the NiO deposition rate at the planar surface is higher than the vertical sidewall, the NiO thickness at the sidewall is found to slightly decrease in the top ~2 μm and keep constant (w_p ~ 104 nm) in the remaining ~4.5 μm. The NiO thickness at the trench bottom is ~200 nm, suggesting



(c)

Photoresist	Breakdown field (MV/cm)	Dielectric constant	Compatibility with developer	Compatibility with acetone	Strip
SF13	5.9-7.3	3.4-3.9	×	√	Remover PG
nLOF2020	6.5-7.1	3.7-4.0	√	√	AZ400T
SU8 2002	6.0-6.9	3.7-4.0	√	√	Piranha

Fig. 6. (a) *I–V* and (b) *C–V* characteristics of different PRs with two thicknesses. The schematic of the test structure is shown in the inset of (a). (c) Summary of the extracted dielectric breakdown field and dielectric constant as well as the process compatibilities of different PRs.

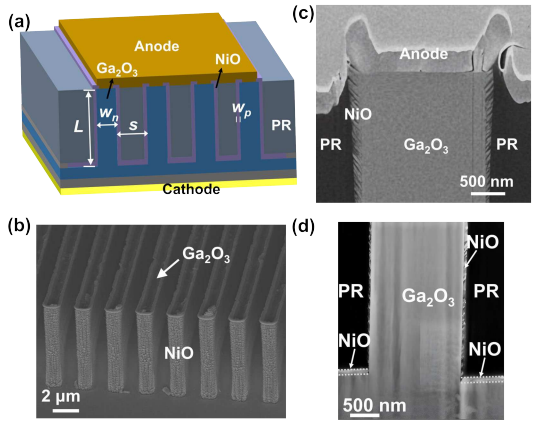


Fig. 7. (a) Three-dimensional schematic of the vertical Ga_2O_3 hetero-SJ SBD. (b) SEM image of the Ga_2O_3 pillars after the self-align NiO deposition and cap removal. Cross-sectional SEM images of (c) top and (d) bottom SJ regions.

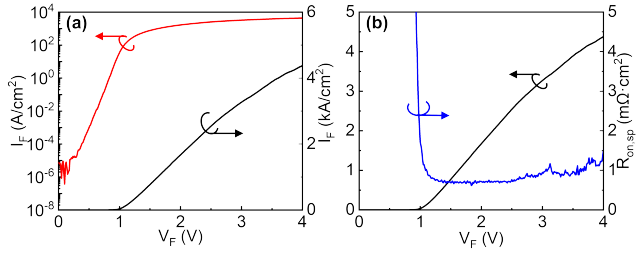


Fig. 8. (a) Forward *I–V* characteristics (semi-log and linear scales) and (b) extracted differential $R_{ON,SP}$ of the Ga_2O_3/NiO hetero-SJ SBD with w_n of 1.6 μm and w_p of 104 nm.

a deposition rate about 2 times higher than that at the sidewall.

C. Device Characteristics

Fig. 8 shows the ON-state *I–V* characteristics and the extracted differential $R_{ON,SP}$ of the fabricated Ga_2O_3/NiO hetero-SJ SBD. w_n is 1.6 μm and w_p is 104 nm. Current density and $R_{ON,SP}$ are normalized to the entire anode area. The SJ SBD shows a turn-on voltage of 1 V, an ON/OFF ratio of 10^9, and a minimum differential $R_{ON,SP}$ is 0.7 mΩ·cm^2.

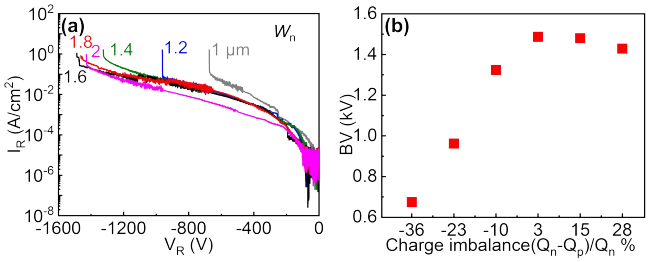


Fig. 9. (a) Reverse *I–V* characteristics of the Ga_2O_3/NiO hetero-SJ SBDs with w_n of 1–2 μm and an identical w_p = 104 nm. (b) *BV* as a function of charge imbalance percentage for the SJ-SBDs with six w_n (1–2 μm).

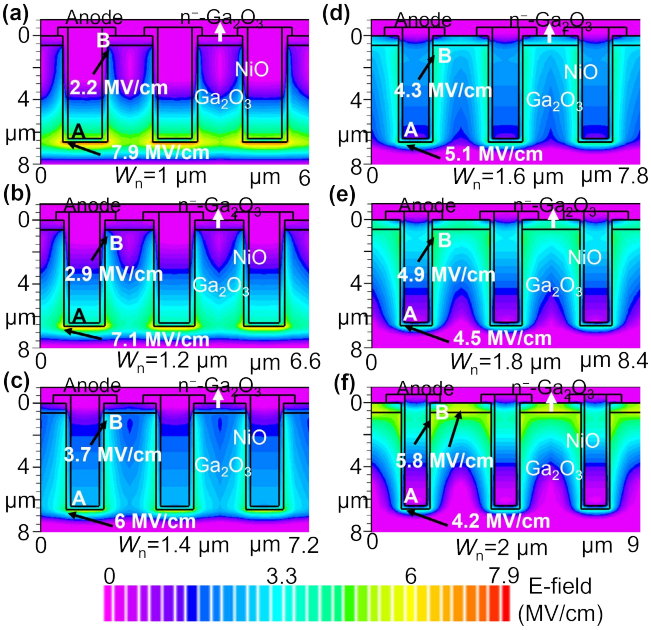


Fig. 10. Simulated *E*-field contour of the Ga_2O_3/NiO hetero-SJ SBDs with different w_n of (a) 1 μm, (b) 1.2 μm, (c) 1.4 μm, (d) 1.6 μm, (e) 1.8 μm, and (f) 2 μm and an identical sidewall wp of 104 nm at −1500 V. The peak *E*-fields at the trench corner and the n-pillar top are marked.

Fig. 9(a) shows the reverse characteristics of the hetero-SJ SBDs with various w_n and an identical w_p of 104 nm. The *BV* initially rises with an increase w_n, surpassing 1500 V at w_n of 1.6 μm, subsequently declining with larger w_n values. This showcases the modulation effect of charge balance on *BV*. The *BV* as a function of the calculated charge imbalance percentage is shown in Fig. 9(b). While the highest *BV* is achieved near the charge balance condition, the *BV* trends in the n-excessive and p-excessive regimes show an asymmetric pattern, which is different from the ideal SJ theory. This phenomenon, as well as the *BV* of hetero-SJ devices with two additional w_p of 90 and 120 nm, will be discussed in the next section.

IV. Breakdown Mechanism

TCAD simulations are employed to explore the breakdown locations in the Ga_2O_3/NiO hetero-SJ SBD under various charge (un)balance conditions. The simulation model is based on [31] and [32]. Fig. 10 shows the simulated *E*-field contours of the hetero-SJ SBDs with different w_n values at a reverse

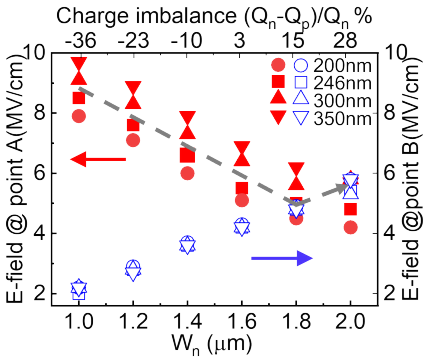


Fig. 11. Evolution of the simulated E-fields at point A (trench corner) and point B (n-pillar top) for varying NiO thicknesses at the trench bottom. w_n ranges from 1 to 2 μm. $w_p = 104$ nm. The dashed arrow shows the highest E-field in the device structure.

bias of 1500 V. The NiO thicknesses at the sidewall and trench bottom are 104 and 200 nm, respectively. As w_n increases, the peak E-field is initially located at the trench corner (point #A) when the SJ is p-excessive, and it transitions to the top region of the n-pillar (point #B) when the SJ is n-excessive. Note that point #B can be either near the sidewall junction or in the middle of the n-pillar, depending on the degree of n-type excess charges. Since the breakdown is determined by these two points when w_n is smaller and larger than the charge-balance condition, the sensitivity of the peak E-field on w_n at respective location determines the $BV \sim w_n$ relation under n-excessive and p-excessive conditions.

Fig. 11 shows the simulated E-fields at points #A and #B as a function of w_n for various NiO thicknesses at the trench bottom. The thicker NiO at the trench bottom is found to elevate the E-field at point #A, which could result in a faster drop of BV when the SJ is under p-excessive condition. On the other hand, the peak E-field at point #B is nearly independent of the NiO thickness at the trench bottom, suggesting the weak impact of this thickness on BV when the SJ is under the n-excessive condition. Such nonuniversal impact on BV is an important cause of the observed asymmetric pattern in the plot of BV versus charge imbalance percentage shown in Fig. 9.

The BV pattern on w_n or charge imbalance percentage is also impacted by w_p. Fig. 12(a) shows the reverse I–V characteristics of devices with different w_p values of 90, 104, and 120 nm and w_n ranging from 1 to 2 μm for each w_p. The NiO thickness at the trench bottom is about twice of each w_p. The box plot of BVs as a function of w_n for three w_p is shown in Fig. 12(b), in which the data of five devices are included for each condition to show the statistical significance. These BV data are replotted versus the charge imbalance percentage in Fig. 12(c). At $w_p = 120$ nm and $w_n = 1.8$ μm, the BV of several devices reaches 2000 V. The slope of BV versus w_n is found to differ for different w_p values, and the slope could be asymmetric in the n- and p-excessive regimes for the same w_p.

Fig. 12(d) shows the evolution of the simulated peak E-fields at points #A and #B when w_n increases from 1 to 2 μm in the devices with three w_p. For each w_p, the simulated critical w_n when two peak E-fields become comparable agrees with the one at which the experimental BV is the highest.

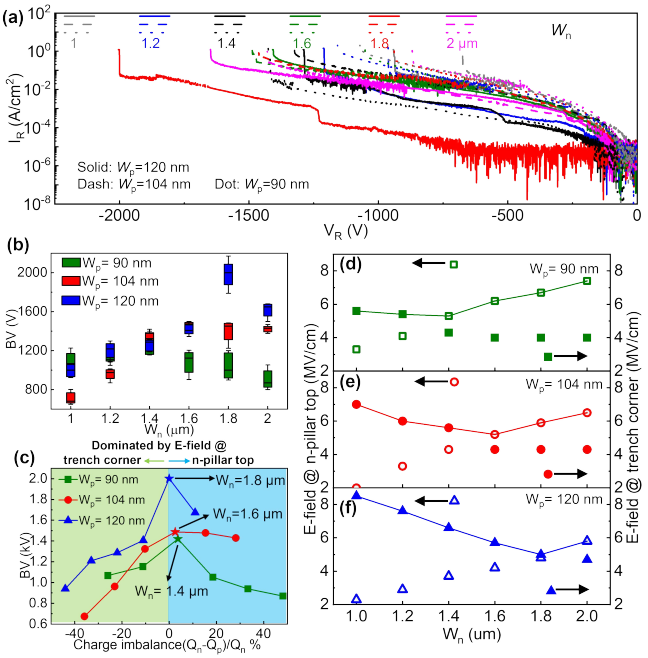


Fig. 12. (a) Reverse I–V characteristics of the Ga_2O_3/NiO hetero-SJ SBDs with w_n of 1–2 μm and various w_p (90/104/120 nm). (b) BV box plot as a function of w_n for various w_p. (c) BV as a function of charge imbalance percentage for the SJ SBDs with different w_p. Evolution of the simulated E-fields at the n-pillar top and at the trench corner for the SJ SBDs with (d) $w_p = 90$ nm, (e) $w_p = 104$ nm, and (f) $w_p = 120$ nm.

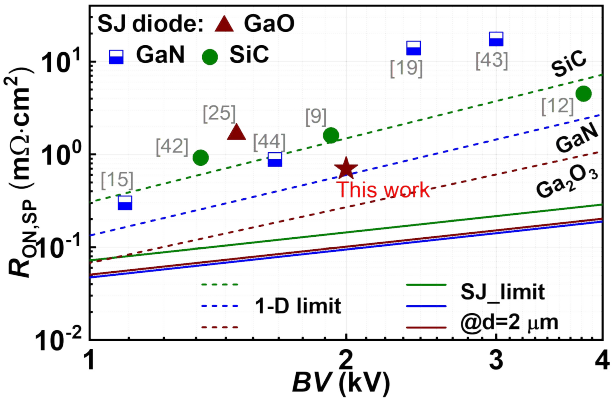


Fig. 13. Differential $R_{ON,SP}$ versus BV of our Ga_2O_3 SJ SBD and the state-of-the-art 1000–4000-V Ga_2O_3, SiC, and GaN SJ power diodes.

In addition, from the simulation, it can be seen that, for the device with $w_p = 120$ nm, w_n of 1.8 μm is near optimal as the two peak E-fields almost equalize; however, for the devices with $w_p = 90$ and 104 nm, an optimal w_n will exist between 1.2 and 1.4 μm and between 1.4 and 1.6 μm, respectively. This may be the reason why the experimental BV of devices with $w_p = 120$ nm and $w_n = 1.8$ μm is higher than that of devices with $w_p = 90$ nm and $w_n = 1.4$ μm and devices with $w_p = 104$ nm and $w_n = 1.6$ μm. Experimental devices with the denser w_n variations could possibly reach the true charge balance condition and achieve higher BV for devices with w_p of 90 and 104 nm. Furthermore, the observed fluctuations in BV across different w_p values may also be attributed to the nonuniform NiO thickness on the sidewalls in the fabricated device.

Finally, the simulation can provide a better understanding of the BV patterns for different w_p values, as shown in Fig. 12(c). In the p-excessive condition (i.e., insufficient w_n), simulation reveals that the device with $w_p = 90$ nm shows the smallest slope in the dependence of the peak E-field at trench corner on w_n, which can explain the slowest BV drop with the exacerbated p-charge imbalance (i.e., lower w_n) for this w_p. Considering the results in Fig. 11, this slower BV drop originates from the thinner NiO thickness at the trench bottom in the device with the smaller w_p.

V. Benchmark and Conclusion

Fig. 13 benchmarks the differential $R_{ON,SP}$ and BV tradeoff of our device and the state-of-the-art 1000–4000-V SJ power diodes reported in WBG and UWBG semiconductors [9], [12], [15], [19], [25], [42], [43], [44]. The Ga_2O_3/NiO hetero-SJ SBD shows one of the best performances in these SJ diodes, and its performance approaches the 1-D GaN limit. It also features a low V_{ON} of 1 V, which is only slightly higher than the lateral GaN diodes but lower than all other SJ diodes compared here. The performance limits of SiC-, GaN-, and Ga_2O_3-based SJs with a cell pitch of $\sim$2 μm are also plotted assuming a practical E_C of 2.8, 3.2, and 6 MV/cm, respectively. The experimental device performance is still far from the SJ limit, suggesting a large room for further improvement.

In summary, this article presents a systematic discussion on the performance limits, practical design guidelines, fabrication, and experimental characteristics of hetero-SJ devices. A Ga_2O_3/NiO hetero-SJ SBD is employed as a case study. A self-aligned process is developed for depositing p-type materials onto the n-pillar sidewalls and removing the p-type cap layers without the need for demanding lithography and dry etch. The BVs of the hetero-SJ devices are found to be determined by the p-type material at the trench bottom region and the n-pillar top region under the p-excessive and n-excessive conditions, respectively. The thickness inhomogeneity of p-type material at the sidewall and trench bottom could lead to an asymmetric pattern for the BV's dependence on the charge imbalance percentage. These results provide critical reference for developing SJ devices in diverse material systems.

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