An Adaptive Method for Mitigating Overvoltage Stress on Motor Windings Driven by SiC Inverters

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***Abstract*—High-performance switching devices such as SiC MOSFETs introduce high-frequency ringing and overvoltage transients at motor terminals, leading to uneven voltage distribution across windings. In SiC-driven motors, the first coil and initial turns experience significant overvoltage stress, increasing the risk of insulation degradation and interturn faults. This study proposes an analog circuit to mitigate overvoltage stress. The circuit detects high dv/dt in the first coil and adaptively inserts a ceramic capacitor via a GaN switch, forming a low-impedance path for high-frequency currents. This diverts part of the transient energy to the second coil, reducing stress on the first coil and promoting uniform voltage distribution. The GaN switch remains closed to sustain the high-frequency current path through the capacitor, adapting to different operating conditions and cable lengths. The circuit was prototyped and experimentally validated on a 2hp induction motor driven by a SiC inverter, demonstrating its effectiveness in mitigating overvoltage stress. This compact solution enhances the reliability of SiC-driven motor systems by addressing uneven high-frequency voltage distribution.**

***Index Terms*—High-frequency overvoltage, insulation aging, insulation reliability, motor drive, motor failure, reflected waves, SiC MOSFET, voltage distribution, voltage stress.**

I. Introduction

INSULATION of motor windings is fundamental to the reliability, longevity, and operational safety of electric propulsion systems. The powertrains in such systems must stand intense electrical, thermal, and mechanical stresses, driven by continuous operation under harsh environmental conditions and demanding speed profiles [1], [2]. The electrical stress on the winding insulation is particularly significant, as it directly affects the motor's ability to withstand overvoltage transients [3], [4]. Ensuring robust insulation prevents premature insulation breakdown, leading to interturn faults, phase-to-phase short circuits, and motor failure. As electric propulsion becomes a key enabler of sustainable transportation, addressing the challenges associated with winding insulation has become more critical than ever.

Adopting wide-bandgap (WBG) semiconductor devices, particularly silicon carbide (SiC) MOSFETs, has significantly enhanced power density and efficiency in electric drives. In addition to their fast-switching capability, their ability to operate at high temperatures makes them particularly advantageous for many applications [5]. However, these advancements have also introduced several challenges for motor windings driven by SiC inverters [6]. The ultra-fast switching characteristics of SiC MOSFETs generate voltage pulses with extremely short rise times (less than 50 ns) and high dv/dt rates. This high dv/dt induces high-frequency overvoltage transients at the motor side [7]. Such fast switching also leads to increased capacitive common-mode currents and reflected wave effects, as highlighted by [8], which further complicate electromagnetic interference (EMI) mitigation and insulation reliability in motor drive systems. When a cable is employed between the drive and motor, even a short-length cable, the wave reflection occurs due to the surge impedance mismatch between the cable and motor. As a result, overvoltage happens at the motor terminals [9], [10]. The overvoltage at the motor terminals is not evenly distributed across the stator windings. The first coil and initial turns are subjected to the highest high-frequency overvoltage stress because they are closest to the motor terminals, experiencing the full impact of the overvoltage transients. As the voltage propagates through the winding, subsequent coils experience less overvoltage stress because the major part of the voltage drops across the first coil. This uneven voltage distribution means the first coil suffers the most from the overvoltage stress. Over time, this nonuniform voltage stress accelerates insulation aging, causes interturn faults, and degrades motor reliability. Conventional winding insulation type, which were designed for sinusoidal voltages, are now subjected to high-frequency repetitive pulses that exceed their original design limits. Therefore, mitigating the adverse effects of ultrafast switching feature of SiC inverter on motor winding insulation has again become an area of research.

Received 4 February 2025; revised 27 April 2025; accepted 20 May 2025. This work was supported in part by the U.S. National Science Foundation under Grant 2135544 and in part by the Office of Naval Research under Grant N00014-22-1-2099. *(Corresponding author: Milad Sadoughi.)*

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Digital Object Identifier 10.1109/TIE.2025.3574543

Several solutions have been proposed in the literature to address motor overvoltage challenges. One commonly employed approach is the use of passive dv/dt filters to increase the rise time of the inverter's output PWM voltage pulses and limit the dv/dt rate. RLC filters, a specific type of dv/dt filter, are typically placed at the inverter terminals, effectively reducing the voltage overshoot at the motor terminals [11], [12], [13], [14], [15]. While effective, these filters have several drawbacks. They are often bulky, costly, and contribute to increased system losses. Additionally, the design of RLC filter parameters requires careful consideration of multiple factors, such as cable length, cable characteristic impedance, and motor impedance, making the design system-dependent. In addition to passive dv/dt filters, active dv/dt filtering techniques have been introduced in recent years [16], [17], [18], [19], [20], [21]. These methods adjust the dv/dt rate of the inverter output pulses by introducing a midlevel in the output voltage, resulting in a quasi-three-level (Q3L) voltage waveform. This approach is implemented by employing an external module connected in parallel with the main inverter module [16], [17], [18], [19]. While this technique cancels the reflected voltage and mitigates the motor terminals' overvoltage, it requires an external module and a complex switching algorithm for the inverter. These additional components increase the cost, size, and system complexity, limiting their practicality in compact systems. Another active-based solution is the open-end winding configuration, which uses two coordinated inverters to control voltage overshoots at the motor terminals [20]. This configuration requires an additional inverter and an extra power cable, effectively doubling the system size and complicating the system's modulation and control. Multilevel inverters have also been proposed as a solution to reduce dv/dt stress by using additional sub-modules [21]. However, multilevel inverter designs are less suitable for low-voltage ($< 1\text{kV}$) applications, where system simplicity, compactness, and cost-effectiveness are essential features. Most of these solutions increase the system's volume, weight, and control complexity, making them less suitable for weight-critical and space-constrained low-voltage applications. These also focus on suppressing overvoltage at the motor terminals.

The nonuniform voltage distribution within the motor windings persists even when terminal overvoltages are mitigated. This uneven distribution exposes the first few turns of the windings to significantly higher overvoltage stress, making them a critical point of concern. Integrating a capacitor across the first coil has been recently proposed [22], [23]. In [22], a GaN switch inserts the capacitor but for a predetermined fixed duration, limiting system adaptability since overvoltage stress varies with cable length. In [23], a fixed capacitor is connected across the initial coil, while a GaN switch adds an additional capacitor in parallel, tracking the high-frequency overvoltage transients. Although this approach mitigates first-coil overvoltage stress, it introduces certain drawbacks. Placing a fixed capacitor across the coil can create resonance issues, and in some cases, the fixed capacitor alone may sufficiently reduce the first coil voltage, rendering the additional capacitor connected via the GaN switch unnecessary. Moreover, the method proposed [23] requires a high bandwidth for GaN switch operation due to the oscillation frequency being in the megahertz (MHz) range. This high ultrafast bang-bang switching can introduce significant EMI issues within the circuit, posing additional challenges for the overall circuit reliability and electromagnetic compatibility (EMC).

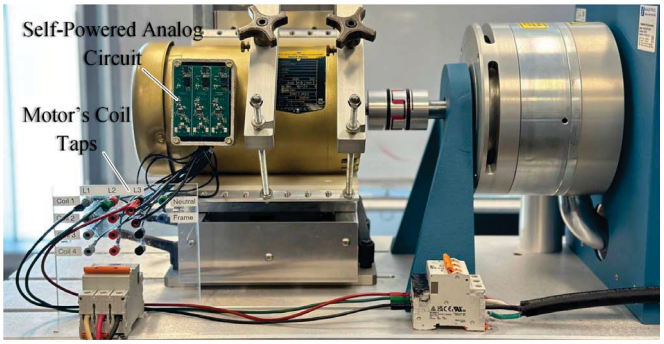

Fig. 1. Proposed self-powered analog circuitry for mitigating overvoltage stress on motor windings.

This article introduces a new method that overcomes these challenges by integrating a capacitor across the coil only when a high-frequency overvoltage transient is first detected. The proposed circuit monitors the duration of the overvoltage to keep the GaN switch closed adaptively. The GaN is connected in series with the capacitor. The circuit relies on simple analog components, a ceramic capacitor in the pF range, and a GaN switch, which offers superior thermal robustness compared with Si switches. As the circuit handles only high-frequency, low-magnitude current (mA-level RMS), the switching losses are minimal, and thermal stress on the device is negligible. This design effectively reduces cost and instability while ensuring reliable performance. This adaptive approach allows the capacitor to be connected only during transient events, enabling the system to operate in normal conditions without the risk of resonance. Unlike a hysteresis-based switching approach [23], our design uses transient detection logic that extends the gate pulse duration in response to overshoot and undershoot ringing events. This results in significantly fewer switching transitions compared with what might be required in a hysteresis-based switching approach. The analog control circuit operates independently of the inverter's modulation algorithm, providing a simple and robust implementation. Moreover, since the proposed circuit is not in the main path of the load current, it does not contribute to additional system losses. This design ensures effective mitigation of first-coil overvoltage without compromising system efficiency or control complexity and is scalable inside the motor terminal box, as shown in Fig. 1. Installation within the motor terminal box should involve coordination with the motor manufacturer or a qualified third-party partner, as adaptations may be necessary depending on the motor's internal winding configuration, voltage rating, and the maximum overvoltage observed at the first coil. While this limits direct applicability to off-the-shelf motors, such integration is feasible in custom or high-performance motor applications.

In addition to the introduction, this article is organized as follows: Section II discusses the effects of high dv/dt caused by inverters on voltage distribution within motor windings from various perspectives. Section III presents the proposed approach

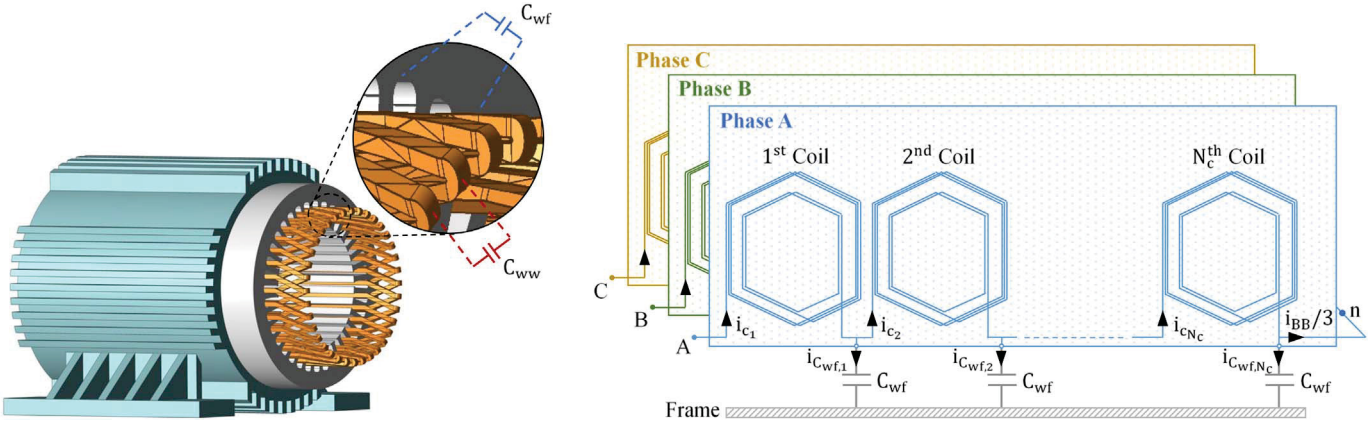

Fig. 2. Stator windings of an ac motor and the stray capacitances existing between the turns of windings, C_{ww}, and windings and stator core/frame, C_{wf}.

in detail and experimentally analyzes it, and Section IV provides experimental verifications of the proposed method in suppressing the coil high-frequency overvoltage transients. Finally, the article concludes with a summary of key findings in Section V.

II. Effect of High dv/dt on Voltage Distribution Inside Stator Windings

As noted earlier, the fast-switching SiC MOSFETs generate high dv/dt PWM pulses, causing high-frequency overvoltage transients in motor windings, with the first coil experiencing the highest voltage stress.

To explain the high-frequency overvoltage stress on the first coil, Fig. 2 illustrates the winding configuration of an induction motor. At high frequencies, the rotor circuit of the motor does not contribute to the electrical behavior, as no flux penetrates the rotor's magnetic circuit [24]. Each phase comprises N_c^{th} coils, with multiple turns per coil. The model includes stray capacitances: C_{ww}, representing the capacitances between turns within the windings, and C_{wf}, representing the capacitances between the windings and the motor frame. The high dv/dt of the voltage pulses can excite these stray capacitances, resulting in a leakage current flowing through them. The high-frequency leakage current passing through the stray capacitances existing between the windings and frame is expressed as

$$i_{C_{wf,k}}(t) = C_{wf}\frac{dv_k}{dt} \tag{1}$$

where v_k represents the voltage between k^{th} and $(k+1)^{\text{th}}$ coils and the frame. Consequently, the high-frequency current flowing through k^{th} coil is given by

$$i_{c,\text{HF}_k}(t) = \left(\sum_{i=k}^{N_c} i_{C_{wf,i}}(t)\right) + \frac{i_{BB}(t)}{3} \tag{2}$$

where i_{BB} represents the high-frequency leakage current (common-mode current) flowing through the ball bearing [24]. Assuming each coil has an identical impedance, denoted as Z_w, the high-frequency voltage across k^{th} coil can be calculated by

$$v_{c_k}(t) = Z_w i_{c,\text{HF}_k}(t). \tag{3}$$

For instance, considering an induction motor with four coils per phase, the high-frequency voltage across the first coil, v_{c1}, can be expressed as

$$v_{c1} = Z_w\left(i_{\text{cf1}} + i_{\text{cf2}} + i_{\text{cf3}} + i_{\text{cf4}} + \frac{i_{BB}}{3}\right). \tag{4}$$

It is, therefore, evident that the high-frequency voltage magnitude on the 4th coil of a motor with four coils becomes, $v_{c4} = Z_w(i_{\text{cf4}} + i_{BB}/3)$, which is much smaller than the first coil voltage in (4), i.e., $v_{c4} \ll v_{c1}$, emphasizing the uneven distribution of high-frequency voltages in the motor windings.

In addition to the fast-switching characteristics of SiC modules, the use of a cable between the drive and motor increases the risk of insulation breakdown in the first coil's windings and further exacerbates the nonuniform voltage distribution across the coils. This issue arises due to the surge impedance mismatch between the cable and motor windings, which causes wave reflections [6], [9], [24], [25], [26], [27]. The superposition of incident and reflected waves at the motor terminals leads to high-frequency overvoltage transients that can reach up to twice the dc-bus voltage, depending on the cable length and the rise time of the PWM voltage pulses. The oscillation frequency of the overvoltage can be estimated from

$$f_{\text{osc}} = \frac{1}{4l_{\text{cable}}\sqrt{L_{\text{cable}}C_{\text{cable}}}} \tag{5}$$

where l_{cable} is the cable length, and L_{cable} and C_{cable} are cable's inductance and capacitance per unit length, respectively. The penetration of these high-frequency overvoltages into the motor windings imposes excessive voltage stress on the first coil with significantly increasing the risk of insulation failure of the coil windings. Fig. 3 illustrates the impact of PWM voltage rise time and cable length on the peak voltage experienced by the first coil. The data was obtained experimentally using a 2hp induction motor driven by a SiC MOSFET-based inverter with a 350 V dc-bus. As shown in the figure, shorter rise times produce significantly higher peak voltages at the first coil, even with a short cable length. Conversely, for the same cable length, a longer rise time leads to a lower peak voltage at the initial coil.

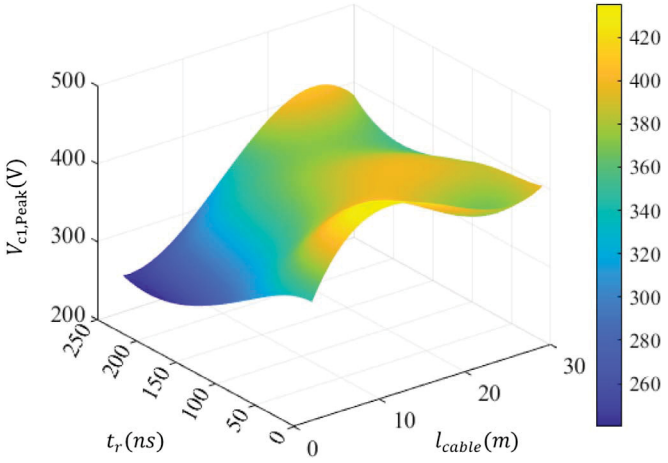

Fig. 3. Peak voltage observed across the initial coil of the stator windings with different cable lengths and switching rise times when dc-bus voltage is $V_{dc} = 350$ V.

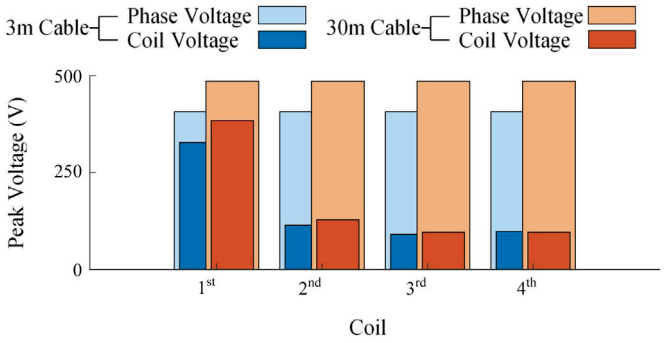

Fig. 4. Voltage distribution within the stator windings of one phase of a 2hp induction motor, along with the corresponding phase voltage, v_{an}, for two scenarios: the motor is fed by a SiC MOSFET-based inverter through 3 and 30 m cables with $V_{dc} = 350$ V, $t_r = 40$ ns.

To demonstrate how the first coil experiences the most overvoltage stress, two scenarios were examined and presented in Fig. 4 under the following condition: $V_{dc} = 350$ V and about $t_r = 40$ ns, where the peak voltages are provided, experienced by each coil in one phase. The figure shows that, regardless of the cable length, the first coil experiences the highest overvoltage stress, which is considerably larger than that of the subsequent coils' voltages. While the remaining coils experience relatively small and uniform voltages, the first coil is subjected to the dominant portion of the phase voltage transient. This highlights the nonuniform voltage distribution caused by fast-switching devices in motor drives, increasing the risk of insulation breakdown and interturn faults. Consequently, even in cases where a short cable is used or overvoltage at the motor terminals is not notable, the first few turns of windings remain exposed to high-frequency overvoltage transients stress due to the high dv/dt. This nonuniform stress distribution poses a significant challenge for motor insulation design and must be addressed to prevent catastrophic motor failures.

In Fig. 4, it is important to note that while the sum of the voltages across all four coils equals the phase voltage at any given instant, the peak voltages of Coils 1 through 4 do not occur simultaneously. Due to propagation delay, each subsequent coil reaches its peak after the previous one. This means that when Coil 1 experiences its peak overvoltage, the other coils have not yet reached theirs. Accordingly, Fig. 4 presents the peak values occurring at different times, only to highlight the importance of mitigating overvoltage stress on the first coil. The following section discusses the proposed approach to mitigate this issue and enhance the reliability of motors driven by SiC inverters.

III. First Coil Overvoltage Suppression via Adaptive Pulse-Width Method

For many applications, e.g., powertrains in propulsion systems, SiC inverters provide high efficiency, but as mentioned in the previous section, overvoltage stress on the first coil can degrade the motor lifetime. This section presents a detailed explanation of the proposed solution to address this issue effectively.

A. Impedance Adjustment for Voltage Stress Mitigation

Fig. 5 illustrates the observed voltage waveforms at inverter output (line-to-line), motor terminals (line-to-line), the motor phase, and across the first coil of the corresponding phase. These measurements were taken under operating conditions of a 350 V dc-bus, $t_r = 40$ ns, and $l_{cable} = 30$ m. As shown, the measured motor terminal voltage exhibits high-frequency overvoltage transients, primarily caused by the short rise time of the PWM pulses and the voltage reflections. These overvoltage transients propagate into the motor, superimposing high-frequency transients onto the phase voltage waveform. While the offset of the phase voltage is inherently present due to the nature of the PWM modulation, the high-frequency transients are directly induced by the overvoltage transients at the motor terminals, see Fig. 5. The phase voltage offset is evenly distributed among the coils. However, the high-frequency transient components are predominantly dropped across the first coil. Therefore, the voltage across the first coil can be modeled as a second-order underdamped system expressed as

$$v_{c1}(t) = V_{os} + v_{HF}(t) \tag{6}$$

where V_{os} and $v_{HF}(t)$ are the dc and transient high-frequency components of the coil voltage, respectively. As shown in Fig. 5, V_{os} can take values of 0, $(V_{dc}/3)/N_c$, $(2V_{dc}/3)/N_c$, $(-V_{dc}/3)/N_c$, and $(-2V_{dc}/3)/N_c$. The high-frequency components, $v_{HF}(t)$, can be expressed as

$$v_{HF}(t) = Ae^{-\xi\omega_n(t-t_i)}\cos(\omega_d(t-t_i)+\varphi) \tag{7}$$

where A is the initial amplitude of the oscillation, given by $A = (1/\sqrt{1-\xi^2})e^{-\xi\omega_n t}$, ξ is the damping ratio, ω_n is the neutral frequency, ω_d is the damped neutral frequency obtained by $\omega_d = 2\pi f_{osc} = \omega_n\sqrt{1-\xi^2}$, φ represents phase shift, and t_i is the time at which the transition occurs.

To suppress the overvoltage stress on the first coil, the impedance of the coil can be adjusted to redirect the high-frequency components of the current toward the second coil by providing a parallel branch. This approach aims to shift only the high-frequency components of the current while maintaining the desired current path for low-frequency components. To achieve this, the impedance of the first coil must be reduced when

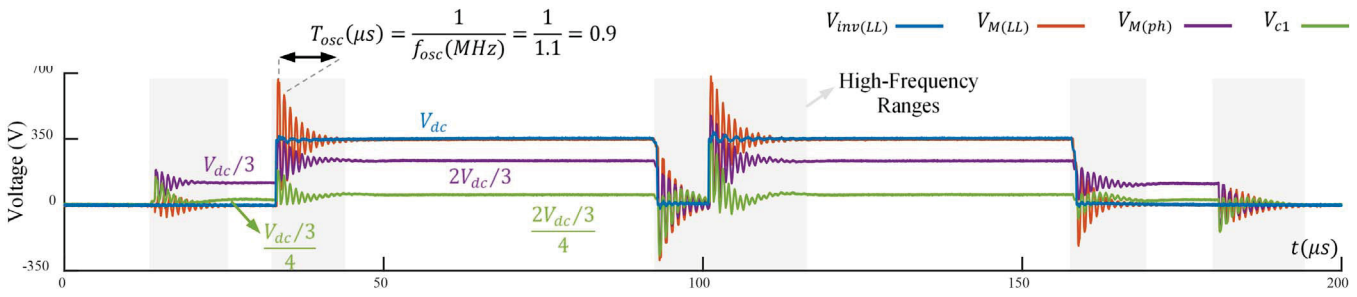

Fig. 5. Measured line-to-line voltages across the inverter output and the motor terminals along with the phase voltage of the motor and the first coil voltage within the corresponding phase when the motor is fed by a SiC MOSFET-based inverter through a 30 m cable with $V_{dc} = 350$ V, $t_r = 40$ ns.

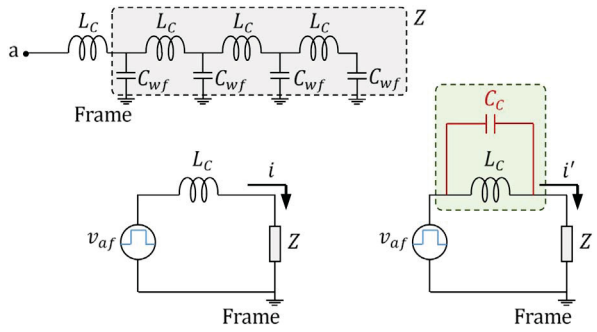

Fig. 6. Simplified high-frequency model of the first coil of phase A in a Y-connected motor, showing the phase-to-frame voltage, v_{af}, coil inductance, L_c, and remaining windings and stray capacitances, Z, for normal condition (left) and coil paralleled with a capacitor (right).

overvoltage transients occur. This can be accomplished by connecting a capacitor in parallel with the first coil. The capacitor provides a low-impedance path for high-frequency currents, mitigating the overvoltage stress on the first coil and resulting in a more uniform voltage distribution among the coils. Notice, the overall leakage currents remain largely unaffected since the phase-to-frame voltage remains unchanged.

Fig. 6 shows the simplified high-frequency model of one phase of the stator windings with respect to the motor frame, including the first coil inductance, L_c, and rest of the coils and stray capacitances lumped as Z. Therefore, the first coil voltage can be written as

$$V_{c1}(s) = Z_c(s).\, I_{\mathrm{HF}}(s) = L_c s.\, I_{\mathrm{HF}}(s) \tag{8}$$

where I_{HF} is the high-frequency current passing through the motor frame. By implementing a capacitor across the first coil, as shown in Fig. 6, the coil impedance is changed to

$$Z_c'(s) = \frac{L_c s}{1 + L_c C_s s^2}. \tag{9}$$

Therefore, the coil voltage is given by

$$V_{c1}'(s) = \frac{L_c s}{1 + L_c C_s s^2}.I_{\mathrm{HF}}'(s) \tag{10}$$

which indicates that at high frequencies $(s \to \infty)$, $Z_c'(s) \to 1/C_s s$, and therefore, the voltage across the coil can be suppressed notably. From (10), one can see that keeping the capacitor in the circuit can have resonance at $1/\sqrt{L_c C_s}$, and may require additional damping elements or control strategies to limit the oscillation. The proposed solution is to insert the capacitor only when needed, limiting its interaction time with the coil. As a result, instant oscillations may occur during transients, but because the capacitor is connected only during high dv/dt events, the duration is too short to sustain resonance.

To demonstrate the impact of paralleling capacitors of different sizes on the coil's impedance of a 2hp induction motor, the impedances of the coil, individual capacitors, and the coil paralleled with each capacitor were measured using an LCR meter, as provided in Fig. 7. The figure indicates that increasing the capacitor size significantly reduces the coil impedance. This observation suggests that reducing the coil impedance can effectively mitigate the high-frequency overvoltage stress on the coil. However, it is also anticipated that this approach could substantially increase the voltage across the second coil due to the rising of i'_{HF}. To prevent excessive voltage stress on the second coil, the capacitor size must be carefully selected. Capacitors with values in the range of hundreds of picofarads, e.g., 470 pF, provide an optimal balance in this case. Additionally, for larger capacitor sizes, the resonance point shifts closer to the overvoltage ringing frequency of the coil. If the resonance frequency aligns with the coil's overvoltage ringing frequency, it can lead to a significant rise in the second coil's voltage. This provides insight into determining an upper bound for selecting the capacitor value. Therefore, the suitable range for the capacitor size is recommended to be between 470 and 1000 pF to achieve an effective reduction in first-coil voltage stress while minimizing the impact on the second coil. Selecting an optimal capacitor size within this range can also promote a more uniform voltage distribution across the motor windings, enhancing insulation reliability and system robustness.

B. Adaptive Capacitor Insertion for High-Frequency Overvoltage Mitigation and Stress Unification

Placing a permanent capacitor across the first coil can lead to resonance, potentially causing increased overvoltage and damage to the windings. To address this challenge, the capacitor is inserted only when high-frequency overvoltage transients are detected. This work examines a solution that uses a GaN switch in series with the capacitor. When high-frequency overvoltage transients are detected, the GaN switch closes, connecting the capacitor in parallel with the first coil. The GaN switch is chosen for two key reasons: it's extremely short rise time and its ability to operate at high switching frequencies. Since overvoltage

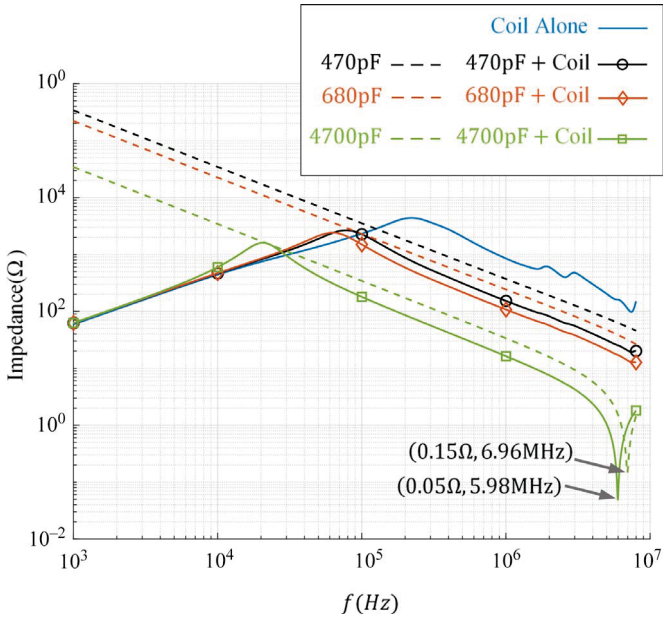

Fig. 7. Measured impedance of a single coil from one phase of a 2hp induction motor, impedances of individual capacitors of different sizes, and impedance of the coil connecting in parallel with each capacitor across a wide frequency range.

spikes ramp up within tens of nanoseconds, a rapid response is critical to suppress them effectively. With a rise time of less than 20 ns, the GaN switch ensures the capacitor is connected quickly enough to suppress the overvoltage effectively. Additionally, a fast control circuit is essential to detect voltage stress and generate the required switching pulses for the GaN within a few nanoseconds, ensuring quick and reliable protection.

Fig. 8 depicts the analog control circuit for the proposed solution, consisting of multiple components to detect the high-frequency overvoltage transients and generate the adaptively adjusted pulse duration for the GaN. To focus on the overvoltage transients, two capacitors with the same size, C_F, are used to remove voltage waveform offsets. These capacitors act as high-pass filters, blocking the dc components, V_{os}, and allowing the high-frequency components, $v_{HF}(t)$, to pass. While a band-pass filter may improve noise immunity for long cables, short cables require a high-frequency cutoff around 10MHz. This wide frequency range reduces its effectiveness and increases complexity, offering no clear advantage over the simpler high-pass design. The transfer function of the high-pass filter in the frequency-domain can be expressed by

$$H(f) = \frac{1}{1 + \frac{2}{R_{Load} C_F (2\pi f)}} \tag{11}$$

where R_{Load} is the equivalent resistance of the components used in this circuit. This results in the following behavior at the filter output

$$\begin{cases} v_{out}(t) \approx 0 & (f \to 0) \\ v_{out}(t) \approx v_{HF}(t) & (f \gg 1/2\pi R_{Load} C_F). \end{cases} \tag{12}$$

The voltage is then stepped down via a voltage divider (resistors R_{D1} and R_{D2}) to a measurable range, i.e., $v_o(t) = (R_{D2}/R_{D1} + R_{D2}) v_{HF}(t)$. After the divider, the waveform contains both positive and negative high-frequency spikes within a low voltage range. A comparator is employed to detect These spikes by setting upper and lower thresholds. To allow the detection of negative spikes, the waveform is shifted upward through a differential amplifier by giving an offset, V_{OCM}, acting as a level shifter. Therefore, the output signal of the differential amplifier can be equal to $v_{diff}(t) = v_o(t) + V_{OCM}$. When the voltage exceeds the upper threshold (U_{UL}) or drops below the lower threshold (U_{LL}), the comparator transitions from high to low. Conversely, when the voltage remains between the thresholds, the comparator output stays high. This behavior is described as

$$\begin{cases} v_{comp}(t) = \text{High} & U_{UL} < v_{diff}(t) < U_{LL} \\ v_{comp}(t) = \text{Low} & v_{diff}(t) < U_{LL} \text{ or } v_{diff}(t) > U_{UL} \end{cases} \tag{13}$$

where $U_{UL} = 1.02 V_{OCM}$ and $U_{LL} = 0.98 V_{OCM}$. The comparator's transition from high to low mode triggers the pulse generator to produce a preset pulse with a duration of T_{pulse}, determined by R_{SET}. The pulse width can be programmed as $T_{pulse} = (1\mu s/50\ k\Omega) R_{SET}$, where R_{SET} can range from 50 to 800 kΩ, allowing flexible control of the pulse duration. Suppose, during the pulse duration ($0 < t < T_{pulse}$), the comparator output steps back to high and subsequently returns to low at time t_r, the pulse generator retriggers. The new pulse begins from t_r, and the total pulse width, t_{OUT}, is extended, which can be expressed as

$$t_{OUT} = T_{pulse} + \sum_{r=1}^{m} (t_r - t_{r-1}) \tag{14}$$

where t_r is time of the rth retrigger, t_{r-1} is time of previous re-trigger, and m is the number of re-triggers. This equation accounts for incremental extensions in pulse width caused by consecutive re-triggers, where each retrigger adds the time elapsed since the previous one. The initial pulse is triggered at $t_0 = 0$ with a duration of T_{pulse}. At t_1, the comparator retriggers, extending the pulse by $t_1 - t_0$. Subsequent retriggers at $t_2, t_3, \ldots, t_m$ further extend the pulse by $t_r - t_{r-1}$, ensuring the capacitor remains engaged as long as transient oscillations persist. This retriggerable behavior enables the pulse generator to adapt dynamically to varying durations and amplitudes of overvoltage transients, ensuring continuous protection and effective mitigation of voltage stress across varying cable lengths and system conditions. Overall, to set the initial pulse duration (i.e., minimum pulse width), a monostable pulse generator is configured using a timing resistor (R_{SET}). If the oscillation takes longer to damp or a new dv/dt event occurs, the pulse duration (t_{out}) is automatically extended until the overshoot and undershoot fall below a predetermined threshold.

C. Design and Implementation of the Proposed Analog Circuit

Fig. 9 illustrates the printed circuit board (PCB) of the proposed analog circuit, designed in Altium Designer, with compact dimensions of 6.4 cm × 8 cm to allow easy integration into the motor terminal box. The feedback path and power supplies for the analog circuit must be isolated, particularly as the coil voltage is used to power the circuit elements. A Transphorm TP65H480G4JSG-TR GaN switch is employed in the circuit.

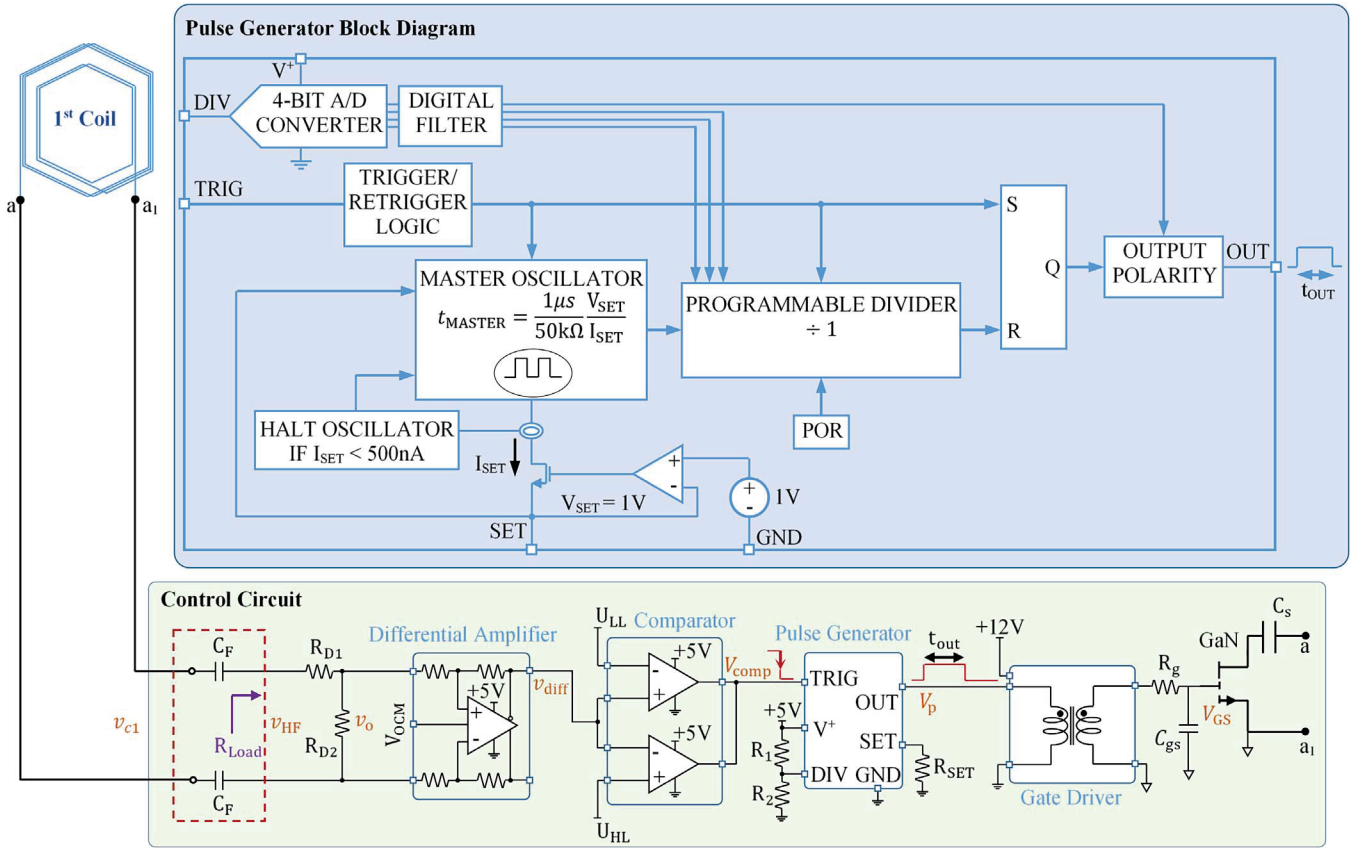

Fig. 8. Schematic of the proposed control circuit for sensing the coil voltage in one phase (phase A), detecting the voltage spikes, and producing the required pulses for the GaN switch along with the pulse generator internal block diagram.

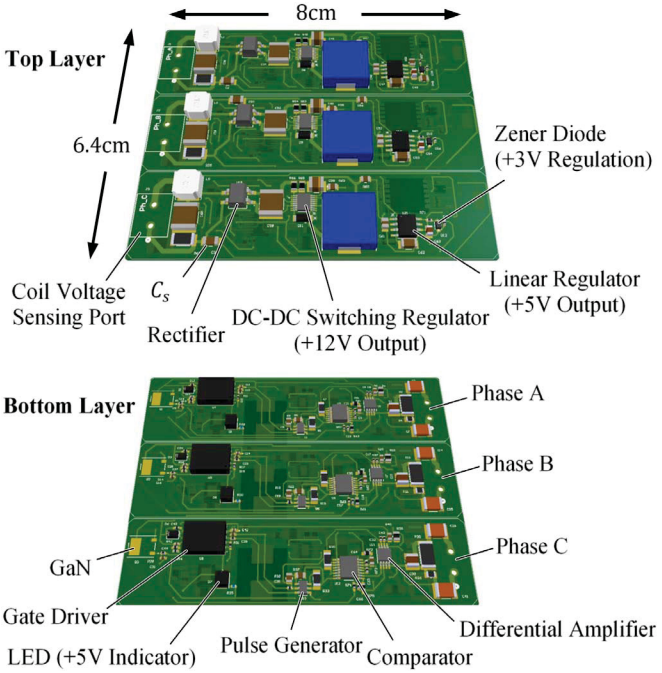

Fig. 9. Proposed circuit: top layer is used for providing the required power supply for the control circuit in the bottom layer and bottom layer used for detecting and suppressing the overvoltage observed across the first coil.

In the presented self-powered analog circuit, where no external supply is used, all required voltage levels are derived from the first coil voltage. To provide gate signal isolation, a pulse-transformer-based gate driver (AHV85110KNHTR) is employed. Unlike dual-side powered gate drivers, which require an isolated dc–dc converter to supply the secondary side, the pulse-transformer transfers gate signals without requiring a secondary-side supply. This eliminates the need for an isolated dc–dc converter in the loop, thereby reducing both circuit complexity and board size, making it suited for the self-powered design. Unlike direct-drive pulse transformers, the AHV85110 modulates the gate signal across the isolation barrier using a balanced, ac-coupled method. The internal "auto-refresh/demagnetization" block ensures the transformer core flux is reset between pulses, preventing saturation even during extended gate-on periods and maintaining undistorted, reliable output signals.

To protect the control system from leakage current originating from the GaN switch's drain, the gate resistor (R_g) is selected at its higher end to ensure circuit's noise immunity, with a small gate-to-source capacitance (C_{gs}) to filter noise at the gate pin while ensuring that the GaN switch turns off before the coil experiences overvoltage stress. The low R_gC_{gs} time constant and relatively high R_g are special design choices that ensure circuit's noise immunity particularly for short-cable length scenarios when the coil's ringing frequency is above 1 MHz.

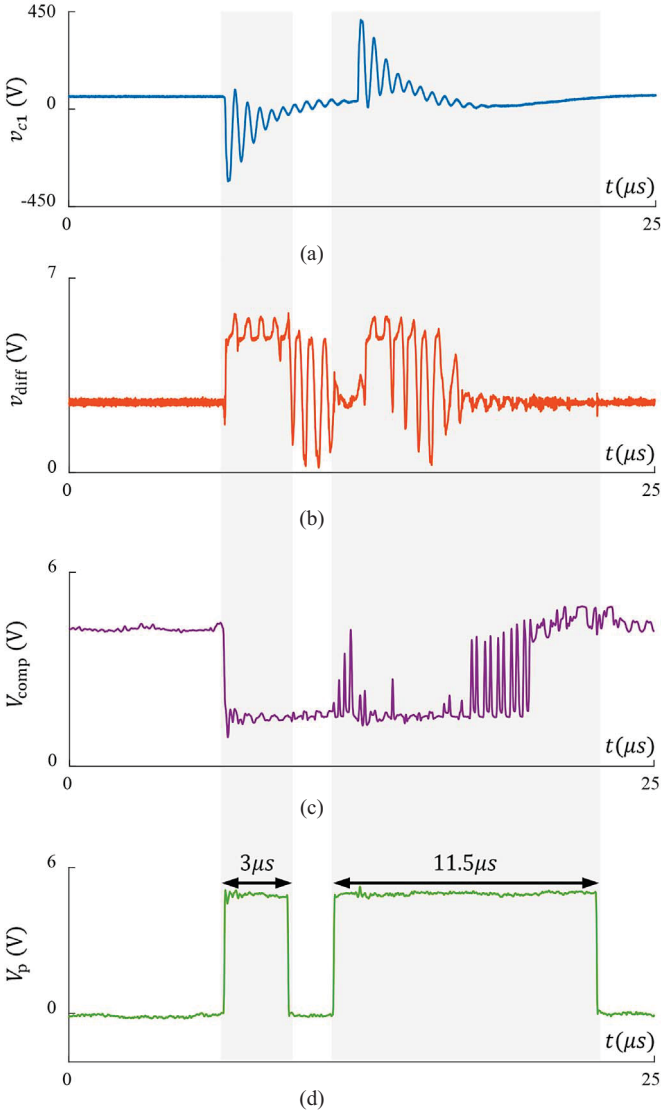

Fig. 10. Proposed circuit detecting high-frequency voltage spikes in the first coil and generating switching pulses for the GaN switch in a motor drive system (2hp motor, 15 m cable, SiC MOSFET-based inverter, $V_{dc} = 350$ V, and $t_r = 40$ ns). (a) First coil voltage waveform. (b) Differential amplifier output. (c) Comparator output. (d) Pulse generator output.

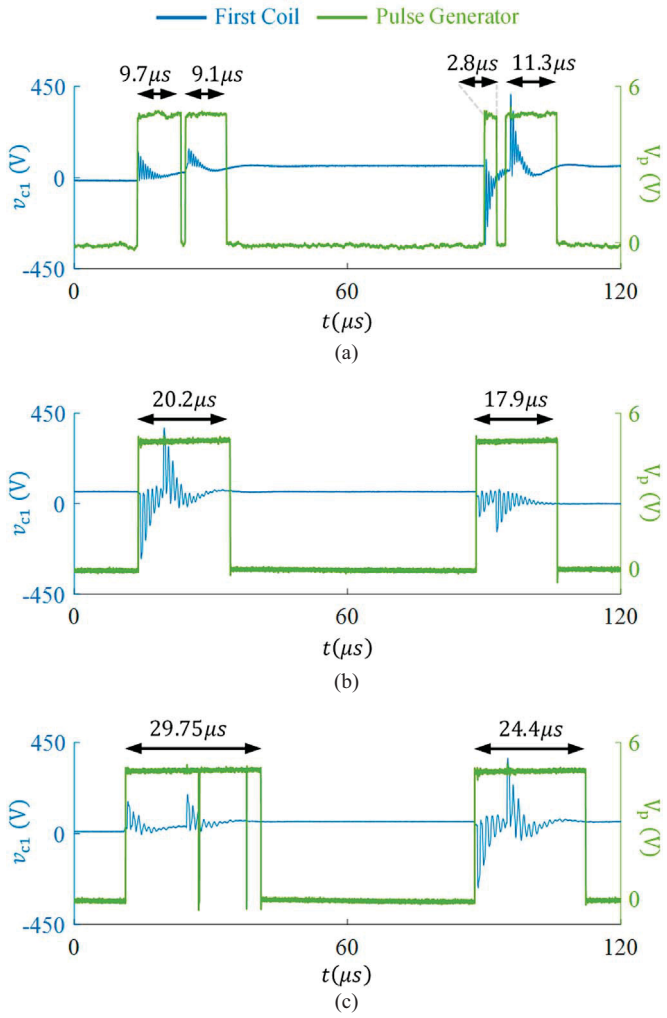

Fig. 11. Measured first coil voltage and the circuit functionality in detecting the voltage spikes and generating the pulses with the desired width for the GaN switch in a motor drive system (2hp motor, 15, 30, and 40 m cables, SiC MOSFET-based inverter, $V_{dc} = 350$ V, and $t_r = 40$ ns). (a) 15 m cable. (b) 30 m cable. (c) 40 m cable.

The series capacitor, C_s, is in the pF range, thus, the GaN switch conducts only high-frequency current, with RMS values in the *mA* range and peak currents of a few amperes. This makes existing GaN devices suitable for low-voltage applications. For coil voltages above 400 V, series-connected GaN or SiC switches are recommended. The selection of the GaN switch and capacitor value, along with the fact that the analog circuit is powered by the coil voltage, means the board design must be tailored to the motor's design, and should be carried out by or in collaboration with the motor manufacturer.

The design offers effective interference immunity, achieved through extensive effort and multiple PCB revisions. An isolated gate driver (pulse transformer) provides complete separation between the analog control section and the high-frequency coil side, where the GaN switch and series capacitor are located. This isolation helps prevent conducted EMI and ground loop issues. The PCB layout was also carefully optimized to minimize parasitic inductance, stray capacitance, and loop areas, reducing radiated EMI and enhancing overall EMC.

In the circuit, 100 pF and 1 nF ceramic capacitors are compatible due to their excellent high-frequency performance, low ESR, and compact size. Specifically, COG (NP0) capacitor types are preferred for their superior stability, maintaining consistent capacitance across temperature and voltage variations.

D. Proposed Circuit's Functionality in Detection Coil Overvoltage and Generating GaN's Switching Pulses

To evaluate the circuit's functionality in detecting coil overvoltage and adaptively generating the switching signals for different conditions, such as cable lengths, different experimental tests were conducted. The dc-bus voltage was 350 V and PWM voltage pulses' rise time was about 40 ns.

As shown in Fig. 8, the overvoltage detection circuit, consisting of a high-pass filter, voltage divider, differential amplifier, and comparator, forms the detection path with a total response

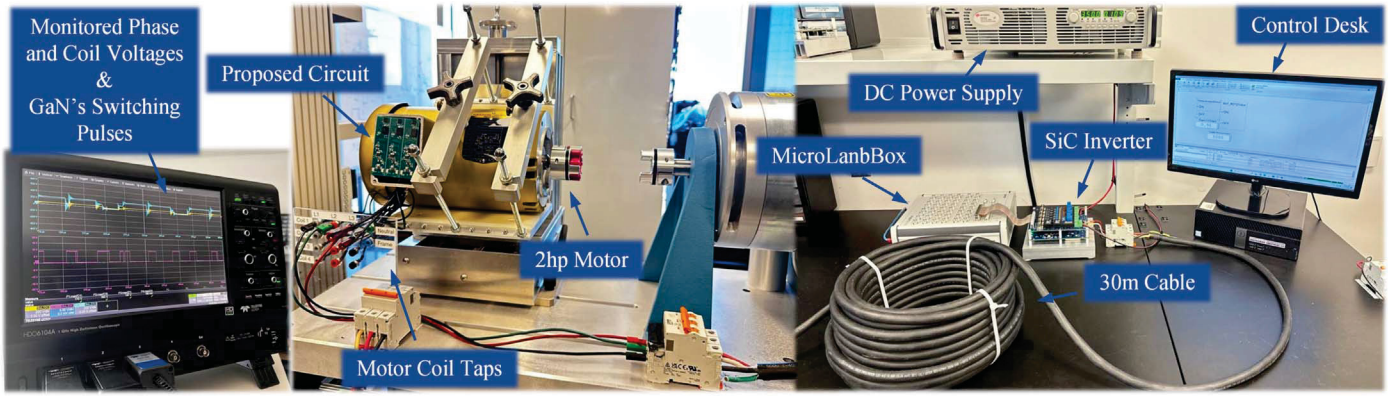

Fig. 12. Hardware setup used for experimental analysis.

time of approximately 18 ns. This response time is appropriate because the ringing frequency for a 15 m cable is around 2 MHz, meaning the first peak occurs within approximately 125 ns. Therefore, the 18 ns delay is sufficiently short to detect the fast dv/dt events across the first coil, ensuring accurate and timely triggering of the protection mechanism.

For a 15 m cable, the circuit's performance is illustrated in Fig. 10. Fig. 10(a) shows the measured first coil voltage, where spikes reach up to 380 V. To process these spikes, the voltage offset of the first coil is removed, and the spike amplitude is reduced using a voltage divider. The differential amplifier, acting as a level shifter, then shifts the waveform around 2.5 V, i.e., V_{OCM}, enabling the comparator to detect both positive and negative voltage spikes, as shown in Fig. 10(b). The comparator output, shown in Fig. 10(c), transitions from high to low levels whenever the first coil voltage exceeds the upper or lower thresholds. This output signal triggers the pulse generator to generate the required pulses, as shown in Fig. 10(d). The default pulse width is set to 3 μs using $R_{\mathrm{SET}} = 150$ KΩ. Fig. 10(d) indicates that the pulse width remains at the preset value when the pulse generator is not retriggered. However, when the pulse generator receives consecutive input signals, the pulse width is adaptively prolonged. The results in Fig. 10(d) demonstrate that the circuit can accurately and rapidly detect coil voltage spikes and adaptively produce pulses for the gate driver, with the pulse width varying according to the duration of the overvoltage transient.

To further evaluate the adaptability of the proposed circuit, two different cable lengths, 30 and 40 m, were tested, as shown in Fig. 11. The results provided in Fig. 11(b) and 11(c) indicate that as the cable length increases, the transient ringing frequency across the coil decreases, resulting in a longer duration of high-frequency overvoltage. The circuit adaptively adjusts the switching pulse durations to match the extended duration of the voltage spikes, demonstrating its capability to accommodate changes in cable length between the motor and the inverter.

IV. Experimental Analysis and Verifications

To evaluate the efficacy of the analog circuit in Fig. 8, experiments were conducted on a 2hp induction motor driven by a SiC inverter with 30 and 40 m cables. The experimental hardware setup is shown in Fig. 12, with detailed specifications of the setup and motor presented in Tables I and II, respectively. An open-loop sinusoidal pulse-width modulation (SPWM) algorithm implemented via a MicroLabBox was employed to control the inverter, driving the motor under no-load conditions. The motor was rewound to provide access to the coil taps, enabling voltage distribution monitoring within the stator windings and addressing overvoltage in the first coil. All experiments were conducted with a dc-bus voltage of 350 V and designed for a PWM switching frequency of 5–80 kHz. Voltage data were

TABLE I
Experimental Setup

Parameters	Detail and Values
SiC MOSFET inverter Gate driver board	CGD15FB45P1
SiC-MOSFET	CCS020M12CM2
PWM carrier frequency	5 kHz
Fundamental frequency	60 Hz
V_{dc}	350 V
t_r	40 ns
4/C 10 AWG cable length	15 m, 30 m, and 40 m

TABLE II
Under-Study Motor Parameters

Parameters	Detail and Values
Catalog number	VEM31157
Power	2hp
Voltage	230/460
Current	5.6/2.8
Speed	1755
Frequency	60
Number of coils per phase (high voltage)	4
Number of coils per phase (low voltage)	2
Number of turns per coil	85
Number of slots	36
Construction	Y-connected

collected using a LeCroy HDO6104A oscilloscope, equipped with HVD3106A and ADP300 differential voltage probes, featuring bandwidths of 120 and 20 MHz, respectively. The waveforms were processed and plotted using MATLAB software, and the results are presented in this section.

To evaluate the proposed overvoltage suppression method for the first coil, a transformer-based gate driver and a GaN switch were integrated into the circuit to connect a 680 pF ceramic capacitor across the coil. The pulse generator output signals, shown in Fig. 11, were sent to a gate driver, which provided isolated gate-to-source signals for driving the GaN switch. The results, presented in Fig. 13, demonstrate that, compared with the normal condition, the first coil's high-frequency overvoltage spikes were effectively mitigated from 334 V and 338 V to 160 V and and 163 V for 40 and 30 m cable lengths, respectively. This reduction is achieved because the GaN switch is triggered appropriately upon spike detection.

Additionally, the pulse durations were adaptively adjusted based on the duration of the overvoltage spikes. As the cable length increases, the oscillation frequency of the overvoltage transient decreases, resulting in a longer oscillation time. Consequently, for longer cables, the required pulse width for the GaN must be longer than that for shorter cable lengths. This adaptive pulse width generation is shown in Fig. 13 for two different cable lengths, confirming the proposed circuit's effectiveness under varying cable conditions.

Fig. 14 illustrates the voltage distribution across the motor windings by measuring peak overvoltage transients. The proposed circuit effectively suppresses voltage spikes in the first coil from 386 to 180 V, while an increase occurs in the second coil, but leading to a more uniform voltage distribution. For this design, a smaller C_s value could further balance the overvoltage between the first and second coils. To evaluate this effect, a 470 pF capacitor was also tested, and the results are shown in Fig. 15. These results indicate that selecting a smaller capacitor can further improve and balance the voltage distribution among the motor coils.

Fig. 16 shows the measured voltage waveform across the 470 pF capacitor during an overvoltage transient. The capacitor used in this experiment is a Johanson Dielectrics VPDD501G471J1GV001E (C0G, 470 pF, 500 V rated), specifically selected for its high dv/dt tolerance, excellent high-frequency stability, and low ESR characteristics. During operation, the measured voltage transient across the capacitor rose from 40 V to a peak of 174 V within 93 ns, resulting in a peak current of approximately 0.68 A, i.e., $i_{Cs,\text{Peak}} = 470\ \text{pF} \times (134/93\ \text{ns}) = 0.68\ \text{A}$. The capacitor's C0G dielectric ensures minimal capacitance variation under high voltage and temperature conditions, maintaining reliable transient suppression without risk of dielectric breakdown.

The capacitor value is selected based on experimental LCR measurements and observed voltage distribution, with 470–680 pF found effective for the 2hp case study. Power consumption remains below 1 W, minimizing thermal stress. Unlike traditional impedance-matching RC circuits that operate continuously, the proposed circuit engages only during transients, reducing energy

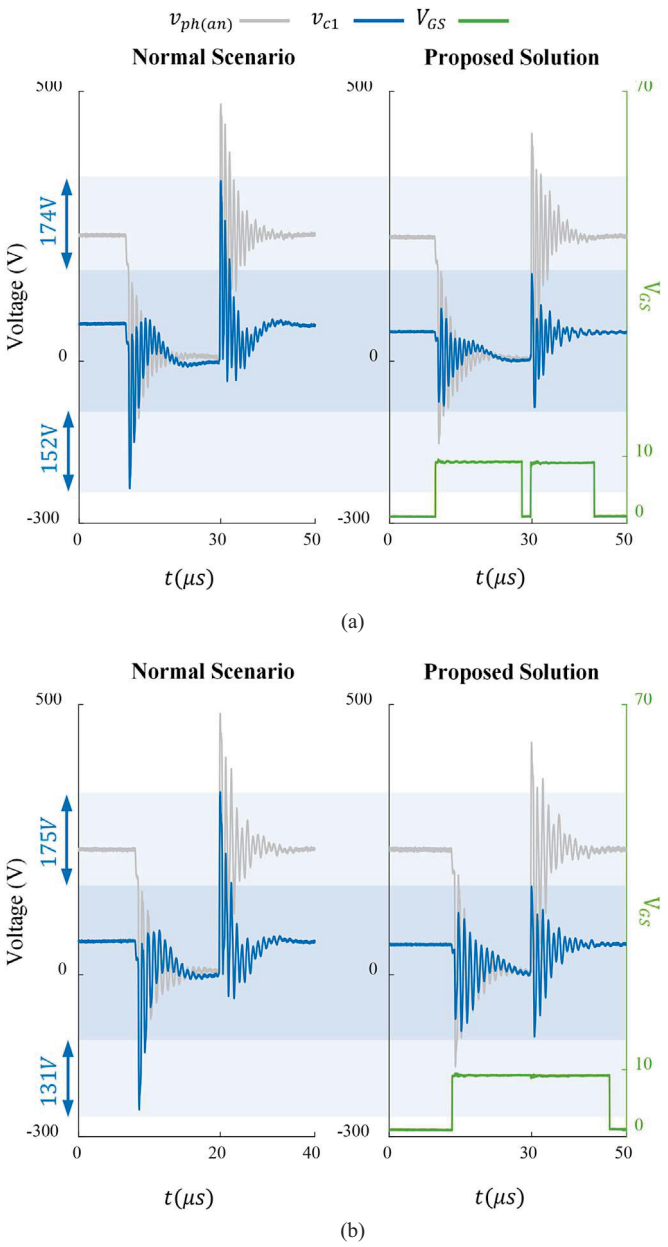

Fig. 13. Experimentally measured phase and the first coil voltage waveforms of a 2hp induction motor fed by a SiC MOSFET-based inverter through different cable lengths with $V_{dc} = 350$, $t_r = 40$ ns, and $f_S = 5$ KHz for two different cases using two different cable lengths: normal scenario (left) and using proposed approach (right). (a) 30 m cable. (b) 40 m cable.

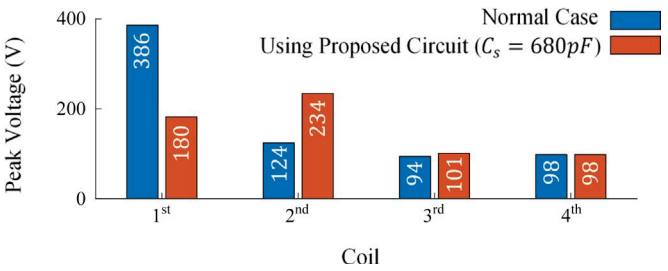

Fig. 14. Measured peak voltages across the coils of the windings of a 2hp motor fed by a SiC MOSFET-based inverter through a 30 m cable with $V_{dc} = 350$ V and $t_r = 40$ ns for two different cases: normal case and using proposed circuit ($C_s = 680$ pF).

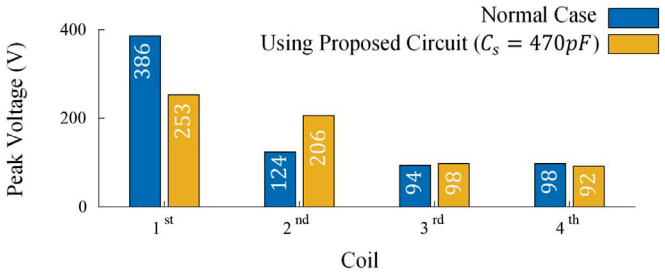

Fig. 15. Measured peak voltages across the coils of the windings of a 2hp motor fed by a SiC MOSFET-based inverter through a 30 m cable with $V_{dc} = 350V$ and $t_r = 40$ ns for two different cases: normal case and using proposed circuit ($C_s = 470pF$).

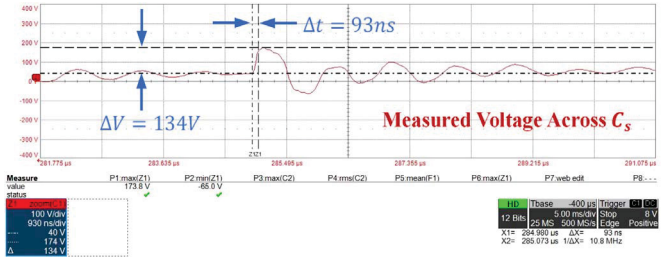

Fig. 16. Measured voltage across the 470 pF capacitor (C_s) during the overvoltage transient.

loss and eliminating the need for precise tuning. The main con is that the board design must be developed by, or in collaboration with, the motor manufacturer.

V. Conclusion

This article has introduced an adaptive pulse-width method to mitigate high-frequency overvoltage transients observed across the first few turns and the first coil within the motor windings driven by a SiC MOSFET-based drive. The proposed solution adjusts the coil impedance by integrating a small capacitor across the coil. This is achieved by detecting high-frequency overvoltage transients and rapidly activating a GaN transistor connected in series with the capacitor. The adaptability of the proposed approach allows for effective mitigation of first-coil overvoltage under varying cable lengths. As the cable length increases, the duration of high-frequency overvoltage transients extends, necessitating wider pulse widths to drive the GaN device accordingly. Experimental analysis has confirmed the efficacy of the proposed approach, demonstrating significant suppression of overvoltage stress on the first coil and promoting a more uniform voltage distribution within the stator windings. This adaptive strategy enhances the reliability and insulation integrity of motor windings, especially in propulsion systems utilizing SiC MOSFET-based drives.

Reference

[1] R. Leuzzi, V. G. Monopoli, L. Rovere, F. Cupertino, and P. Zanchetta, "Analysis and detection of electrical aging effects on high-speed motor insulation," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 6018–6025, Nov./Dec. 2019.

[2] M. Kaufhold, H. Aninger, M. Berth, J. Speck, and M. Eberhardt, "Electrical stress and failure mechanism of the winding insulation in PWM-inverter-fed low-voltage induction motors," *IEEE Trans. Ind. Electron.*, vol. 47, no. 2, pp. 396–402, Apr. 2000.

[3] A. K. Khiz and S. H. Jayaram, "SiC-MOSFET-based high voltage pulse generator for testing motor insulation used in EVs," *IEEE Trans. Transport. Electrific.*, vol. 11, no. 1, pp. 1026–1034, Feb. 2025.

[4] L. Bruno, D. D'Amato, R. Leuzzi, and V. G. Monopoli, "Analysis of electrical aging effects on ac high frequency motor based on exchange market algorithm model parameter identification," *IEEE Access*, vol. 12, pp. 32753–32761, 2024.

[5] X. She, A. Q. Huang, Ó. Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017.

[6] A. von Jouanne and P. N. Enjeti, "Design considerations for an inverter output filter to mitigate the effects of long motor leads in ASD applications," *IEEE Trans. Ind. Appl.*, vol. 33, no. 5, pp. 1138–1145, Oct. 1997.

[7] E. Persson, "Transient effects in application of PWM inverters to induction motors," *IEEE Trans. Ind. Appl.*, vol. 28, no. 5, pp. 1095–1101, Oct. 1992.

[8] R. Phukan, X. Zhao, P. Asfaux, D. Dong, and R. Burgos, "Investigation of staggered PWM scheme for AC common mode current minimization in SiC-based three-phase inverters," *IEEE Trans. Transport. Electrific.*, vol. 8, no. 4, pp. 4378–4390, Dec. 2022.

[9] B. Mirafzal, G. L. Skibinski, and R. M. Tallam, "A failure mode for PWM inverter-fed AC motors due to the antiresonance phenomenon," *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1697–1705, Sep./Oct. 2009.

[10] H. Lewis-Rzeszutek, R. Tallam, R. Phukan, M. Solveson, and T. Clancy, "Simulation of cable charging current and its effects on operation of low power AC drives," in *Proc. IEEE Energy Convers. Congr. Expo.*, Milwaukee, WI, USA, Sep. 2016, pp. 1–7.

[11] S. Lee and K. Nam, "Overvoltage suppression filter design methods based on voltage reflection theory," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 264–271, Mar. 2004.

[12] H. Kim, A. Anurag, S. Acharya, and S. Bhattacharya, "Analytical study of SiC MOSFET based inverter output dv/dt mitigation and loss comparison with a passive dv/dt filter for high frequency motor drive applications," *IEEE Access*, vol. 9, pp. 15228–15238, 2021.

[13] N. Wang, Z. Wang, Z. Liu, G. Xin, X. Shi, and Y. Kang, "A band-stop-type dv/dt filter for terminal overvoltage mitigation of SiC motor drives," *IEEE Trans. Power Electron.*, vol. 39, no. 12, pp. 16391–16399, Dec. 2024.

[14] K. K.-F. Yuen and H. S.-H. Chung, "A low-loss "RL-Plus-C" filter for overvoltage suppression in inverter-fed drive system with long motor cable," *IEEE Trans. Power Electron.*, vol. 30, pp. 2167–2181, Apr. 2015.

[15] Y. Jiang, W. Wu, Y. He, H. S.-H. Chung, and F. Blaabjerg, "New passive filter design method for overvoltage suppression and bearing currents mitigation in a long cable based PWM inverter-fed motor drive system," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7882–7893, Oct. 2017.

[16] W. Zhou, M. Diab, X. Yuan, L. Xie, J. Wang, and Z. Zhang, "Inverter with paralleled modules to extend current capacity and combat motor overvoltage in SiC-based adjustable speed drives," *IEEE Trans. Ind. Electron.*, vol. 71, no. 5, pp. 4474–4484, May 2024.

[17] T. Lackie, Y. Jiang, L. Shillaber, and T. Long, "Motor overvoltage mitigation by active cancellation of reflections using parallel SiC devices with a coupled inductor," *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 11368–11384, Sep. 2023.

[18] W. Zhou, M. Diab, X. Yuan, and C. Wei, "Mitigation of motor overvoltage in SiC-based drives using soft-switching voltage slew-rate (dv/dt) profiling," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9612–9628, Aug. 2022.

[19] W. Zhou, X. Yuan, and Z. Zhang, "An active dv/dt filter to combat motor terminal overvoltage in SiC-based adjustable speed drives," *IEEE Trans. Ind. Electron.*, vol. 72, no. 1, pp. 1076–1081, Jan. 2025.

[20] S. De Caro, "Motor overvoltage mitigation on SiC MOSFET drives exploiting an open-end winding configuration," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11128–11138, Nov. 2019.

[21] X. Li, "Simple switching strategies for dv/dt reduction in SiC-device-based modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1485–1493, Feb. 2023.

[22] M. Sadoughi, A. Sadasivan, F. Fateh, J. He, and B. Mirafzal, "Mitigation of uneven overvoltage distribution in motor windings fed by SiC-based drives using a GaN-based adaptive surge impedance method," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA, 2024, pp. 2385–2391.

[23] M. T. Fard, J. He, L. Wei, R. Ilka, B. Mirafzal, and F. Fateh, "Mitigation of motor reflected overvoltage fed by SiC drives - a new solution based on smart coils," *IEEE Trans. Power Electron*, doi: 10.1109/TPEL.2024.3502352.
[24] B. Mirafzal, G. L. Skibinski, and R. M. Tallam, "Determination of parameters in the universal induction motor model," *IEEE Trans. Ind. Appl.*, vol. 45, no. 1, pp. 142–151, Jan./Feb. 2009.
[25] D. Busse, J. Erdman, R. J. Kerkman, D. Schlegel, and G. Skibinski, "Bearing currents and their relationship to PWM drives," *IEEE Trans. Power Electron.*, vol. 12, no. 2, pp. 243–252, Mar. 1997.
[26] Y. Xie, J. Zhang, F. Leonardi, A. R. Munoz, and M. W. Degner, "Investigation of surge voltage propagation in inverter-driven electric machine windings," *IEEE Trans. Ind. Electron.*, vol. 70, no. 10, pp. 9811–9822, Oct. 2023.
[27] Y. Azadeh, "Cable and motor winding impedance interactions in motor drive systems and its impact on HF overvoltages," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 1244–1253, Jan. 2024.

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