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Performance and Scalability of Strain Engineered 2D $MoTe_2$ Phase-Change Memristors

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ABSTRACT This work presents a performance optimization and scalability study of a two-dimensional vertical molybdenum ditelluride ($MoTe_2$) phase-change memristor. The device switches between the semimetallic (1T') and semiconducting (2H) states under an electric field. Process-induced strain engineering techniques at the contacts reduces the switching energy barrier, biasing the active region closer to the phase switching point. This work focuses on optimizing this technique to achieve the best yield and device performance, with a low switching voltage ($\leq$0.5V) and high on/off ratio $\geq 10^5$. Small length and area of the contact between the metal stressor and the 2D 1T'-$MoTe_2$ flake are critical for high yield and performance, potentially due to lowered chances of encountering defects introduced during the fabrication process ($L \leq 0.6\mu m$ and $A \leq 0.3\mu m^2$). Smaller flake contact perimeters $\leq 1.2\mu m$ also reduce defect incidence, and increases on/off ratios. The switching voltage is influenced by the contact-flake geometry, exhibiting a lower value for 2D flake geometries with contact angles $\leq 65^o$ likely due to geometric variation in strain distribution effects from process-induced strain engineering. These results demonstrate that by accounting for device geometry, our process may achieve yield approaching 90% with consistent low switching voltage and high on/off ratio. Yield and performance properties become better when scaled down in size due to our phase-change mechanism, which is the opposite behavior to most conductive filament based memristors.

INDEX TERMS Memristor, two-dimensional materials, strain engineering, phase-change memory, device fabrication.

I. INTRODUCTION

The memristor is a two terminal device that can be switched between a high resistance and low resistance state under applied voltage bias, causing a characteristic hysteresis loop [1], [2]. This hysteretic resistive behavior makes memristors promising for next-generation memory and neuromorphic computing applications [3], [4], [5]. Two-dimensional (2D) materials can be used to fabricate these devices, attracting great attention due to their lower-power operation, compatibility with flexible substrates, and potential integration through 3D monolithic integration, while also offering benefits such as reduced latency, reduced switching voltage, and reduced footprint [6], [7]. Despite the benefits, both regular and 2D memristors typically rely on filamentary conduction from the motion of defects, grain boundaries or metal ions to operate. This results in highly variable behaviors, limited scalability, and fewer engineerable or designable parameters, making them unsuitable for translation from laboratory-based demonstration to industrial applications [8].

Recent advances from our group and others include the development of high-performance vertical molybdenum ditelluride ($MoTe_2$) phase-change memristors [9], [10], which operates on a fundamentally different mechanism. A forward bias voltage drives an electric-field-induced phase transition in 2D $MoTe_2$, switching between semimetallic (1T') and semiconducting (2H) states to represent the two resistive states. This phase-change mechanism has the

potential to offer more stable and controllable switching compared to traditional filamentary memristors due to it relying less on random processes [9], [10], [11], [12], [13].

While the strain-phase change mechanism has been proven effective, uncontrolled parameters such as the shape of the exfoliated flakes or defects inserted during fabrication present significant challenges in reproducibility and performance reliability. The distinct geometries of each exfoliated 2D flake increases the complexity when dealing with device performance, since it affects how the strain is distributed. In contrast to our group's original work [10], which primarily focused on validating the strain-induced phase change mechanism in 2D $MoTe_2$, here we explore remaining open questions related to device scalability and performance consistency. Parameters such as flake contact area and flake geometry were not considered previously, and thus high performance devices were not reliably achieved. In this work, to obtain predictable memristor behavior, we now focus on understanding which parameters are crucial to achieving consistent high performance. Thus, here we present an optimized fabrication process to obtain consistently high performance in 2D phase-change memristors with high yield, reliable low switching voltage and high on/off ratio.

It is shown in this work that devices achieve their best performance as they are scaled down in size, a beneficial feature to any potential future applications. This is counter to most memristors, which rely on defects to form conductive pathways that facilitate the switching between resistance states leading to poorer performance as devices are scaled down. Since our device operates through a phase-change mechanism, we are not limited by the same issues and in this work it is shown that through defect-free fabrication and control of strain distribution, we may address scalability and device variability challenges present in current 2D memristor technology.

II. STRAIN-BASED $MoTe_2$ MEMRISTOR

Process-induced strain engineering techniques have been used in commercial complementary metal-oxide-semiconductor (CMOS) nanofabrication processes since the 90-nm technology node [14]. Uniaxial tensile or compressive strain is used to selectively enhance the mobility of electrons or holes for n-type or p-type metal-oxide-semiconductor field effect transistors. This process was originally done through the deposition of highly stressed thin films that relax, introducing strain in the transistor channels [15]. This approach can also be applied to 2D materials on a device-to-device basis, with control of the magnitude and direction of the strain [16]. To achieve that control, parameters like film force and geometry of the film stressor are important since these factors control strain magnitude and strain distribution. The film force, film stress $\times$ film thickness, can be used to quantify the strain magnitude applied by the film to the 2D flake [17]. The Stoney equation [18] enables the calculation of the average film stress (σ). The applied film force (F_f) is related to the film stress and the film thickness (t_f) by $F_f = t_f \times \sigma$ [19], [20].

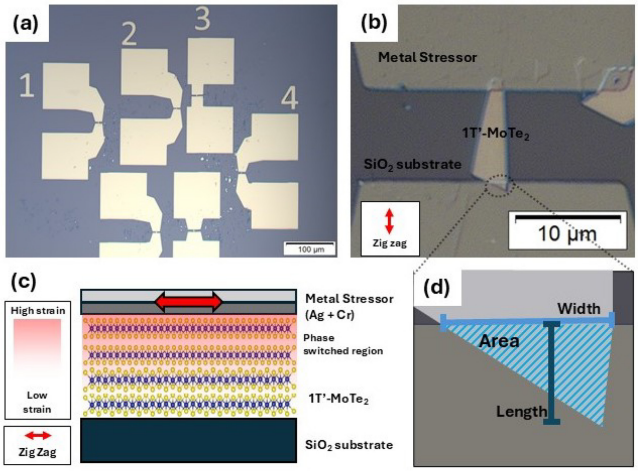

FIGURE 1. Optical micrograph of a) multiple devices and b) a single device. c) Schematic of strain transfer from the metal stressor to the 2D material and d) parameters measured to obtain flake contact length, width, and area.

In our memristor design, a stressed metallic thin film applies uniaxial tensile strain to 1T'-$MoTe_2$ (Fig. 1a,b). The strain is transferred from the metal contact to the 2D material, from the top layers down, through van der Waals interactions [16], [17], [21]. The strain transfer length scale is finite in the out-of-plane direction of $MoTe_2$, restricting the phase transition to the uppermost layers, while the layers past ~7nm remain unstrained [10]. A phase-transition from semimetallic (1T') to semiconducting (2H) states is induced by the uniaxial strain, happening underneath the contacts. This both naturally creates a self-aligned vertical transport structure (Fig. 1c), and utilizes the strain to put the material closer to the phase transition point, where small perturbations from an electric field can induce the phase-transition. The electric field is applied out-of-plane from a two-terminal voltage that ranges from -1.2 to 1.2V. The device operates in a high resistance state (HRS) when in the semiconducting 2H phase and a low resistance state (LRS) when it is in the semimetallic 1T' phase, with switching triggered by specific voltage thresholds. It has been shown in our previous work that increasing tensile strain applied along the zigzag direction, alters the material's phase stability, lowers the barrier to phase transition, and enhances device performance. The application of tensile strain along the zigzag direction often also results in compressive strain along the armchair direction, from the positive Poisson ratio of the flake, affecting the phase transition behavior and the strain distribution [22]. Therefore, the strain-induced phase transition mechanism is highly sensitive to the crystallographic orientation of the $MoTe_2$ flakes and the distribution of the strain applied from the stressed metal contact [10].

Considering the sensitivity of the phase-change to individual process-parameters at the edge of the 2D flake, variations in the geometry of the flakes, the area and the length

of contact, and the quality of the flake edge perimeters are important in determining the full potential of these $MoTe_2$ memristors. Here, we provide a detailed study of these process parameters that play a large role in achieving consistent high-performance in this class of device, including contact area, contact length, contact angle, and flake edge-perimeter.

III. DEVICE FABRICATION AND CHARACTERIZATION

1T'-$MoTe_2$ multilayer flakes were tape exfoliated from the bulk crystal along its identified zigzag direction. The 2D memristors were fabricated on SiO_2 substrates, demonstrating the potential for CMOS compatibility [23] since previously demonstrated results were performed on MgO substrates [10]. The substrates were cleaned in oxygen plasma at 100 W and 200 mTorr for 4 minutes, to ensure surface purity. The plasma cleaner chamber was previously cleaned, under the same conditions, for 20 minutes before placing the substrates. Post-cleaning ($\leq$1min), 1T'-$MoTe_2$ was exfoliated onto SiO_2 and baked at 100°C for 90 seconds to improve flake adhesion. The tape was slowly removed, and the chip was placed into acetone and taken to an ultrasonic bath for 20 minutes, to delaminate poorly adhered flakes [24]. Direct-write laser photolithography was used to pattern the memristors on the 1T'-$MoTe_2$ flakes. The metal contact geometries, flake thickness range (7 to 25 nm) and flake angle (aligned along crystal zigzag direction) were the same for all devices, varying only the length of the metal contact on the flake as shown in Fig. 1d. For the metal contacts, 25 nm of silver (Ag) and 25 nm of chromium (Cr) were deposited, using e-beam evaporation at a rate of 1Ås^{-1}, under a chamber pressure below 5x10^{-6} torr. To quantify the strain applied by the deposited film, the film force was measured by placing a clean microscope coverslip with the sample into the e-beam evaporator for the metal contact deposition step. Before and after the deposition, the radius of curvature of the coverslip was measured using contact profilometry and the film force was calculated based on the Stoney equation mentioned previously. Since the transferred film stress primarily depends on the film force (film stress $\times$ film thickness), rather than deposition area, the film force exerted at the 2D material under the metal contact is consistent with the large-area calibration coverslip [17].

The *I-V* characteristics were obtained through a Keysight 2901A Precision Source/Measure Unit (SMU) (Fig. 2). A wire bonder was used to connect the metal contacts to a resistivity puck placed into a sample wiring test station, allowing the devices to be analyzed in the SMU. The voltage at which the device turned on was called switching voltage and the on/off ratio was determined by the ratio between the current in the on and off state at 100 mV (Fig. 2a). The endurance test was performed using 300 full *I-V* sweeps of the device, ranging from -0.5 to 0.5V. The current compliance was 100μA. The current at $-$100mV was extracted in every cycle, where only curves with successful switching were included. Devices that exhibited resistive

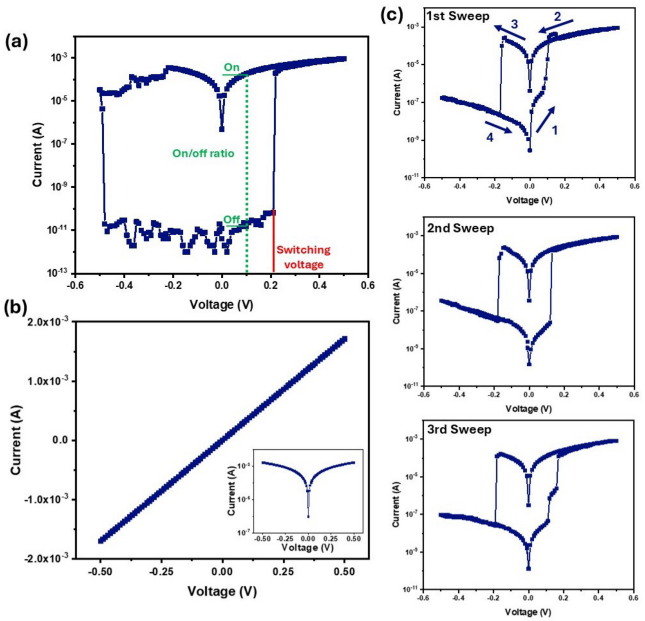

FIGURE 2. **a) *I-V* characteristic of the strain-engineered memristor with labels indicating on/off ratio and switching voltage (switched device) b) *I-V* characteristic of a device that did not switch (linear device). Inset: Same plot in log scale. This device has a 0.742μm^2 area, increasing the likelihood of occurring encountering defects that impede the switching behavior. c) *I-V* characteristic of a device over a cycle of three sweeps.**

switching behavior were classified as 'switched devices' (Fig. 2a) and the ones that did not show switching behavior, without the hysteresis loop typically seen in memristors, were classified as 'linear devices' (Fig. 2b). Figure 2c shows the device behavior over a cycle of three sweeps.

Initial fabrication process parameters were chosen based on empirically demonstrated 'best conditions' for device performance as reported by Hou et al. [10]. These parameters are as follows: film force of 25 N/m from the contacts, with contact/flake overlap designed perpendicular to the zigzag axis to apply tensile strain aligned along the zigzag direction and the contact/flake overlap length being $\leq$1.1μm (Fig. 1d). This serves as the starting point for our exploration into varying process parameters to increase device yield and reproducibility.

IV. SCALING EFFECTS ON MEMRISTOR PERFORMANCE

Device scaling was tested by varying the contact length between the metal stressor and the flakes during the fabrication process. The corresponding contact areas and other geometric parameters were measured using optical microscopy images and the software ImageJ. These measurements were confirmed by scanning electron microscopy (SEM). As shown in Figure 3, device yield increases for both shorter contact length, as well as smaller contact area (purple to blue), and decreases for larger contact length and larger contact area (purple to red). This is the opposite behavior of typical filamentary memristors, which rely on defects or grain boundaries to seed switching. In contrast,

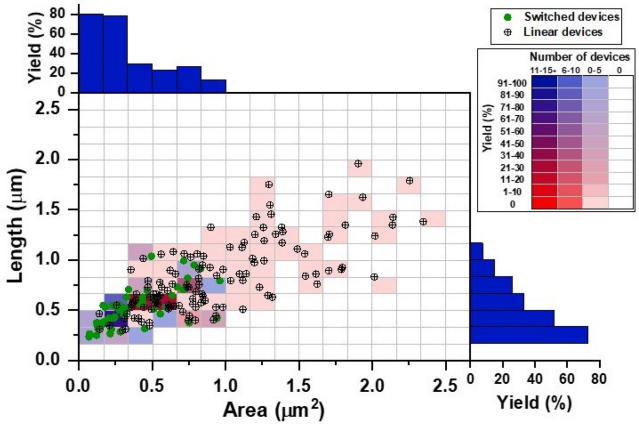

FIGURE 3. Yield in terms of area, length, and number of devices. Where darker colors indicate a higher number of devices, and the yield is indicated by the red (0%) to blue (100%) color range.

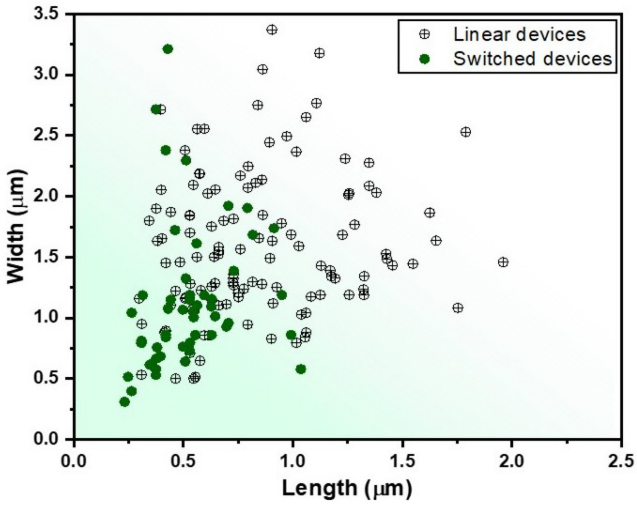

FIGURE 4. Length *vs* width for all devices, linear and switched.

defects in our device impede switching, and smaller contact areas lead to reduced probability of encountering defects that may short out the device. A Poisson defect model estimated density of device shorting defects, introduced during the fabrication process, as approximately 2 per square micrometer (defects/μm^2) [25], [26]. For comparison, recent work has shown under Au metal evaporation at $5x10^{-6}$ torr, an average defect density of 17.47 μm^{-1} [27], measured in cross-sectional transmission electron microscopy (TEM) images. However, these quantified defects vary in size or clustering, such that not all defects reach the threshold to impede switching. Larger defects and clustered regions increase the probability of critical failures, reducing the yield [28], [29]. Plug formation during metal deposition can introduce such defects, due to atom or cluster bombardment and localized heating [30].

In our experiment, shorter length is also seen to enhance device yield. This may be due to more efficient phase switching because the induced strain is more uniformly localized near the edge, as demonstrated in previous works [10]. Although length and area are intrinsic correlated, their effect on the device performance varies. Figure 4 presents the length *vs* width distribution of all devices (linear and switched). A significant portion of the switched devices is concentrated in the bottom-left region, where both length and width are smaller. There are several devices with length $\leq 0.6\mu m$, however, the majority of successfully switched devices exhibits both a length $\leq 0.6\mu m$ and a width $\leq 1.25\mu m$. Regardless of the shape, with a smaller length and width, the device area will consequently decrease, reinforcing that the contact area is the dominant factor influencing the performance. A small area increases yield, even with variations in length, whereas maintaining a small length alone does not. Thus, smaller contact lengths ensures the device is experiencing adequate strain uniformity for phase switching, but its a small area that minimize defects and increases the yield. These results confirm that our memristor is improved as it scales down in size, unlike most other memristor implementations where defects are needed to create the conductive bridge.

V. OPTIMIZATION OF MEMRISTOR PERFORMANCE

To understand the factors that play a role in engineering for deterministic performance and yield in phase-change memristors, we now explore the contact/flake geometry dependence on device performance. While previous work has demonstrated film force, strain directionality, and contact length dependency on device switching characteristics, there are still many contact geometry dependent variables in engineering repeatable device behavior, particularly a high on/off ratio and low switching voltage. When exfoliated, the 2D materials form flakes with a high variability of shapes, even if exfoliated from the same bulk crystal. This remaining variability induced by the flake geometric shape and possible imperfections of the 2D material could lead to the memristors lack of performance reliability. To address this, we conducted additional analysis of other parameters that could influence the device performance. Regarding this analysis, a switching voltage ≤ 0.5 V was considered low and an on/off ratio $\geq 10^5$ was considered high.

From Fig. 3 it is possible to identify that most switched devices were within the 0 to 0.3 μm^2 area range. This observation helps eliminate one confounding variable, allowing the analysis to focus on other factors that affect device performance. By selecting this range and plotting the switching voltage *vs* on/off ratio graphic (Fig. 5a), the devices end up in three different regions. Region 1 (blue) represents the best condition, where the devices have a high on/off ratio and a low switching voltage. Region 2 (green) has a low switching voltage, but a low on/off ratio and Region 3 (orange) with a high switching voltage and a low on/off ratio. To find potential causes of each behavior, measurements of flake edge perimeter and contact angle were done (Fig. 5b).

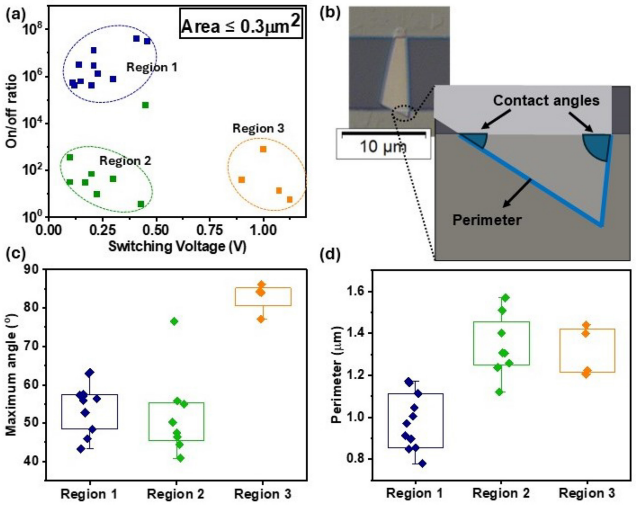

FIGURE 5. **a) Switching voltage *vs* on/off ratio for the devices with an area ≤0.3 μm^2, categorized into regions based on performance. b) Parameters measured to obtain the flake edge perimeter and contact angles. c) Maximum contact angle for the regions described in a) and d) flake edge perimeter for the regions described in a).**

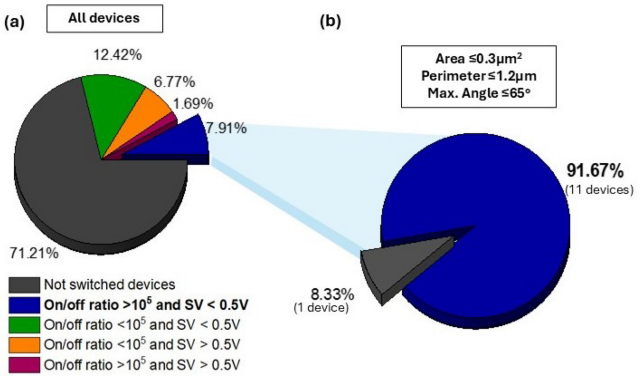

FIGURE 6. **a) All devices fabricated and b) devices with optimized fabrication parameters distributed according to electrical characteristics, switching voltage (SV) and on/off ratio.**

Other parameters, like contact flake width, total flake area, length, and width, did not show a strong correlation.

The results of the flake edge perimeter and contact angle are shown in Fig. 5c and d, showing region 1 having low perimeter and region 3 having larger contact angle. This suggests larger contact angles lead to high switching voltages, and larger perimeters lead to lower on/off ratio. The maximum angle between the metal stressor and flake is related to the geometry of the flake portion in contact with the metal stressor. This geometry likely influences the strain distribution [10], [16], [17], [31], which affects the voltage needed to switch the devices between the on and off states. Variations in strain distribution could influence the uniformity of phase-change, consequently affecting the electrical properties obtained, such as the voltage required for phase transitions. Our group has shown how the controlled application of strain via patterned stressors can affect the strain distribution onto the 2D flake [16]. Similarly, here we have observed that the geometry of the 2D flake could also be responsible for strain distribution variations according to the maximum angle formed between the metal contact and the edge of the flake. This suggests that a subset of flake geometries benefit the device performance, likely due to their uniform strain distribution.

On the other hand, the on/off ratio is affected by the flake edge perimeter in contact with the metal stressor. Edge defects could influence the change in resistance between the on and off states. General findings from defect studies in a similar material (2H-$MoTe_2$) reported improvement in device performance, such as electrical conductivity and stability, by reducing defect density of the material [32], focusing primarily on bulk materials properties. It is plausible to assume that defects located at the edge may interact with the metal contact, creating a nonuniform switching. Consequently, smaller perimeters decrease the chance of encountering edge defects, leading to higher on/off ratios.

VI. PARAMETERS DEPENDENCE

When analyzing all the fabricated devices (177), there is approximately a 30% chance of having a switched device. Within that 30% we have different device behaviors, with a probability of 7.91% of fabricating the ideal case, with a high on/off ratio and a low switching voltage (Fig. 6a).

Considering only the devices with an area $\leq 0.3\ \mu m^2$, perimeter $\leq 1.2\mu m$ and a maximum angle $\leq 65°$, approximately 91.67% of them exhibited a low switching voltage and high on/off ratio, the ideal operation of a memristor. These parameters represent the optimal design conditions that contribute to achieving the best performance. Thus, among the fabricated devices that met these geometric criteria, the yield within the best case scenario increases from 7.91%, considering all fabricated devices, to 91.67%, when applying the discussed parameters (Fig. 6b). In addition to achieving a high on/off ratio and low switching voltage, the ideal switching devices also exhibit high endurance properties (>300 switching cycles), similar to our previously published results [10]. Variations in the film force and in fabrication from chip-to-chip did not affect the overall device behavior, as we found no significant differences between each measured chip.

VII. CONCLUSION

We have shown that optimizing the 2D flake-contact area, flake edge perimeter, and the maximum contact angle, significantly enhances the memristor performance, achieving 91.67% yield and a reliable low switching voltage ($\leq$0.5 V) and high on/off ratio ($\geq 10^5$). The area and the length play distinct roles in the device performance: smaller areas increase the yield by reducing the likelihood of encountering defects that could impede the phase transition, and shorter lengths ensure more uniform strain profile, preventing non-switched regions from shorting the devices. Most switched

devices had an area $\leq 0.3\mu m^2$, among these devices, those with a flake edge perimeter $\leq 1.2\mu m$ exhibited a higher on/off ratio ($\geq 10^5$), likely due to the reduced number of flake-edge defects allowing for a larger change in resistance between LRS and HRS. Additionally, a maximum flake-contact angle of 65° likely represents an optimal flake geometry, where the strain distribution is more uniform, affecting the phase transition occurrence and decreasing the voltage needed to switch between phases. This work identifies parameters that collectively enhance device performance, building on the findings of our previous study, where device behavior was less controlled. Compared to existing memristor technology, that have limited reproducibility and scalability, our optimized fabrication process parameters are not restricted by the same issues. Using our strain-engineered phase-change mechanism, we show a 2D $MoTe_2$ memristor with consistent low switching voltage and high on/off ratio, high yield, and favorable scalability behavior, significantly improving device performance when geometric factors are accounted for. While this study demonstrates an enhanced fabrication approach, scaling to an industrial level will require the growth of a single-crystalline, wafer-scale, high-quality 1T'-$MoTe_2$ thin films on silicon, which may support consistent patterning in the optimized flake geometry.

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