Steady-State and Small-Signal Analysis of High-Ratio Hybrid Buck Converters With Enhancement to State-Space-Averaging Methodology

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***Abstract*—This paper proposes convergence enhancement to state-space averaging (SSA) methodology for steady-state and small-signal analysis of high-ratio hybrid DC-DC converters, first using analysis of Double-Step-Down (DSD) topology, including parasitics, as an example, then extending to other hybrid topologies with different numbers of capacitors and inductors. The enhanced SSA method can be used to: *1)* derive small-signal control-to-output transfer functions, which is essential to optimize the compensator for fast and stable closed-loop operation; *2)* calculate steady-state inductor currents, output voltage, input current and the voltage(s) across the flying capacitor(s), V_{CFs}, which is important to determine steady-state characteristics and performance; *3)* include circuit non-idealities such as parasitics and timing mismatches; and *4)* evaluate V_{CF} balancing property by the proposed matrix invertibility principle and added constants, and determine whether dedicated V_{CF} balancing circuits can be eliminated, which is considered an important benefit with reduced complexity and improved reliability. The theoretical results of DSD are then plotted in MATLAB and verified in simulations using PSIM and Cadence periodic transfer function (PXF) analysis, and measurement results using GaN devices. The simulation and measurement results match well with theoretical analysis. The enhancement is then extended beyond the DSD topology to analyze emerging hybrid topologies with more switched inductors and capacitors, future-proofing its capability to be applicable to new hybrid topologies.**

***Index Terms*—State-space averaging, small-signal analysis, hybrid switching converters, point-of-load converters, double step down, dual-inductor hybrid, flying capacitor balance, flying capacitor multilevel converter.**

I. Introduction

HYBRID DC-DC power converter designs, which include both switched inductive and capacitive components and take advantage of both types, are one of the most popular research topics in power electronics and power management integrated circuits (PMICs) in the recent decade due to the booming applications in data centers (48V to Point-of-Load, PoL) and automobile (24 – 60V to PoL). Every year, many new topologies are being introduced, each has its own characteristics. For power converters, steady-state analysis is needed to understand the DC characteristics, and small-signal analysis is needed to reveal the transfer functions to optimize the dynamic response (e.g., load transients and reference tracking), while ensuring stability. The mathematical model for a power converter, especially in state-space form, is also imperative to be able to train machine learning models or form a digital twin, for instance, to investigate better topologies for a given application. In the literature, such analysis has been done for traditional 2-level buck, and the more recent flying-capacitor multilevel (FCML), especially 3-level DC-DC buck converters [1], [2], [3], [4], [5], [6] with some papers also considering parasitics for these converters [7], [8], [9], [10], [11]. However, there lacks a systematic approach for newer hybrid topologies, especially including non-idealities (e.g., parasitics and timing mismatches) and for high-conversion-ratio operations.

Among the many new hybrid topologies, the double step down (DSD) topology, which is also known as series-capacitor topology, is one of the earliest, most popular and widely studied hybrid topologies. For steady-state analysis, several papers [12], [13], [14] highlighted the important benefits of DSD converters: the intrinsic balancing of flying capacitor voltage and inductor currents; and several others studied the balancing of flying capacitors in FCML converters using conventional state-space averaging (SSA) [15], [16]. However, systematic analysis was not provided to prove this phenomenon. For small-signal behavior, the control-to-output transfer function was mentioned in [1], but no explanations, derivations or verifications were provided, and the impacts of parasitics or timing-mismatches were not considered. More importantly, the previous works utilizing SSA mostly used traditional methodology to derive the transfer functions only, without regards to DC operating point ignoring the insights provided by the steady-state results and the model even fails to converge, as will be discussed in a later section, for several recently proposed PoL topologies such as dual-inductor hybrid (DIH) [17], [18] known for their inherent balancing property similar to DSD and better PoL efficiency.

The traditional SSA methodology only proves to be of limited use in its current form owing to convergence failure, e.g., it can provide the correct steady-state operating points for the DSD which has only one flying capacitor and inherent

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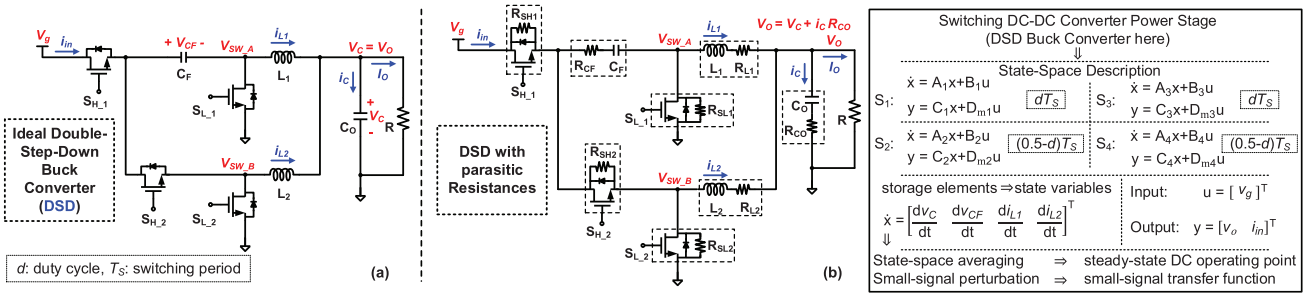


Fig. 1. Double-step-down (DSD) power stage with (a) ideal components, and (b) parasitic resistances and its state-space model.

balancing property. On the other hand, it also appears to be useful for 3-level topology [6], but only with several non-idealities included that vary a lot between integrated and discrete designs. However, as the topologies become more complex, the modelling of the converter becomes challenging as unique steady-state results can no longer be derived. For instance, many recent topologies are comprised of parallel current paths with capacitors to significantly reduce conduction losses, e.g. multiple current paths for the same inductor current shared by flying capacitors in DIH topologies, resulting in dependencies between the flying capacitors making the traditional SSA model incomplete due to the lack of a systematic method of including dependencies. In addition, when topologies such as FCML require V_{CF} calibrations for proper operation, traditional SSA model again fails to converge. This makes the results derived from traditional SSA not align with the actual results derived from standard steady-state analysis, i.e., with volt-second and amp-second balance expressions. As a result, an already complicated control of topologies with more inductors, flying capacitors, power switches, the modelling and design become cumbersome.

In view of the needs, this work proposes convergence enhancement to traditional SSA methodology to provide systematic steady-state and small-signal analysis while increasing the scope of SSA making it applicable to any non-resonant hybrid topologies. For topologies with singular state matrix, although the steady-state solution can be derived following complicated procedure of substitution and elimination of state variables using dependencies and/or calibrated capacitor voltage expressions to achieve reduced-order invertible state matrix, it still requires solving another system of equations for dependencies besides losing transient information from the model. This work focuses on completing the state matrix including calibrations and dependencies rather than solely determining the steady-state solution that results in convergence of the model in a simpler and systematic manner without loss of dynamic information for passives making the state matrix suitable for more accurate modeling [19], [20], [21]. Another key contribution of this work is the theoretical determination of intrinsic inductor-current and flying-capacitor-voltage (V_{CF}) balancing of a given topology, which is an important characteristic to determine complexity and feasibility when new topologies are proposed. If a topology lacks such intrinsic balancing, dedicated circuitry for active sensing of V_{CF} and inductor current, with closed-loop control become necessary, whereby it increases design complexity while influencing stability. With emerging interests, the framework would also open new possibilities for automated topology generation, offering a structured approach to next-generation power converter design. In this paper, the popular DSD (Fig. 1) topology serves as an initial case study before extending the proposed methodology to other hybrid topologies. Specifically:

The state-space averaging will include: 1) computation of basic DC operating point that is necessary to derive the small-signal transfer function; and more importantly, those DC operation points comprise 2) the average voltage V_{CF} across the flying capacitor C_F, which is an important parameter to ensure proper operation of the converter without exceeding the voltage rating of the devices if lower-voltage devices are used, or increasing the inductor current ripples, or affecting the symmetry between multiple inductor currents, all of which directly affect the efficiency; and also 3) the average inductor currents of the inductors, which are important to be balanced to optimize the efficiency and reduce output voltage ripples.

The small-signal analysis, as a follow-up step of determining the DC operating point, derives control-to-output transfer functions, for each non-ideal element of DSD separately to highlight the effects of each element. The results are important, in general, for optimizing the compensation network for fast and stable closed-loop operation.

The paper is organized as follows: Section II discusses the derivation of SSA model for DSD, followed by Section III providing detailed steady-state and small-signal analysis results of DSD with parasitics. Then, Section IV generalizes the SSA matrix invertibility principle to a range of buck converters and finally conclusions are provided in Section V.

II. State Space Averaging for the DSD Topology

There are four states of operation in DSD buck converters [12] resulting in four matrices for state-space modelling denoted by the subscript of each A, B, C and D_m matrices where additional subscript m is being used for matrix D to distinguish it from the DC component of duty cycle, D. These matrices with the parasitics included are given in Table I and can be used along with the durations of each state to get averaged matrices as follows:

$$M = d\,(M_1 + M_3) + (0.5 - d)(M_2 + M_4), \tag{1}$$

where d is the duty cycle and M is A, B, C or D_m matrix. The input vector, u, comprises the supply voltage, V_g. Performing steady-state analysis for the DSD power stage using the four storage elements in the power stage as the state variables results in a set of four differential equations, i.e., the two inductor currents and the two capacitor voltages relating the state variables with the rates of change of these variables and the input voltage. The input voltage and state-variable coefficients in these equations determine the elements of the matrices B and A, respectively. Similarly, the equations relating

TABLE I
DSD STATE-SPACE AVERAGING MATRICES

$A_1 = \begin{bmatrix} -\gamma_1 & 0 & \gamma_2 & \gamma_2 \\ 0 & 0 & 1/C_F & 0 \\ -\gamma_4 & -1/L_1 & -\gamma_7 & -\gamma_3 \\ -\gamma_6 & 0 & -\gamma_5 & -\gamma_8 \end{bmatrix}$	$A_{2,4} = \begin{bmatrix} -\gamma_1 & 0 & \gamma_2 & \gamma_2 \\ 0 & 0 & 0 & 0 \\ -\gamma_4 & 0 & -\gamma_9 & -\gamma_3 \\ -\gamma_6 & 0 & -\gamma_5 & -\gamma_8 \end{bmatrix}$
$A_3 = \begin{bmatrix} -\gamma_1 & 0 & \gamma_2 & \gamma_2 \\ 0 & 0 & 0 & -1/C_F \\ -\gamma_4 & 0 & -\gamma_9 & -\gamma_{10} \\ -\gamma_6 & 1/L_2 & -\gamma_{11} & -\gamma_{12} \end{bmatrix}$	$B_1 = \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 \end{bmatrix}^T$ $B_2=B_3=B_4= [0\ 0\ 0\ 0]^T$
$\alpha_1 = R\|\|R_{CO}$	$\alpha_2 = \alpha_1/R_{CO}$
$\gamma_1 = \alpha_2/(RC_O)$	$\gamma_2 = 1/C_O - R_{CO}\gamma_1$
$\gamma_3 = \alpha_1/L_1$	
$\gamma_4 = \alpha_2/L_1$	$\gamma_5 = \alpha_1/L_2$
$\gamma_6 = \alpha_2/L_2$	
$\gamma_7 = \beta_3/L_1$	$\gamma_8 = \beta_4/L_1$
$\gamma_9 = \beta_2/L_1$	
$\gamma_{10} = \beta_1/L_1$	$\gamma_{11} = \beta_1/L_2$
$\gamma_{12} = \beta_5/L_2$	
$\beta_1 = R_{SL1} + \alpha_1$	$\beta_2 = R_{L1} + \beta_1$
$\beta_4 = R_{L2} + R_{SL2} + \alpha_1$	
$\beta_3 = R_{CF} + R_{SH1} + R_{L1} + \alpha_1$	$\beta_5 = R_{CF} + R_{L2} + R_{SH2} + \beta_1$
$C_1 \begin{bmatrix} \alpha_2 & 0 & \alpha_1 & \alpha_1 \\ 0 & 0 & 1 & 0 \end{bmatrix}$	$C_{2,3,4} \begin{bmatrix} \alpha_2 & 0 & \alpha_1 & \alpha_1 \\ 0 & 0 & 0 & 0 \end{bmatrix}$
$D_{m1\sim m4}[0]$	

to the output vector, state vector and the input vector are used to determine the components of C and D_m matrices. As small ripple and relatively higher output power capability are typically required in PoL applications, only continuous-conduction mode (CCM) is considered, and non-linear techniques to approximate large ripples such as MFA [19], KBM [20], [21] or TIMF [20] are not considered in this paper.

The state-transition matrix, $(sI–A)^{-1}$, when evaluated at DC ($s = 0$) results in the inverse of the matrix A. However, if determinant of a matrix is zero (a singular matrix), its inverse does not exist. This property serves as an important result making SSA useful not only to model the dynamic response, where SSA is often used, but also to determine steady-state balance of a converter as will be discussed later.

A. Matrix Invertibility in DSD State-Space Model

Invertibility of matrix A in the state-space model provides useful insights. The steady-state matrix equation $Ax+B=0$ can only have a unique solution if matrix A is invertible with the state variable matrix x having a unique set of values given by:

$$x_0 = -A^{-1}Bu_0 = [V_C\ V_{CF}\ I_{L1}\ I_{L2}]^T, \tag{2}$$

where the subscript in x_0 and u_0 indicate the DC values. This invertibility can be determined by the determinant of the matrix, for instance. In case the determinant is zero ($|A| = 0$), there is no unique set of values in x_0 that can satisfy (2). In other words, it can either have no solution or infinitely many solutions depending on matrix B. This result is especially important for the V_{CF}, which can only have a unique DC value at steady-state if the inverse of matrix A exists. This principle is also apparent for the state-space model of the 3-level converter [6], explored in detail later in the paper, where matrix A has a determinant of zero (and hence no unique value of V_{CF}). In contrast, the matrix A in Table I for DSD has none of the rows filled with zeros even in an ideal case (ignoring parasitics) indicating that V_{CF} is always balanced to half of V_g in steady-state in the DSD topology, which explains its intrinsic V_{CF} balancing capability, in contrast to the 3-level converters [6].

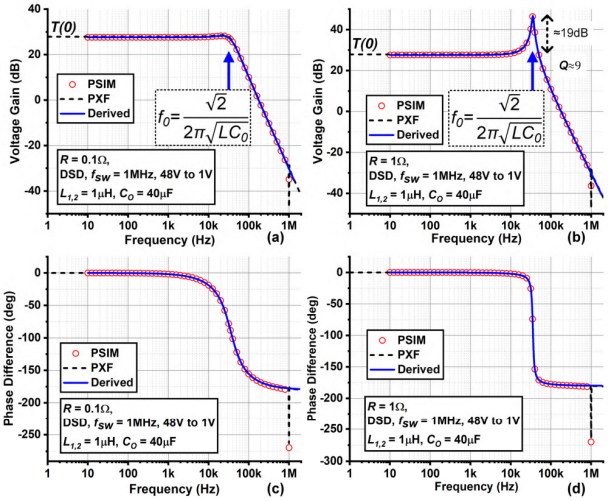


Fig. 2. Bode plots for ideal small-signal control-to-output transfer functions of DSD with voltage gain at (a) 0.1Ω load and (b) 1Ω load, and with phase difference at (c) 0.1Ω load and (d) 1Ω load.

B. Steady-State and Small-Signal Analysis of DSD

The state-space model can be simplified in s-domain, resulting in the following expression:

$$y(s) = (C(sI - A)^{-1}B + D_m)u(s), \tag{3}$$

to determine the output s-domain vector containing line-to-output transfer function, for instance. Solving (3) at DC ($s=0$) gives the following expression comprising the DC values of the output vector:

$$y_0 = \left(-CA^{-1}B + D_m\right)u_0 = [V_O\ I_{in}]^T, \tag{4}$$

where the matrices C and D_m are computed using output voltage and capacitor current expressions, given by $V_O = V_C + i_C R_{CO}$ and $i_C = i_{L1} + i_{L2} - i_O$, respectively; the expressions can be simplified to write V_O in terms of state variables as follows:

$$V_O = R\|R_{CO}\left(\frac{1}{R_{CO}}.V_C + 0.V_{CF} + i_{L1} + i_{L2}\right) \tag{5}$$

In order to determine the small-signal control-to-output transfer function, perturbation can be applied in the state-space model with each state-space parameter having a quiescent (DC) and a small-signal AC component [1], [4]. In other words, $x = x_0 + \hat{x}$, $d = D + \hat{d}$ and $u = u_0 + \hat{u}$. Using these expressions, the simplification of the state-space model gives:

$$\dot{\hat{x}} = A\hat{x} + B\hat{u} + E\hat{d}, \tag{6}$$

where matrix E is given by:

$$E = (A_1 + A_3 - 2A_2)\,x_0 + (B_1 + B_3 - 2B_2)\,u_0 \tag{7}$$

computed using the state-space matrices given in Table I. Finally, the transfer function from the perturbation analysis can be computed as follows [3]:

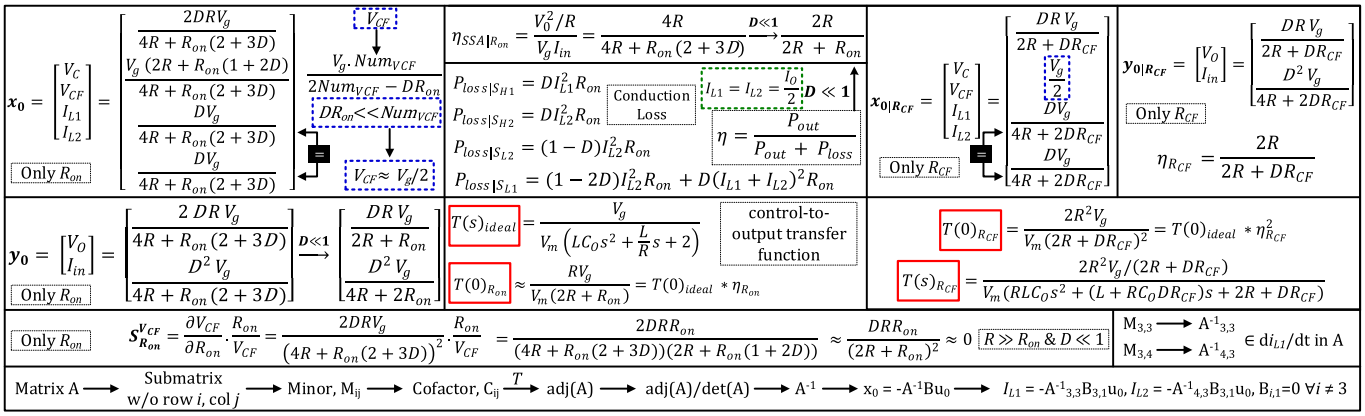
$$T(s) = -trace((sI - A)^{-1}EG), \tag{8}$$

where matrix G is related as $\hat{d} = G\hat{x}$ and using (5) is given by:

$$G(s) = -\frac{A_{cmp}(s)\,R\|R_{co}}{V_m}\left[\frac{1}{R_{co}}\ 0\ 1\ 1\right], \tag{9}$$

TABLE II

DSD DC OPERATING POINTS FOR RON OF POWER SWITCHES AND FOR ESR OF CF



where compensation transfer function, $A_{cmp}(s)$, for the closed-loop operation is included in the expression of $G(s)$ to maintain generality but it is unity in this case and V_m is the peak-to-peak voltage of the ramp signal used to generate pulse-width modulated (PWM) gate drive signals. As mentioned above, the DC operating points are necessary to derive the transfer function(s) using (7), therefore it is essential to have the unique steady-state values, only feasible with invertible matrix A.

The frequency responses of the ideal transfer functions of DSD derived using the state-space model along with the parameters used for both heavy- and light-load conditions are shown in Fig. 2. The same responses from the PSIM AC sweep and the Cadence periodic transfer function (PXF) simulations, performed under the same conditions, are also added to the same plots for comparison, both of which agree well with the derived model. In summary, the ideal control-to-output transfer function, $T(s)_{ideal}$ in Table II, of DSD is similar to conventional 2-level and 3-level buck converters [6] with the only difference in the factor of two in the resonant frequency (f_0 expression provided in Fig. 2) and quality factor expressions.

III. SMALL-SIGNAL EFFECTS OF PARASITICS FOR DSD

A. Effects of On-Resistances of Power Switches

The effects of on-resistances of the power transistors, R_{on}, are analyzed in this section assuming all the resistances of the switches are equal, that is $R_{SH1} = R_{SL1} = R_{SH2} = R_{SL2} = R_{on}$. They also affect the efficiency of the converter and the steady-state DC values as shown in Table II with the important results highlighted. As high-ratio conversion, i.e. 48V-to-1V is being used in this work, the duty cycle, D, is at least an order of magnitude smaller than 1 (25X less for $D = 4\%$), hence $D \ll 1$ is a valid assumption. Besides, D is limited to 50% for DSD. Please note that the $D \ll 1$ assumption is only used for DSD, while not being used for other topologies in Section IV.

The results in Table II also show that the DC component of each state variable and the output variables are dependent on the ratio of R_{on} to the load resistance, R. Hence, even a larger D would result in negligible effect on V_{CF} due to $R \gg R_{on}$ being generally true for PoL converters. In addition, the V_{CF} also deviates only negligibly with the R_{on} and remains at half the supply voltage, V_g, as required for the proper operation of the converter even for larger D due to DR_{on} being practically small, as illustrated in Table II. This is also evident from the almost-zero sensitivity of V_{CF} with respect to R_{on}, given by

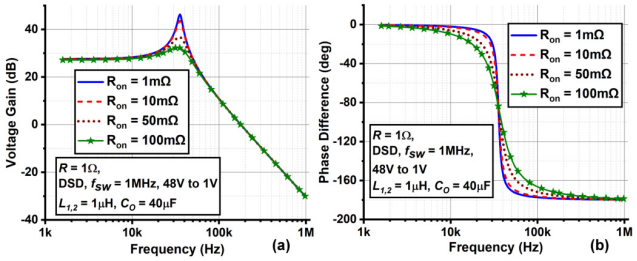


Fig. 3. Frequency response of the transfer functions of DSD derived using state-space averaging with (a) magnitude response, and (b) phase response when considering only R_{on}.

$S^{V_{CF}}_{R_{on}}$ (Table II). The DC (or average) values of the two inductor currents, I_{L1} and I_{L2}, are simply half of the output current I_O, while output capacitor voltage, V_C, and output voltage of the converter, V_O, are equal in this case as series resistance of the output capacitor, R_{CO}, is ignored. The DC input current, I_{in}, is the same as DI_{L1} due to the fact that I_{in} only flows in state I of the operation. The DC parameters obtained can also used to derive the efficiency, $\eta_{SSA|Ron}$, using the expressions for V_O and I_{in}. The efficiency results are further verified by the efficiency expression, η, with the assumption of the symmetry between the two inductors, i.e., $I_{L1} = I_{L2}$, and computing the conduction loss of each switch (Table II). As for the state variables, efficiency is only weakly related to the duty cycle of the converter.

The frequency response with different R_{on} values at fixed loading conditions is shown in Fig. 3. The values of R_{on} within 10mΩ depict the typical case of discrete devices, whereas integrated power switches will have relatively higher R_{on} depending on the cost-efficiency-density trade-offs. Thus, both higher and lower R_{on} are used in the analysis. The DC gain of the transfer function in this case, $T(0)_{Ron}$, has the same dependence on R_{on} as that of state variables and efficiency, therefore it can also be written in terms of the efficiency of the converter (Table II).

B. Effects of Flying Capacitor's Series Resistance

When considering only the equivalent series resistance (ESR) of the flying capacitor, R_{CF}, it has little impact on the DC operating point parameters because the state variables, output variables and the efficiency depend on DR_{CF} (Table II) where D is very small along with the fact that current flows

TABLE III

DSD DC OPERATING POINTS FOR DCR OF INDUCTORS

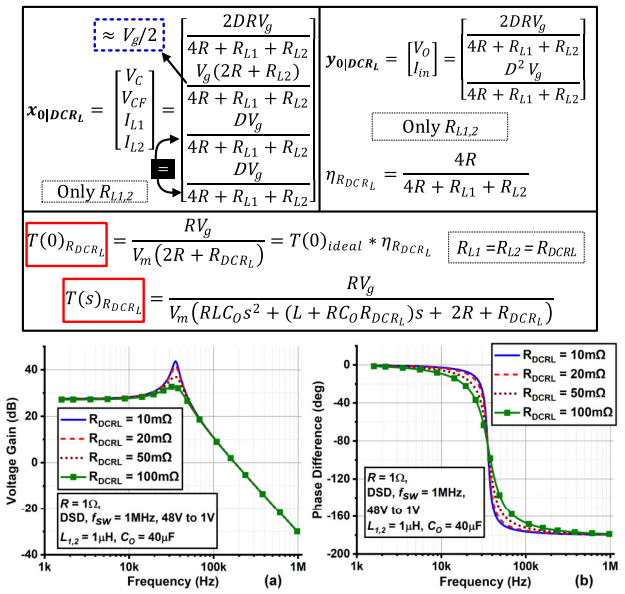


Fig. 4. Frequency response of the transfer functions of DSD derived using state-space averaging with (a) magnitude response, and (b) phase response when considering only R_{DCRL} of inductors.

through R_{CF} only during states I and III, both of which have a duration of only 4% of the switching period as D is only 4% for 48V-to-1V. For the same reason, R_{CF} does not have a noticeable impact on the frequency response of the transfer function in this case, $T(s)_{RCF}$. The DC gain of the transfer function in this case depends on the square of the efficiency, η_{RCF}, which further corroborates its weak dependence on R_{CF}.

C. Effects of DC Resistance of Each Inductor

When considering only the series resistance (DCR) of each inductor, R_{L1} and R_{L2}, the DC state variables, the output variables and the efficiency, η_{DCRL}, depend on the value of each resistance without the scaling factor D being multiplied to the resistances owing to the fact that the DCR of each inductor conducts throughout the switching period of the converter.

The results for this case are shown in Table III where the DCR of each inductor is considered separately to emphasize the effect of each resistance on each variable. Each of these resistances contribute equally to determining the DC values of all the variables except V_{CF}, where R_{L2} seems to contribute more. However, a careful look at the results shows that it does not cause deviation in the V_{CF} to a significant extent. For instance, a worst-case scenario with the unity ratio of DCR to R (R = 50mΩ for 50A loading current with 1V output resulting in 80% efficiency). For this case, if R_{L2} is assumed to be 10% larger than R_{L1}, V_{CF} deviates from the required $V_g/2$ steady-state DC value by <2% only. Moreover, the intrinsic current balancing of DSD [1], [14] is also proved here in Table III, as I_{L1} and I_{L2} are the same despite the mismatches between the DCR of the two inductors.

On the other hand, steady-state V_{CF} equals to $V_g/2$ if both R_{L1} and R_{L2} are the same, i.e., $R_{L1} = R_{L2} = R_{DCRL}$. The transfer function in this case, $T(s)_{RDCRL}$, can also be expressed in terms of the efficiency as shown in Table III. The frequency

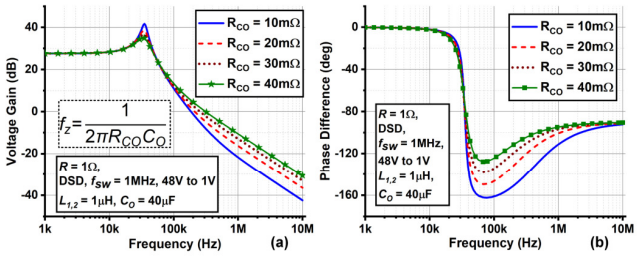


Fig. 5. Frequency response of the transfer functions of DSD derived using state-space averaging with (a) magnitude response, and (b) phase response when considering only R_{CO}.

TABLE IV

DSD DC OPERATION POINTS FOR ESR OF C_O

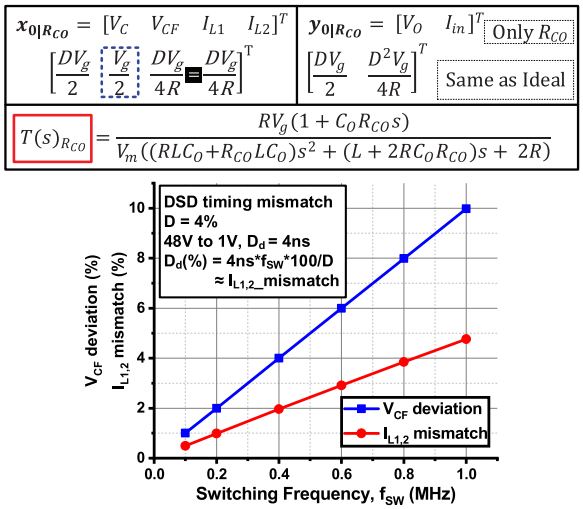


Fig. 6. DSD high-side and low-side timing mismatch effects on steady-state V_{CF} deviation and inductor-current mismatch compared to nominal values (D_d = 0) at different switching frequencies.

response of this transfer function is given in Fig. 4 for various values of DCR with higher values indicating higher inductance required in case of low-frequency operation of the converter. This frequency response also shows that the low-frequency gain and the locations of pole/zero are not disturbed by the DCR greatly, but only Q is reduced due to increased loss in every switching cycle.

D. Effects of Series Resistance of Output Capacitor

As shown in Table IV, the ESR of the output capacitor, R_{CO}, does not cause any changes in the DC values of any of the variables in the state-space model because it is not in the main current path. Upon computing the transfer function, $T(s)_{RCO}$, for this case, it is seen that the R_{CO} adds a zero to the system (Fig. 5), which is similar to traditional buck converters. Besides, R_{CO} is typically smaller due to minimum voltage ripples and droops during load transient requirements of PoL converters.

E. Effects of High and Low Side Timing Mismatch

There are two pairs of complementary high and low side switches in DSD. The PWM gate signals for each pair are generated using comparators with clocks, analog ramps, and digital logics, which can result in timing mismatches between the gate signals of each pair. At high conversion ratios i.e. very

TABLE V
DSD DC OPERATION POINT FOR TIMING MISMATCH

$\boldsymbol{x_{0\|D_d}} = [V_C \quad V_{CF} \quad I_{L1} \quad I_{L2}]^T$ $\left[\frac{DV_g(D+D_d)}{2D+D_d} \quad \frac{DV_g}{2D+D_d} \quad \frac{DV_g(D+D_d)^2}{R(2D+D_d)^2} \quad \frac{D^2V_g(D+D_d)}{R(2D+D_d)^2}\right]^T$
$\boldsymbol{y_{0\|D_d}} = [V_O \quad I_{in}]^T = \left[\frac{DV_g(D+D_d)}{2D+D_d} \quad \frac{D^2V_g(D+D_d)^2}{R(2D+D_d)^2}\right]^T$
$S_{D_d}^{V_{CF}} = \frac{\partial V_{CF}}{\partial D_d}\cdot\frac{D_d}{V_{CF}} = \frac{-DV_g}{(2D+D_d)^2}\cdot\frac{D_d}{V_{CF}} = \frac{-D_d}{2D+D_d} \approx \frac{-D_d}{2D}$

small duty cycle, the on-time mismatch, D_d, usually becomes important. For example, for 1MHz switching frequency, a 4% DSD duty cycle for 48V-to-1V conversion and a 2.5% mismatch would mean 1-ns of time. For conventional buck and 3-level topologies, this duty cycle is only 2%, where mismatch can be relatively more important. However, the 2X duty cycle in DSD for the same conversion ratio reduces the timing mismatch effects compared to other topologies. In addition, higher frequency operation that poses challenges in minimizing the timing mismatch as shown by V_{CF} deviation and $I_{L1,2}$ mismatch effects in Fig. 6, may not be feasible due to high step-down ratio and high-current nature of PoL converters, resulting in high switching loss. The results for this case are summarized in Table V indicating that output voltage and V_{CF} do not vary to a large extent because timing mismatch, with proper layout, can usually be at least an order of magnitude smaller than the on-time of the high side transistors. The sensitivity of V_{CF} with respect to D_d, provided in Table V as $S_{D_d}^{V_{CF}}$, also gives the same insight of almost negligible effects of timing mismatch on V_{CF}, given that $D \gg D_d$. Same is the case for inductor currents where expressions appear to be different, but $D \gg D_d$ simplification results in the same expressions for both currents. Considering worst-case scenario of D_d to be 10% of D, i.e., 4ns, causes V_{CF} to change by <5% only, while I_{L1} and I_{L2} differ by ~8%. Careful layout of both devices and signal routing can, however, avoid such extreme situations. Yet, the mismatch effect is negligible compared to 3-level where such mismatches can cause V_{CF} to reach either 0V or V_g [22]. In addition, the DC value of the transfer function is also not affected by timing mismatches to a noticeable extent, and the impact on small-signal behavior is also negligible in presence of parasitic capacitances. The implementation of DSD using discrete components would, however, require careful design constraints such as matched routing.

F. Measurement Results

To verify the theoretical results of DSD state-space averaging model, a printed circuit board (PCB), shown in Fig. 8, is designed using the components from Table VI with GaN transistors; and a small-signal AC perturbation at a given frequency is applied to the duty cycle, also shown in Fig. 8, then the frequency spectrum of the output voltage, V_O, at that frequency is recorded to extract the magnitude and phase information. The $A_{cmp}(s)$ in (9) is set to unity, while V_m is set to 2V for these measurements. The magnitude responses Fig. 8 (a-c) and phase responses Fig. 8 (d-f) are provided for 48V to 1V/1A, 36V to 1.8V/1A and 24V to 1.2V/1A, respectively. These results are plotted with Cadence PXF simulations, under

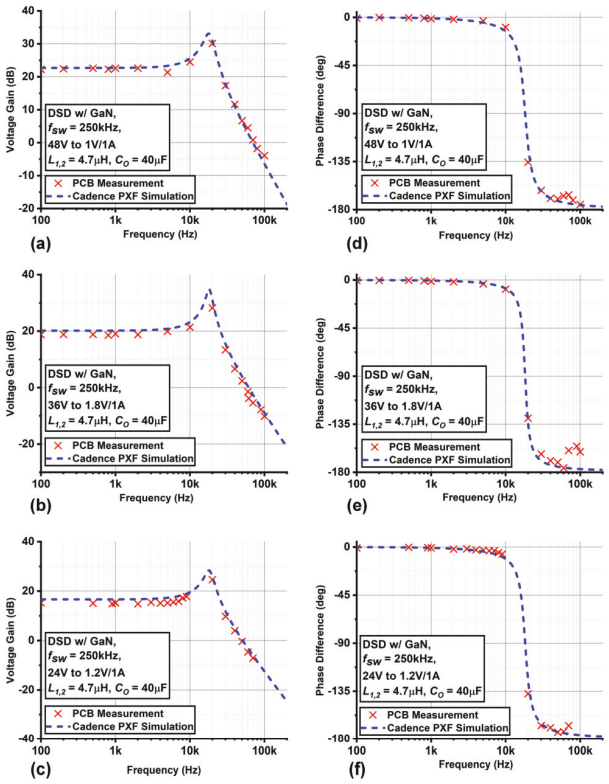


Fig. 7. Frequency response of DSD from the PCB measurements and Cadence PXF analysis simulations for different operating conditions with (a-c) magnitude response, and (d-f) phase response.

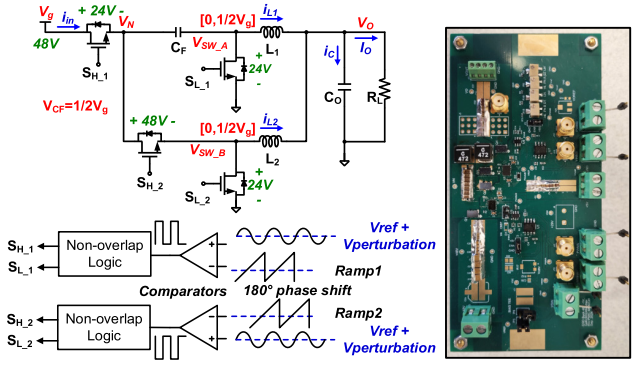


Fig. 8. DSD measurement (left) setup for small-signal perturbation and (right) PCB for control-to-output transfer function.

the same conditions and using the same GaN device models in the power stage, that shows the close agreement of simulation, as well as theoretical results from Fig. 2, and measurement results; thereby justifying the efficacy of the derived SSA model, despite having additional parasitics and sources of timing mismatches of the measurement setup.

IV. GENERALIZED MATRIX INVERTIBILITY PRINCIPLE

In Sections II & III, the traditional SSA is applied to the DSD topology which comprises two inductors and only one flying capacitor. This section extends the derivation of steady-state parameters to generalize the principle of matrix invertibility to well-known topologies with different numbers of inductors, flying capacitors and numbers of phases than DSD, but without including parasitics (ideal model) which makes V_C and V_O the same for all cases. The ideal SSA

TABLE VI

RELEVANT COMPONENTS USED FOR DSD PCB DESIGN

Component	Part Number	Specifications
Switches $S_{H\_1,2}$, $S_{L\_1,2}$	EPC EPC2031	60V, 2.6mΩ, 48A
Gate drivers	Texas Instruments LMG1210RVRT	200V half-bridge GaN FET driver
Comparators	Analog Devices LT1720CS8#PBF	Dual, 4.5ns, Rail-to-Rail
Flying capacitor, C_F	Murata GRM31CR71H475KA12L	4 x 4.7µF, 1206 X7R (50V)
Bootstrap capacitors	TDK YFF18PW0J474MT0H0N	0.47µF, 0603 (6.3V), 3-terminal
Bootstrap diodes	Nexperia BAT46WJ,115	100V, 250mA, Schottky
Output capacitors, C_O	Murata LLL1U4R60G435ME22D	3 x 4.3µF, 0204 X5R (4V)
Inductors, $L_{1,2}$	Coilcraft XGL6060-472MEC	4.7µH, 10.1mΩ max.

TABLE VII

IDEAL DSD STATE-SPACE AVERAGING MATRICES

$$A=\begin{bmatrix} -\frac{1}{RC_O} & 0 & \frac{1}{C_O} & \frac{1}{C_O} \\ 0 & -2K & \frac{D}{C_F} & -\frac{D}{C_F} \\ -\frac{1}{L_1} & -\frac{D}{L_1} & 0 & 0 \\ -\frac{1}{L_2} & \frac{D}{L_2} & 0 & 0 \end{bmatrix} \quad B=\begin{bmatrix} 0 \\ K \\ D \\ \frac{}{L_1} \\ 0 \end{bmatrix}$$

V_{CF} balancer ⇒ $K \neq 0$

$K=0 \Rightarrow |A| \neq 0$ (A invertible inherently), V_{CF} & $I_{L1,2}$ inherently balanced

Redundant K ⇒ same solution

$$x_0 = [V_C \quad V_{CF} \quad I_{L1} \quad I_{L2}]^T = \left[\frac{DV_g}{2} \quad \frac{V_g}{2} \quad \frac{DV_g}{4R} \quad \frac{DV_g}{4R}\right]^T$$

matrices are modified using the proposed convergence enhancement to derive the DC operating points, allowing derivation of the control-to-output transfer functions. The ideal SSA matrices and DC operating points for DSD are provided in Table VII as a reference of comparison, where K is an arbitrary constant given by:

$$\frac{\Delta V_{CF}}{\Delta t} = -2K\left(V_{CF} - \frac{V_g}{2}\right) = K(V_g - 2V_{CF}), \qquad (10)$$

where $V_g/2$ is the reference voltage determined from the volt-second balance, and time period, T_S, term is absorbed into the constant K. The addition of the constant, however, does not change the solution for DSD due to matrix A being inherently full-rank, thereby adding no more constraints to the system of equations i.e. the constant is redundant in this case. As DC operating point computation only requires matrices A and B, other matrices in the SSA model are not included in this section. The correctness of the DC operating point solution is confirmed using steady-state analysis of the converter utilizing standard volt-second and amp-second balance equations. For example, the voltage-conversion ratio is given by V_C/V_g in x_0 in Table VII for DSD. Several hybrid buck topologies are also analyzed in this section where conventional SSA model needs to be modified to get the correct and unique DC operation points.

A. 3-Level Buck, One Inductor & One Flying Cap., 4-Phase

The SSA model of 3-level buck converter (Fig. 9) can be derived from the inductor-current and capacitor-voltage

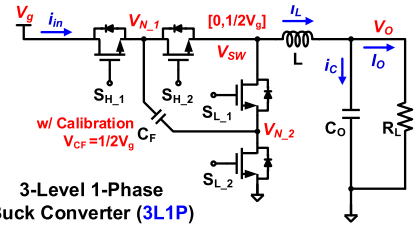


Fig. 9. 3-Level buck converter topology.

TABLE VIII

3-LEVEL STATE-SPACE AVERAGING MATRICES

$$A=\begin{bmatrix} -\frac{1}{RC_O} & 0 & \frac{1}{C_O} \\ 0 & -2K & 0 \\ -\frac{1}{L} & 0 & 0 \end{bmatrix} \quad B=\begin{bmatrix} 0 \\ K \\ D \\ \frac{}{L} \end{bmatrix}$$

$K=0 \Rightarrow |A|=0$ (A not invertible)

V_{CF} calibration required ⇒ $a_{2,2} \neq 0$

$$x_0 = [V_C \quad V_{CF} \quad I_L]^T = \left[DV_g \quad \frac{V_g}{2} \quad \frac{DV_g}{R}\right]^T$$

equations for each phase of the switching cycle. There are four phases of operation for 3-level [6] that gives four sets of equations, hence four matrices similar to the ones derived for DSD in Section II, with each set comprising the following:

$$\frac{dV_o}{dt} = \frac{i_c}{C_o} = \frac{i_L}{C_o} - \frac{V_o}{RC_o}, \qquad (11)$$

$$\frac{dV_{CF}}{dt} = \frac{i_{CF}}{C_F}, \qquad (12)$$

$$\frac{di_L}{dt} = \frac{V_L}{L}. \qquad (13)$$

The SSA matrices can then be derived by averaging using (1). The computation of DC operating point requires only matrices A and B using (2) with the result provided in Table VII. The arbitrary proportionality constant, K, is added to (12) using (10) to incorporate the effects of V_{CF} balancing circuitry by adjusting V_{CF} each cycle towards a set reference voltage, using any balancing method in general such as adjusting the on-time of charging and discharging phases.

In case $K = 0$, the inverse of matrix A doesn't exist due to its determinant being zero, hence indicating the necessity of V_{CF} balancer during operation corroborating the well-known requirement of V_{CF} balancer in a 3-level converter. In other words, rank-deficient matrix A becomes full-rank with the addition of the constant. Intuitively, if a state variable appears in multiple phases with same magnitude but opposite signs, then it gets canceled out upon averaging, resulting in a zero row and/or column. For instance, the same charging/discharging currents of C_F, which is often the case for single-inductor topologies, could result in such a situation. The position of the required constant, K, can also be determined intuitively by observing that a non-zero element at the intersection of a zero row and a zero column, $a_{2,2}$ in Table VIII, makes matrix A invertible. This position also denotes the relation given in (10).

It can be noted that with the addition of the constant K, the solution converges to a unique and correct DC solution; and that the final DC operating point is independent of K, thus the actual value of K doesn't affect the final solution. It is also interesting to note that the matrix A used for invertibility test is computed for an ideal case, therefore complexity of the

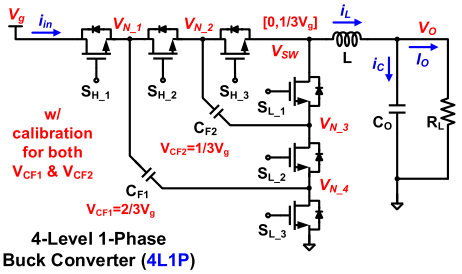


Fig. 10. 4-Level buck converter topology.

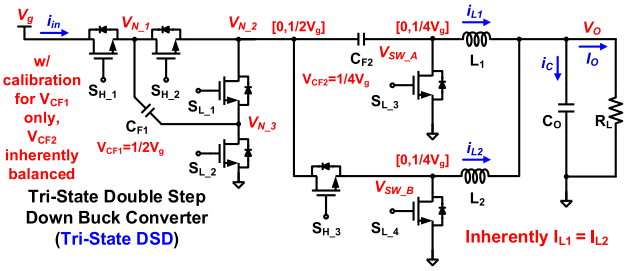


Fig. 11. Tri-State DSD buck converter topology.

TABLE IX
4-LEVEL STATE-SPACE AVERAGING MATRICES

$$A = \begin{bmatrix} -\frac{1}{RC_O} & 0 & 0 & \frac{1}{C_O} \\ 0 & K_1 & 0 & 0 \\ 0 & 0 & K_2 & 0 \\ -\frac{1}{L} & 0 & 0 & 0 \end{bmatrix} \quad B = \begin{bmatrix} 0 \\ -\frac{2K_1}{3} \\ -\frac{K_2}{3} \\ \frac{D}{L} \end{bmatrix}$$

$K_{1,2}=0 \Rightarrow |A|=0$ (A not invertible), $V_{CF1,2}$ require calibration

V_{CF} calibration $\Rightarrow a_{2,2}\neq 0, a_{3,3}\neq 0$

$$x_0 = [V_C \quad V_{CF1} \quad V_{CF2} \quad I_L]^T = \left[DV_g \quad \frac{2V_g}{3} \quad \frac{V_g}{3} \quad \frac{DV_g}{R}\right]^T$$

TABLE X
TRI-STATE-DSD STATE-SPACE AVERAGING MATRICES

$$A = \begin{bmatrix} -\frac{1}{RC_O} & 0 & 0 & \frac{1}{C_O} & \frac{1}{C_O} \\ 0 & K_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{2D}{C_{F2}} & -\frac{2D}{C_{F2}} \\ -\frac{1}{L_1} & 0 & -\frac{2D}{L_1} & 0 & 0 \\ -\frac{1}{L_2} & 0 & \frac{2D}{L_2} & 0 & 0 \end{bmatrix} \quad B = \begin{bmatrix} 0 \\ -\frac{K_1}{2} \\ 0 \\ \frac{D}{L_1} \\ 0 \end{bmatrix}$$

V_{CF1} calibration $\Rightarrow a_{2,2}\neq 0$

$K_1=0 \Rightarrow |A|=0$ (A not invertible), V_{CF1} requires balancing, V_{CF2} inherently balanced

Inherent I_L balance: $I_{L1}=I_{L2}$

$$x_0 = [V_C \quad V_{CF1} \quad V_{CF2} \quad I_{L_1} \quad I_{L_2}]^T = \left[DV_g \quad \frac{V_g}{2} \quad \frac{V_g}{4} \quad \frac{DV_g}{4R} \quad \frac{DV_g}{4R}\right]^T$$

model due to the addition of parasitics, similar to that shown for DSD in Section III, is greatly simplified.

B. 4-Level Buck, One Inductor & Two Flying Caps., 6-Phase

The SSA model of a 4-level converter (Fig. 10) [23], another FCML topology similar to 3-level, can be derived in a similar manner. In this case, there are four storage elements, hence four state variables in the SSA model as shown in Table IX. This topology has six phases of operation with the defining equations as follows:

$$\frac{dV_{CF1}}{dt} = \frac{i_{CF1}}{C_{F1}}, \tag{14}$$

$$\frac{dV_{CF2}}{dt} = \frac{i_{CF2}}{C_{F2}}, \tag{15}$$

$$\frac{di_L}{dt} = \frac{V_L}{L}, \tag{16}$$

where $V_{CF1,2}$ ($i_{CF1,2}$) are the voltages (currents) of the two flying capacitors, namely C_{F1} and C_{F2}, respectively. The output capacitor voltage expression is the same as (10) for all the phases. The averaging of each matrix for this topology can be achieved as follows:

$$M = d\,(M_1 + M_2 + M_3) + (1 - 3d)(M_4), \tag{17}$$

where $M_{1,2,3}$ correspond to the inductor-charging, whereas $M_4 = M_5 = M_6$ correspond to the inductor-discharging phases. As matrix A for this topology is also not invertible originally, it can be made invertible using two arbitrary constants, K_1 and K_2, which can be added to (14) and (15) for the two flying capacitors, C_{F1} and C_{F2}, respectively, as follows:

$$\frac{\Delta V_{CF1}}{\Delta t} = K_1\left(V_{CF1} - \frac{2V_g}{3}\right), \tag{18}$$

$$\frac{\Delta V_{CF2}}{\Delta t} = K_2\left(V_{CF2} - \frac{V_g}{3}\right). \tag{19}$$

The two reference voltages in this case are $2V_g/3$ and $V_g/3$ for V_{CF1} and V_{CF2}, respectively. As a result, a unique and correct DC solution is achieved as shown in Table IX. In the absence of either of the two constants, matrix A is not invertible, hence it's essential to have V_{CF} balancer for both of the flying capacitors for this topology according to the proposed invertibility principle. This result also corroborates the well-known requisite of 4-level topology for proper operation i.e. V_{CF} balancing circuitry for both flying capacitors, again without including the complexity of parasitics in the SSA model.

C. Tri-State DSD, Two Inductors & Two Flying Caps., 8-Phase

The SSA model of a Tri-State DSD [24], shown in Fig. 11 as a cascaded version of the 3-level converter and the DSD, has five state variables due to the topology having five storage elements (Table X). For this topology, flying capacitor C_{F2} corresponds to DSD stage, hence it is inherently balanced to $V_g/4$. However, C_{F1} corresponds to the 3-level stage and requires V_{CF} balancer [24]. Matrix A for this topology is also singular originally (without adding any constants), for this reason an arbitrary constant, K_1, is added to eliminate a row/column of zeros, thereby making its determinant non-zero as shown in Table X. The defining equations for each of the eight phases are given as follows:

$$\frac{dV_o}{dt} = \frac{i_c}{C_o} = \frac{i_{L1} + i_{L2}}{C_o} - \frac{V_o}{RC_o}, \tag{20}$$

$$\frac{dV_{CF1}}{dt} = \frac{i_{CF1}}{C_{F1}}, \tag{21}$$

$$\frac{dV_{CF2}}{dt} = \frac{i_{CF2}}{C_{F2}}, \tag{22}$$

$$\frac{di_{L1}}{dt} = \frac{V_{L1}}{L_1}, \tag{23}$$

$$\frac{di_{L2}}{dt} = \frac{V_{L2}}{L_2}. \tag{24}$$

Averaging the matrices for eight phases gives the following expression:

$$M = d\,(M_1 + M_3 + M_5 + M_7) + (1 - 4d)(M_2), \tag{25}$$

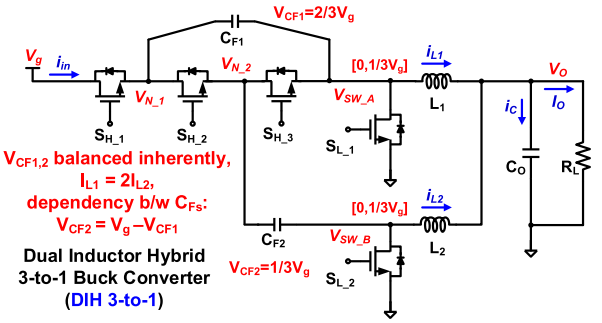


Fig. 12. Dual inductor hybrid 3-to-1 buck converter topology.

TABLE XI

DIH-3-TO-1 STATE-SPACE AVERAGING MATRICES

$$A=\begin{bmatrix} -\frac{1}{RC_O} & 0 & 0 & \frac{1}{C_O} & \frac{1}{C_O} \\ 0 & 0 & 0 & \frac{D}{2C_{F1}} & -\frac{D}{C_{F1}} \\ 0 & -K_1 & -K_1 & -\frac{D}{2C_{F2}} & \frac{D}{C_{F2}} \\ -\frac{1}{L_1} & -\frac{D}{L_1} & 0 & 0 & 0 \\ -\frac{1}{L_2} & \frac{D}{L_2} & -\frac{D}{L_2} & 0 & 0 \end{bmatrix} \quad B=\begin{bmatrix} 0 & 0 & K_1 & \frac{D}{L_1} & 0 \end{bmatrix}^T$$

$$A_{RREF}=\begin{bmatrix} 1 & 0 & 0 & 0 & -3R \\ 0 & 1 & 0 & 0 & \frac{3R}{D} \\ 0 & 0 & 1 & 0 & \frac{6R}{D} \\ 0 & 0 & 0 & 1 & -2 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

K_1=0

Rank(A)=4

$V_{CF2}=V_g-V_{CF1}$

$$x_0=[V_C \quad V_{CF1} \quad V_{CF2} \quad I_{L_1} \quad I_{L_2}]^T \Downarrow = \left[\frac{DV_g}{3} \quad \frac{2V_g}{3} \quad \frac{V_g}{3} \quad \frac{2DV_g}{9R} \quad \frac{DV_g}{9R}\right]^T$$

$K_1 \neq 0$

Rank(A)=4 ⇒ $|A|$=0 (A not invertible) ⇒ need one more constraint
⇒ add dependencies ⇒ A full rank ⇒ Inherently balanced

where $M_{1,3,5,7}$ correspond to the inductor-charging phases, while $M_2 = M_4 = M_6 = M_8$ correspond to the inductor-discharging phases. A term containing the constant K_1 is then added to (19) using:

$$\frac{\Delta V_{CF1}}{\Delta t} = K_1\left(V_{CF1} - \frac{V_g}{2}\right), \tag{26}$$

where $V_g/2$ is the reference voltage. As before, the ideal model with proposed invertibility principle predicts C_{F1} to require balancing, and C_{F2} to be inherently balanced, while achieving the correct and unique DC solution of all state variables. In addition, the analysis of Tri-State DSD also proves the proposed principle for a model with a combination of intrinsically balanced and intrinsically unbalanced capacitors.

D. DIH 3-to-1 Buck, Two Inds. & Two Flying Caps., 4-Phase

The DIH topology with 3-to−1 switched-capacitor stage (Fig. 12) [17] has the same number of storage elements as that of Tri-State DSD with different numbers of phases of operation though. In addition, the voltage-conversion ratio expression, given by V_C/V_g from Table XI, is different than Tri-State DSD and the two inductor currents are not the same for this topology. Apart from these differences, what makes it a special case to look at is the observation that matrix A, given in Table XI, does not have any rows or columns of zeros as was the case with earlier topologies. However, the determinant of matrix A is still zero, because looking at the reduced-row-echelon form of matrix A (A_{RREF}), the matrix is rank-deficient. On the contrary, this topology is well-known (and from steady-state analysis) to have inherent flying capacitor balance [17] that makes it look like a discrepancy at first because matrix A is supposed to be invertible. However, a careful look at the SSA model reveals the limitation of the traditional derivation which is incomplete without including the charge sharing or dependency between the two flying capacitors i.e. $V_{CF2} = V_g -$

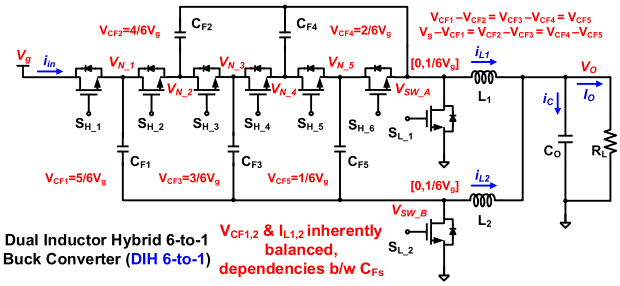


Fig. 13. Dual inductor hybrid 6-to-1 buck converter topology.

TABLE XII

DIH-6-TO-1 STATE-SPACE AVERAGING MATRICES

$$A=\begin{bmatrix} -\frac{1}{RC_O} & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_O} & \frac{1}{C_O} \\ 0 & K_1 & -K_1 & 0 & 0 & -K_1 & -\frac{D}{3C_{F1}} & \frac{D}{3C_{F1}} \\ 0 & 0 & K_2 & -K_2 & 0 & -K_2 & \frac{D}{3C_{F2}} & -\frac{D}{3C_{F2}} \\ 0 & 0 & 0 & K_3 & -K_3 & -K_3 & -\frac{D}{3C_{F3}} & \frac{D}{3C_{F3}} \\ 0 & 0 & 0 & 0 & K_4 & -2K_4 & \frac{D}{3C_{F4}} & -\frac{D}{3C_{F4}} \\ 0 & -K_5 & 0 & 0 & 0 & -K_5 & -\frac{D}{3C_{F5}} & \frac{D}{3C_{F5}} \\ -\frac{1}{L_1} & \frac{D}{L_1} & -\frac{D}{L_1} & 0 & 0 & 0 & 0 & 0 \\ -\frac{1}{L_2} & -\frac{D}{L_2} & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$B=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & K_5 & 0 & \frac{D}{L_2} \end{bmatrix}^T$$

$K_{1\sim5}$=0 ⇒ $|A|$=0
(A not invertible, incorrect! w/ C_{Fs} dependencies ignored)

$$x_0=[V_C \quad V_{CF1} \quad V_{CF2} \quad V_{CF3} \quad V_{CF4} \quad V_{CF5} \quad I_{L_1} \quad I_{L_2}]^T \quad K_{1\sim5}\neq 0$$

$$= \left[\frac{DV_g}{6} \quad \frac{5V_g}{6} \quad \frac{2V_g}{3} \quad \frac{V_g}{2} \quad \frac{V_g}{3} \quad \frac{V_g}{6} \quad \frac{DV_g}{12R} \quad \frac{DV_g}{12R}\right]^T$$

Correct w/ dependencies

Rank(A)=4 ⇒ $|A|$=0 (A not invertible) ⇒ need 4 more constraints
⇒ add dependencies ⇒ A full rank ⇒ Inherently balanced
K_1=0 OR K_5=0 ⇒ Rank(A)=8 ⇒ One redundant dependency ⇒ Same solution

V_{CF1}. This dependency can be incorporated into the model in a similar way as V_{CF} balancer is added for other topologies using an arbitrary constant K_1 as follows:

$$\frac{\Delta V_{CF2}}{\Delta t} = K_1(V_g - V_{CF1} - V_{CF2}), \tag{27}$$

whereby it gives a unique and correct DC solution from the modified (and complete) SSA model once again without even taking the parasitics into account. The governing equations for the SSA model of this topology can be written in the same way as Tri-State DSD with only difference in the averaging expression, which is similar to that of DSD, thus given by (1). The analysis of this DIH topology also reveals that the improved (inclusive of dependency behavior) SSA model with proposed matrix invertibility principle is also applicable to the topologies where the two inductor currents are not the same.

E. DIH 6-to-1 Buck, Two Inds. & Five Flying Caps., 4-Phase

An extension to the previous special case of DIH converter, with more flying capacitors and more dependencies among them, is DIH 6-to−1 topology (Fig. 13) [18]. This topology has eight storage elements, hence eight state variables (Table XII). The governing equation for each of the eight storage elements can be written for each of the four phases using aforementioned principle and then the averaging of matrices for this topology is also given by (1) due to the same

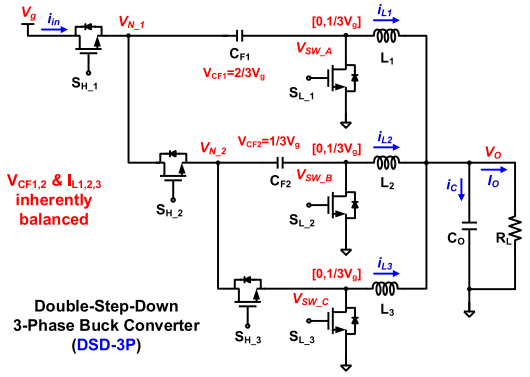


Fig. 14. DSD 3-phase buck converter topology.

TABLE XIII

DSD-3-PHASE STATE-SPACE AVERAGING MATRICES

$$A=\begin{bmatrix} -\frac{1}{RC_O} & 0 & 0 & \frac{1}{C_O} & \frac{1}{C_O} & \frac{1}{C_O} \\ 0 & K_1 & 0 & \frac{D}{C_{F1}} & -\frac{D}{C_{F1}} & 0 \\ 0 & 0 & K_2 & 0 & \frac{D}{C_{F2}} & -\frac{D}{C_{F2}} \\ -\frac{1}{L_1} & -\frac{D}{L_1} & 0 & 0 & 0 & 0 \\ -\frac{1}{L_2} & \frac{D}{L_2} & -\frac{D}{L_2} & 0 & 0 & 0 \\ -\frac{1}{L_3} & 0 & \frac{D}{L_3} & 0 & 0 & 0 \end{bmatrix} \quad B=\begin{bmatrix} 0 \\ -\frac{2K_1}{3} \\ -\frac{K_2}{3} \\ \frac{D}{L_1} \\ 0 \\ 0 \end{bmatrix}$$

$V_{CF1,2}$ balancer $\Rightarrow K_{1,2}\neq 0$

$K_{1,2}=0 \Rightarrow |A|\neq 0$ (A invertible inherently), V_{CFs} inherently balanced, $I_{L1}=I_{L2}=I_{L3}$

Redundant $K_{1,2}$ $\Downarrow$ Same solution w/ $K_{1,2}=0$ and $K_{1,2}\neq 0$

$$x_0=[V_C \quad V_{CF1} \quad V_{CF2} \quad I_{L1} \quad I_{L2} \quad I_{L3}]^T=\left[\frac{DV_g}{3} \quad \frac{2V_g}{3} \quad \frac{V_g}{3} \quad \frac{DV_g}{9R} \quad \frac{DV_g}{9R} \quad \frac{DV_g}{9R}\right]^T$$

numbers of phases as DSD. Again, the traditional SSA model is incomplete and has multiple columns of zeros in matrix A without any modifications (constants $K_{1\sim5}=0$ in Table XII) indicating a discrepancy from the actual behavior [18] where all the flying capacitors are inherently balanced. Modifying the traditional SSA model by adding five arbitrary constants, $K_{1\sim5}$, considering the inherent dependencies between all the flying capacitors, shown in Fig. 13, in the following way makes matrix A invertible, thereby resulting in the correct and unique DC solution provided in Table XII.

$$\frac{\Delta V_{CF1}}{\Delta t}=K_1(V_{CF1}-V_{CF2}-V_{CF5}), \tag{28}$$

$$\frac{\Delta V_{CF2}}{\Delta t}=K_2(V_{CF2}-V_{CF3}-V_{CF5}), \tag{29}$$

$$\frac{\Delta V_{CF3}}{\Delta t}=K_3(V_{CF3}-V_{CF4}-V_{CF5}), \tag{30}$$

$$\frac{\Delta V_{CF4}}{\Delta t}=K_4(V_{CF4}-2V_{CF5}), \tag{31}$$

$$\frac{\Delta V_{CF5}}{\Delta t}=K_5(V_g-V_{CF1}-V_{CF5}). \tag{32}$$

The DC operating point, in this case too, agrees with the conversion ratio, flying capacitor voltages and inductor currents as derived from the steady-state analysis [18]. Moreover, one redundant dependency does not affect the final solution, similar to what was observed for DSD.

F. DSD-3-Phase, Three Inductors & Two Flying Caps., 6-Phase

Another topology of interest analysis is the DSD−3-phase (Fig. 14) [12] with three inductor-charging and three inductor-discharging phases, resulting in a total of six phases of operation. This topology has an additional inductor than DSD

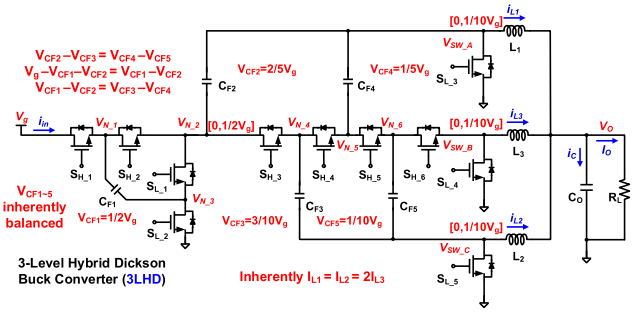


Fig. 15. 3-level hybrid dickson buck converter topology.

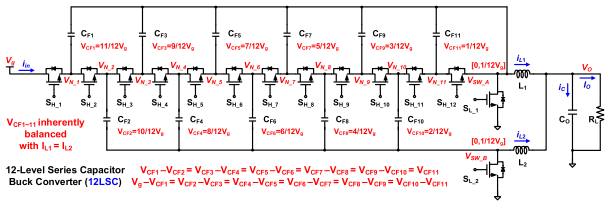


Fig. 16. 12-level series capacitor hybrid buck converter topology.

which is of interest to generalize the matrix invertibility principle where state variables include more numbers of inductors than flying capacitors. The governing equation for each storage element remains the same as other topologies, however, the averaging expression for each of the SSA matrices changes as follows:

$$M=d\,(M_1+M_3+M_5)+(1-3d)(M_2), \tag{33}$$

where $M_{1,3,5}$ correspond to the inductor-charging phases, while $M_2=M_4=M_6$ correspond to the inductor-discharging phases. Although state variables are more in number for this topology compared to DSD, but comparable to some of the above-mentioned topologies, it can be seen that the SSA model with both the traditional ($K_{1,2}=0$ in Table XIII) and enhanced ($K_{1,2}\neq 0$) methodology predict, with proposed invertibility principle, that both the V_{CF1} and V_{CF2} are balanced due to matrix A being inherently invertible as it converges to the correct and unique DC solution where all three inductor currents are the same and the voltage-conversion ratio is $D/3$ as determined from the steady-state analysis of the converter. This topology also serves as an example where redundant constants are added but the final solution remains the same.

G. 3-Level Hybrid Dickson, Three Inds. & Five C_{Flys}, 12-Phase

Besides DSD−3-phase, another topology that requires three inductors and five flying capacitors along with having dependencies between the flying capacitors is 3-level hybrid Dickson topology (3LHD) [25]. The 3LHD topology (Fig. 15) consists of a 3-level stage followed by a 5-to−1 hybrid Dickson stage with six inductor-charging and six inductor-discharging phases, resulting in a total of twelve phases of operation. The governing equation for each storage element remains the same as other topologies, however, the averaging expression for each of the SSA matrices changes as follows:

$$M=ld\left(\sum_{i=1}^{6}M_i\right)+(1-6d)(M_7), \tag{34}$$

where phases $M_{1\sim6}$ correspond to the inductor-charging phases, while M_7 corresponds to the inductor-discharging phase.

TABLE XIV

3-LEVEL HYBRID DICKSON STATE-SPACE MATRICES

$$A = \begin{bmatrix} -\frac{1}{RC_O} & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_O} & \frac{1}{C_O} & \frac{1}{C_O} \\ 0 & -2K_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -K_2 & K_2 & K_2 & -K_2 & 0 & \frac{D}{C_{F2}} & -\frac{D}{C_{F2}} & 0 \\ 0 & -K_3 & K_3 & K_3 & -K_3 & 0 & -\frac{D}{C_{F3}} & \frac{D}{C_{F3}} & 0 \\ 0 & 0 & -K_4 & K_4 & K_4 & -K_4 & \frac{D}{C_{F4}} & -\frac{D}{C_{F4}} & 0 \\ 0 & 0 & K_5 & -K_5 & -K_5 & K_5 & 0 & \frac{D}{C_{F5}} & -\frac{2D}{C_{F5}} \\ -\frac{1}{L_1} & 0 & -\frac{2D}{L_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ -\frac{1}{L_2} & 0 & \frac{D}{L_2} & -\frac{D}{L_2} & \frac{D}{L_2} & -\frac{D}{L_2} & 0 & 0 & 0 \\ -\frac{1}{L_3} & 0 & 0 & 0 & 0 & \frac{2D}{L_3} & 0 & 0 & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} 0 & K_1 & 0 & 0 & 0 & 0 & \frac{D}{L_1} & 0 & 0 \end{bmatrix}^T$$

V_{CF} dependencies ⇒ $a_{2,2}\neq 0$ inherently

$$x_0 = [V_C \quad V_{CF1} \quad V_{CF2} \quad V_{CF3} \quad V_{CF4} \quad V_{CF5} \quad I_{L1} \quad I_{L2} \quad I_{L3}]^T$$

$$= \left[\frac{DV_g}{5} \quad \frac{V_g}{2} \quad \frac{2V_g}{5} \quad \frac{3V_g}{10} \quad \frac{V_g}{5} \quad \frac{V_g}{10} \quad \frac{2DV_g}{25R} \quad \frac{2DV_g}{25R} \quad \frac{DV_g}{25R}\right]^T$$

$K_{1\sim5}=0$ ⇒ Rank(A)=6 ⇒ $|A|=0$ ⇒ need 3 more constraints ⇒ add dependencies ⇒ A full rank ⇒ Inherently balanced

$K_{3,5}=0$ ⇒ A full rank ⇒ Two redundant dependencies ⇒ Same solution

Modifying the traditional SSA model in a similar manner to what we did for the DIH before by adding five arbitrary constants, $K_{1\sim5}$, considering the dependencies between all the flying capacitors (Fig. 15), in the following way makes matrix A inherently invertible, thereby resulting in the correct and unique DC solution (Table XIV):

$$\frac{\Delta V_{CF1}}{\Delta t} = K_1\left(V_{CF1} - \frac{V_g}{2}\right), \tag{35}$$

$$\frac{\Delta V_{CF2}}{\Delta t} = K_2(V_{CF2} - V_{CF1} + V_{CF3} - V_{CF4}), \tag{36}$$

$$\frac{\Delta V_{CF3}}{\Delta t} = K_3(V_{CF3} - V_{CF1} - V_{CF4} + V_{CF2}), \tag{37}$$

$$\frac{\Delta V_{CF4}}{\Delta t} = K_4(V_{CF4} - V_{CF2} + V_{CF3} - V_{CF5}), \tag{38}$$

$$\frac{\Delta V_{CF5}}{\Delta t} = K_5(V_{CF5} + V_{CF2} - V_{CF3} - V_{CF4}). \tag{39}$$

As before, the ideal model with proposed invertibility principle predicts inherently balanced C_{Fs}, while achieving the correct and unique DC solution of all state variables. Again, the final solution is not affected by the addition of redundant constants.

H. 12-Level Series Cap., Two Inds. & Eleven C_{Flys}, 4-Phase

Another two-inductor topology with inherent flying capacitor balancing property is 12-level series capacitor (12LSC) [26], shown in Fig. 16, with eleven flying capacitors, two inductor-charging and two inductor-discharging phases, resulting in a total of four phases of operation. The governing equation for each storage element remains the same as other topologies, whereas SSA averaging expression is given by (1), due to same number of phases as DSD.

The traditional SSA model is modified by adding eleven arbitrary constants, $K_{1\sim11}$, including one redundant constant for the dependencies between the flying capacitors (Fig. 16) as follows:

$$\frac{\Delta V_{CF1}}{\Delta t} = K_1(V_{CF1} + V_{CF2} - V_{CF3} - V_g), \tag{40}$$

TABLE XV

12-LEVEL SERIES CAPACITOR STATE-SPACE MATRICES

$$\begin{bmatrix} a_{1,1} & & & & a_{1,13} & a_{1,14} \\ a_{2,2} & a_{2,3} & a_{2,4} & & a_{2,13} & a_{2,14} \\ a_{3,2} & a_{3,3} & a_{3,12} & & a_{3,13} & a_{3,14} \\ a_{4,3} & a_{4,4} & a_{4,5} & a_{4,6} & a_{4,13} & a_{4,14} \\ a_{5,4} & a_{5,5} & a_{5,12} & & a_{5,13} & a_{5,14} \\ a_{6,5} & a_{6,6} & a_{6,7} & a_{6,8} & a_{6,13} & a_{6,14} \\ a_{7,6} & a_{7,7} & a_{7,12} & & a_{7,13} & a_{7,14} \\ a_{8,6} & a_{8,7} & a_{8,8} & a_{8,9} & a_{8,13} & a_{8,14} \\ a_{9,8} & a_{9,9} & a_{9,12} & & a_{9,13} & a_{9,14} \\ a_{10,9} & a_{10,10} & a_{10,11} & a_{10,12} & a_{10,13} & a_{10,14} \\ a_{11,10} & a_{11,11} & a_{11,12} & & a_{11,13} & a_{11,14} \\ a_{12,2} & a_{12,11} & a_{12,12} & & a_{12,13} & a_{12,14} \\ a_{13,1} & a_{13,2} & & & & \\ a_{14,1} & a_{14,2} & a_{14,3} & & & \end{bmatrix}$$

All other $a_{i,j}=0$

$$\begin{bmatrix} 0 \\ -K_1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ K_{11} \\ \frac{D}{L_1} \\ 0 \end{bmatrix}$$

B

$$\begin{bmatrix} -\frac{1}{RC_O} & 0 & 0 & 0 & \frac{1}{C_O} & \frac{1}{C_O} \\ K_1 & K_1 & -K_1 & 0 & \frac{D}{6C_{F1}} & -\frac{D}{6C_{F1}} \\ -K_2 & K_2 & K_2 & 0 & -\frac{D}{6C_{F2}} & \frac{D}{6C_{F2}} \\ -K_3 & K_3 & K_3 & -K_3 & \frac{D}{6C_{F3}} & -\frac{D}{6C_{F3}} \\ -K_4 & K_4 & K_4 & 0 & -\frac{D}{6C_{F4}} & \frac{D}{6C_{F4}} \\ -K_5 & K_5 & K_5 & -K_5 & \frac{D}{6C_{F5}} & -\frac{D}{6C_{F5}} \\ -K_6 & K_6 & K_6 & 0 & -\frac{D}{6C_{F6}} & \frac{D}{6C_{F6}} \\ -K_7 & K_7 & K_7 & -K_7 & \frac{D}{6C_{F7}} & -\frac{D}{6C_{F7}} \\ -K_8 & K_8 & K_8 & 0 & -\frac{D}{6C_{F8}} & \frac{D}{6C_{F8}} \\ -K_9 & K_9 & K_9 & -K_9 & \frac{D}{6C_{F9}} & -\frac{D}{6C_{F9}} \\ -K_{10} & K_{10} & K_{10} & 0 & -\frac{D}{6C_{F10}} & \frac{D}{6C_{F10}} \\ -K_{11} & -K_{11} & K_{11} & 0 & \frac{D}{6C_{F11}} & -\frac{D}{6C_{F11}} \\ -\frac{1}{L_1} & -\frac{D}{L_1} & 0 & 0 & 0 & 0 \\ -\frac{1}{L_2} & \frac{D}{L_2} & -\frac{D}{L_2} & 0 & 0 & 0 \end{bmatrix}$$

A

$$\begin{bmatrix} V_C \\ V_{CF1} \\ V_{CF2} \\ V_{CF3} \\ V_{CF4} \\ V_{CF5} \\ V_{CF6} \\ V_{CF7} \\ V_{CF8} \\ V_{CF9} \\ V_{CF10} \\ V_{CF11} \\ I_{L1} \\ I_{L2} \end{bmatrix} \quad \begin{bmatrix} \frac{DV_g}{12} \\ \frac{11V_g}{12} \\ \frac{5V_g}{6} \\ \frac{3V_g}{4} \\ \frac{2V_g}{3} \\ \frac{7V_g}{12} \\ \frac{V_g}{2} \\ \frac{5V_g}{12} \\ \frac{V_g}{3} \\ \frac{V_g}{4} \\ \frac{V_g}{6} \\ \frac{V_g}{12} \\ \frac{DV_g}{24R} \\ \frac{DV_g}{24R} \end{bmatrix}$$

x_0

$K_{1\sim11}=0$ ⇓ Rank(A)=4 ⇓ $|A|=0$ (A not invertible) ⇓ need 10 more constraints

⇒ add dependencies ⇒ A full rank ⇒ Inherently balanced

$K_6=0$ OR $K_7=0$ OR $K_8=0$ ⇒ Rank(A)=14 ⇒ A full rank ⇒ One redundant dependency ⇒ Same solution

$$\frac{\Delta V_{CF2}}{\Delta t} = K_2(V_{CF2} - V_{CF1} + V_{CF11}), \tag{41}$$

$$\frac{\Delta V_{CF3}}{\Delta t} = K_3(V_{CF3} - V_{CF2} + V_{CF4} - V_{CF5}), \tag{42}$$

$$\frac{\Delta V_{CF4}}{\Delta t} = K_4(V_{CF4} - V_{CF3} + V_{C11}), \tag{43}$$

$$\frac{\Delta V_{CF5}}{\Delta t} = K_5(V_{CF5} - V_{CF4} + V_{CF6} - V_{CF7}), \tag{44}$$

$$\frac{\Delta V_{CF6}}{\Delta t} = K_6(V_{CF6} - V_{CF5} + V_{CF11}), \tag{45}$$

$$\frac{\Delta V_{CF7}}{\Delta t} = K_7(V_{CF7} - V_{CF6} + V_{CF8} - V_{CF9}), \tag{46}$$

$$\frac{\Delta V_{CF8}}{\Delta t} = K_8(V_{CF8} - V_{CF7} + V_{CF11}), \tag{47}$$

$$\frac{\Delta V_{CF9}}{\Delta t} = K_9(V_{CF9} - V_{CF8} + V_{C10} - V_{C11}), \tag{48}$$

$$\frac{\Delta V_{CF10}}{\Delta t} = K_{10}(V_{C10} - V_{CF9} + V_{CF11}), \tag{49}$$

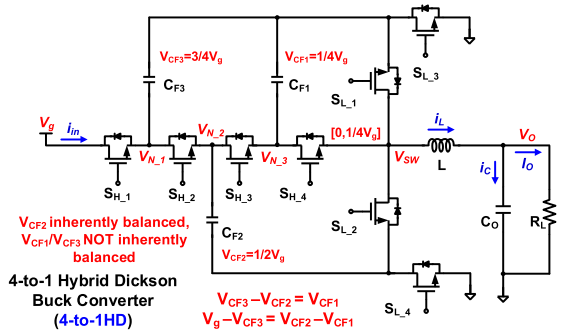


Fig. 17. 4-to-1 hybrid dickson buck converter topology.

TABLE XVI

4-TO-1 HYBRID DICKSON STATE-SPACE AVERAGING MATRICES

$$A=\begin{bmatrix} -\frac{1}{RC_O} & 0 & 0 & 0 & \frac{1}{C_O} \\ 0 & K_1 & K_1 & -K_1 & 0 \\ 0 & -K_2 & K_2 & K_2 & 0 \\ 0 & 0 & 0 & K_3 & 0 \\ -\frac{1}{L} & 0 & -\frac{D}{L} & 0 & 0 \end{bmatrix} \quad B=\begin{bmatrix} 0 & 0 & -K_2 & -\frac{3K_3}{4} & \frac{D}{L} \end{bmatrix}^T$$

$$x_0=[V_C \quad V_{CF1} \quad V_{CF2} \quad V_{CF3} \quad I_L]^T = \left[\frac{DV_g}{2} \quad \frac{V_g}{4} \quad \frac{V_g}{2} \quad \frac{3V_g}{4} \quad \frac{DV_g}{2R}\right]^T$$

$K_{1\sim3}$=0 ⇒ Rank(A)=2, need 3 more constraints

Dependencies ($K_{1,2}$≠0, K_3=0) ⇒ Rank(A)=4, Not enough constraints!

⇒|A|=0 ⇒ C_{Fs} unbalanced ⇒ Add C_{F3} balancer (K_3≠0) ⇒ A invertible

$$\frac{\Delta V_{CF11}}{\Delta t} = K_{11}(V_{C11} - V_{CF1} - V_{CF10} + V_g). \tag{50}$$

As a result, the correct and unique DC solution (Table XV) of all the state variables is achieved.

I. 4-to-1 Hybrid Dickson, One Ind. & Three C_{Flys}, 4-Phase

The final hybrid topology of interest for the analysis is the 4-to−1 hybrid Dickson (4-to−1HD) [27], [28], shown in Fig. 17, with single inductor and three flying capacitors. Although, this topology also has dependencies between the flying capacitors as was the case with other topologies, it does not have inherent balancing property that makes it a special case. Similar to DSD, the inductor charges for two phases and discharges for the other two phases, thereby making it a 4-phase operation. The governing equation for each storage element remains the same as other topologies, whereas SSA averaging expression is given by (1), due to same number of phases as DSD.

The dependencies between the flying capacitors (Fig. 12) can be added to the traditional SSA model by adding three arbitrary constants, $K_{1\sim3}$ as follows:

$$\frac{\Delta V_{CF1}}{\Delta t} = K_1(V_{CF1} + V_{CF2} - V_{CF3}), \tag{51}$$

$$\frac{\Delta V_{CF2}}{\Delta t} = K_2(V_{CF2} - V_{CF1} + V_{CF3} - V_g), \tag{52}$$

$$\frac{\Delta V_{CF3}}{\Delta t} = K_3\left(V_{CF3} - \frac{3V_g}{4}\right). \tag{53}$$

However, the dependencies are not enough in this case to provide the required number of constraints for a unique solution, therefore matrix A remains singular and the proposed invertibility principle suggests that V_{CF3} balancer be added to the model for the missing constraint making matrix A invertible, thus the correct and unique DC solution is reached (Table XVI), again corroborating the known requirement of a V_{CF} balancer for this topology [27]. It is worth nothing that this topology is a special case where matrix A is a composite

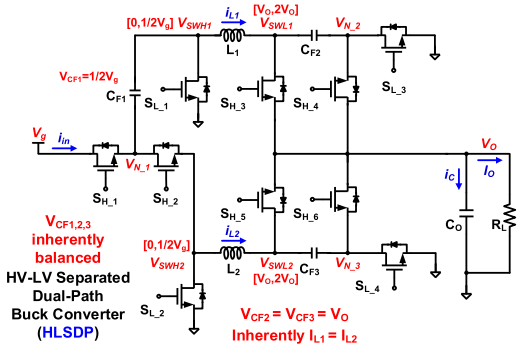


Fig. 18. HV-LV separated (HLS) Dual-Path hybrid buck converter topology.

TABLE XVII

HLS DUAL-PATH STATE-SPACE AVERAGING MATRICES

$$A=\begin{bmatrix} -\frac{1}{RC_O} & 0 & 0 & 0 & \frac{2-D}{C_O} & \frac{2-D}{C_O} \\ 0 & 0 & 0 & 0 & \frac{D}{C_{F1}} & -\frac{D}{C_{F1}} \\ 0 & 0 & -K_2 & K_2 & 0 & 0 \\ -K_3 & 0 & 0 & K_3 & 0 & 0 \\ -\frac{1}{L_1} & -\frac{D}{L_1} & \frac{D-1}{L_1} & 0 & 0 & 0 \\ -\frac{1}{L_2} & \frac{D}{L_2} & 0 & \frac{D-1}{L_2} & 0 & 0 \end{bmatrix}$$

$K_{2,3}$=0 ⇓ Rank(A)=4 need 2 more constraints, dependencies ($K_{2,3}$≠0) ⇓ A full rank ⇒ inherently balanced

$$B=\begin{bmatrix} 0 & 0 & 0 & 0 & \frac{D}{L_1} & 0 \end{bmatrix}^T \quad x_0=[V_C \quad V_{CF1} \quad V_{CF2} \quad V_{CF3} \quad I_{L1} \quad I_{L2}]^T$$

$$= \left[\frac{DV_g}{2(2-D)} \quad \frac{V_g}{2} \quad \frac{DV_g}{2(2-D)} \quad \frac{DV_g}{2(2-D)} \quad \frac{DV_g}{4R(2-D)^2} \quad \frac{DV_g}{4R(2-D)^2}\right]^T$$

of the constants derived from both the dependencies and a V_{CF} balancer.

J. HV-LV Separated, Two Inds. & Three C_{Flys}, 4-Phase

The final hybrid topology of interest for the analysis is the HV-LV separated dual-path (HLSDP) [29], shown in Fig. 18, with dual inductors and three flying capacitors. This topology is unique because it does not have inductor-last configuration as was the case with the previously discussed topologies. The output current is provided via dual paths i.e. both the inductors and flying capacitors contribute to the output current [29]. Despite the dependencies between the flying capacitors, matrix A for this topology is invertible (Table XVII) thus it has inherent balancing property using the proposed invertibility principle. The HLSDP topology also has four phases of operation, similar to DSD, whereby it makes the averaging expression same as (1).

The two arbitrary constants, $K_{2,3}$, incorporate the dependencies between the capacitors (Fig. 18) to the traditional SSA model as follows:

$$\frac{\Delta V_{CF2}}{\Delta t} = K_2(V_{CF3} - V_{CF2}), \tag{54}$$

$$\frac{\Delta V_{CF3}}{\Delta t} = K_3(V_{CF3} - V_O), \tag{55}$$

thereby achieving the correct and unique DC solution (Table XVII) of all the state variables again.

The small-signal transfer functions, such as control-to-output, for each of the aforementioned topologies can be easily derived using (8) and the already derived DC operating points, x_0, using the same procedure shown earlier for DSD from Section II-A onwards. The matrix E, given by (7) for DSD, can be derived using averaging expressions of each topology while matrix G, given by (9) for DSD, can be derived using (5)

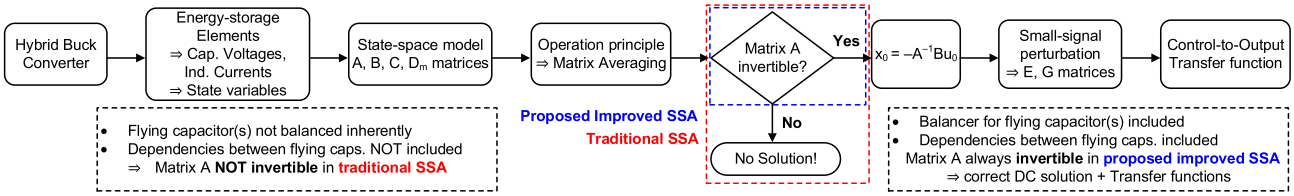


Fig. 19. Comparison between traditional and proposed improved SSA methodologies to derive transfer functions.

TABLE XVIII
COMPARISON BETWEEN TRADITIONAL AND PROPOSED IMPROVED SSA METHODOLOGIES FOR HYBRID BUCK CONVERTERS

Hybrid Buck Topology	Balancing Characteristics	Dependencies & Comparison¥
3-level	NOT inherently balanced	No/No/Yes
4-level	NOT inherently balanced	No/No/Yes
DSD or Series Cap.	Inherently balanced Same inductor currents	No/Yes/Yes
Tri-State DSD	Only one C_F balanced Same inductor currents	No/No/Yes
Dual-Inductor Hybrid 3-to-1	Inherently balanced Different ind. currents	Yes/No/Yes
Dual-Inductor Hybrid 6-to-1	Inherently balanced Same inductor currents	Yes/No/Yes
DSD 3-Phase	Inherently balanced Same inductor currents	No/Yes/Yes
3-level Hybrid Dickson	Inherently balanced Different ind. currents	Yes/No/Yes
12-level Series Capacitor	Inherently balanced Same inductor currents	Yes/No/Yes
4-to-1 Hybrid Dickson	NOT inherently balanced	Yes/No/Yes
HV-LV Separated Dual-Path	Inherently balanced Same inductor currents	Yes/No/Yes

¥ Dependencies between flying capacitors / Traditional SSA solution exists / Proposed Enhanced solution exists

which is the same for each topology except the difference in i_L term that is a sum of all the inductor currents, thus depends on the numbers of inductors in a topology.

K. Summary of Proposed Matrix Invertibility Principle

The proposed matrix invertibility principle, in conjunction with the proposed enhancement to SSA model, establishes whether a given non-resonant buck converter inherently balances V_{CF}(s) to the required voltage(s) (via a single matrix A), and whether multi-inductor topologies inherently maintain identical inductor currents (by computing x_0). The results of this section are summarized in Table XVIII.

The primary contribution lies in guaranteeing the invertibility of the state matrix (dashed box in Fig. 19) for any hybrid buck topology (excluding resonant topologies, e.g., a switch-tank converter [30]), which is crucial for the continuation of the analysis. Once the steady-state matrix, x_0, is derived, the methodology seamlessly progresses to the small signal transfer function derivation – a routine step in SSA-based analysis. Therefore, we think it suffices to derive x_0 without providing measurement results. Conversely, the DSD topology is selected to include non-idealities, and it is subjected to a complete analysis (entire flow in Fig. 19) with experimental verification.

V. CONCLUSION

In this paper, matrix invertibility principle is proposed with convergence enhancements to SSA-based methodology for high-ratio hybrid DC-DC converters, including circuit non-idealities, to determine flying-capacitor balancing property. The theoretical analysis of DSD is verified with PSIM, PXF simulations, in Cadence, and GaN-based PCB measurements. DSD topology is first used as the initial case study highlighting important parasitics, the analysis is then extended to other popular hybrid topologies. Primary observations are summarized below:

1) Matrix A, the state matrix, in SSA model is not invertible for a hybrid topology with V_{CF} not intrinsically balanced;

2) Conventional SSA model is not complete without incorporating dependencies between the flying capacitors;

3) SSA model can achieve convergence simply by adding constants considering V_{CF} balancer effects or intrinsic dependencies between flying capacitors or both;

4) Guidance to derive the small-signal transfer functions of several multi-level and multi-inductor converters provided;

5) The DC operating point results derived using enhanced SSA model are identical to the steady-state results derived using traditional volt-sec and amp-sec balance expressions;

6) The proposed methodology is simple and systematic in nature guaranteeing invertibility of the state matrix without loss of dynamic information for state variables;

7) The enhanced SSA model is applicable to any non-resonant hybrid buck topology, in general, making it possible to derive transfer functions for a whole range of topologies: with multiple flying capacitors with and without dependencies, different numbers of inductors and/or phases with and without identical inductor currents regardless of the inductor placement, and whether some or all flying capacitors are naturally balanced; and the principle holds true even in the absence of parasitics.

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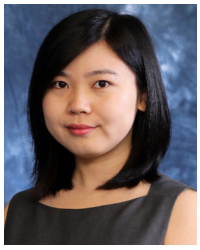

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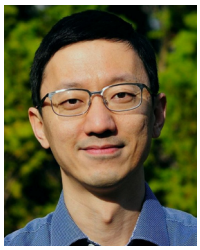

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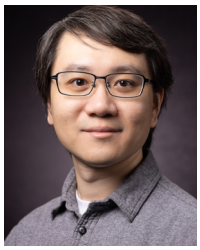

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