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Graded index couplers for next generation chip-to-chip and fiber-to-chip photonic packaging

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Abstract

The transition towards designs which co-package electronic and photonic die together in data center switch packages has created a scaling path to Petabyte per second (Pbps) input/output (I/O) in such systems. In a co-packaged design, the scaling of bandwidth, cost, and energy will be governed by the number of optical I/O channels and the data rate per channel. While optical communication provide an opportunity to exploit wavelength division multiplexing to scale data rate, the limited 127 μm pitch of V-groove based single mode fiber arrays and the use of active alignment and bonding for their packaging present challenges to scaling the number of optical channels. Flip-chip optical couplers which allow for low loss, broadband operation and automated passive assembly represent a solution for continued scaling. In this paper, we propose a novel scheme to vertically couple between silicon based waveguides on separate chips using graded index couplers in combination with an evanescent coupler. Simulation results using a 3D finite-difference time-domain solver are presented, demonstrating coupling losses as low as 0.35 dB for a chip-to-chip gap of 11 μm; 1 dB vertical and lateral alignment tolerances of approximately 2.45 μm and $\pm$ 2.66 μm, respectively; and a possible 1 dB bandwidth of greater than 1500 nm. These results demonstrate the potential of our coupler as a universal interface in future co-packaged optics systems.

1. Introduction

Silicon photonic integrated circuits (Si-PICs) have seen significant advancement over the past 40 years, highlighted by their rise to dominance as data center interconnects [1] and the novel application of Si-PICs as biochemical sensors [2], in LIDAR [3], photonic switching [4], photonic computing [5], and even chip based 3D printing [6]. However, the scaling of optical input/output (I/O) remains a significant manufacturing challenge, underscored photonic packaging, assembly, and testing occupying 70%–80% of the total cost of Si-PIC manufacturing [7]. One of the primary barriers to optical I/O scaling is the use of active alignment and bonding of V-groove based single mode fiber (SMF) arrays to Si-PICs using UV-curable epoxies, increasing cost and limiting throughput. Not only are current optical packaging methods costly, but they are severely limited in terms of pitch—SMF arrays operating near datacom (1310 nm) or telecom (1550 nm) wavelengths have minimum pitches of 127 μm, meaning a maximum density of only 8 fibers/mm is possible. The assembly challenge is especially pertinent to co-packaged optics (CPO) systems, which may require $> 10^3$ SMFs to scale to the Pbps package I/O data rates by 2035 as required by current CPO trends [8]. In addition, photonic packaging solutions are further constrained by the optical coupling requirements in terms of bandwidth (i.e. the operational wavelength window), coupling loss, and polarization dependent loss. Specifically, the future targets set out by the

'Silicon Photonics' chapter of the *Integrated Photonic Systems Roadmap—International* (IPSR-I) calls for fiber-to-chip edge couplers featuring 0.5–1 dB coupling loss by 2030, 0.1–0.3 dB polarization dependent loss by 2035, and 800–1000 nm bandwidth by 2040 [9]. The combination of packaging related challenges and difficulties in scaling coupling performance represents a critical roadblock to building future Si-PIC based systems. This notion is further emphasized by the 'Transceivers and Interconnects' IPSR-I chapter indicating that flip-chip PICs with simultaneous optical and electrical connections, passive alignment of components, and $<$1 dB total insertion loss each represent a critical roadblock (or 'purple brick wall') to be addressed by 2029–2035 to continue interconnect performance scaling [10].

In light of these device, packaging, and assembly related problems, we have developed and patented [11] an optical coupling solution based on integrated graded index (GRIN) lenses and evanescent couplers which can be used for flip-chip (i.e. chip-to-chip, chip-to-interposer, or chip-to-package substrate) connections, analogous to the electrical solder joint. Moreover, this optical coupling solution can be simultaneously used for fiber-to-chip (or fiber-to-interposer or fiber-to-package substrate) coupling and packaged alongside electrical back-end-of-line (BEOL) interconnects. As will be described in this study, the proposed technology overcomes each of the aforementioned IPSR-I critical technology roadblocks for optical interconnects nearly 5–15 years in advance. Furthermore, it does so while simultaneously meeting current and future fabrication standards by being complimentary metal–oxide–semiconductor (CMOS) foundry compatible without requiring any metal hard masks or liftoff masks and without having any process temperature $>$ 350 °C. As will be shown, the coupler can also be fabricated on both silicon based and glass based substrates, making it compatible with the current state-of-the-art high performance silicon interposers used in electronics [12, 13] and the emerging high performance glass interposers and substrates being developed for co-packaged optics systems [14–17]. An example of how this can be incorporated in a CPO system layout with a glass package substrate is shown in figure 1.

This study focuses on the design and simulation of the GRIN coupler in the context of fiber-to-chip and chip-to-chip coupling. It is important to note that, for the purposes of this study, the phrase 'fiber-to-chip coupling' not only means coupling to PICs, but also fiber-to-interposer or fiber-to-package substrate connectivity as well. Similarly, the phrase 'chip-to-chip' can indicate chip-to-interposer or chip-to-package substrate connectivity. The simulations evaluated the coupling loss, 1 dB and 3 dB misalignment tolerances, 1 dB wavelength tolerance, and the fabrication tolerances of such a design. Moreover, section 1.1 describes the operational principle and novelty compared to prior designs, section 2 depicts the systems constraints and simulation setup, section 3 presents the collected data, section 4 shows initial fabrication progress towards realizing the GRIN lens experimentally, and section 5 provides takeaways and a comparison to similar designs.

1.1. Graded index (GRIN) optical couplers

The basis for our GRIN coupler design involves using silicon oxynitride ($Si_xO_yN_z$, abbreviated SiON for the remainder of this report) layers with a GRIN profile to vertically focus, and a lens and taper combination to horizontally focus the incoming optical mode, as shown in figure 2. Our design builds on prior efforts from [19, 20] and is similar to the variations found in [21–23]. However, our design is distinct from these in several ways. First, it is intended for coupling between two separate chips or from interposer to chip (inter-chip coupling) in addition to fiber-to-chip or fiber-to-interposer coupling. By using a GRIN coupler for chip-to-chip coupling, we can increase the allowable vertical gap between chips by an order of magnitude compared to other types of chip-to-chip couplers such as evanescent, grating, or edge based methods. An inter-chip gap $>$ 10 μm will allow for the integration of emerging high performance electrical connections such as solderless Cu μ-pillar bumps [24] or solder-based μ-bumps [25, 26] without the need for fabricating them in a trench. Moreover, this can be accomplished without sacrificing the ability to process GRIN couplers in parallel at the wafer scale, unlike couplers reliant on two photon polymerization (TPP) processes which are fabricated serially. The goal of these couplers will be to increase lateral 1 dB alignment tolerance beyond the capability of the current automated pick-and-place die bonders found in high volume manufacturing [27–29] so that passive assembly can be utilized. Widening alignment tolerances to enable passive assembly of optical and electrical components directly equates to faster assembly speeds and lower costs.

The second novel aspect of our design is the addition of an evanescent coupling element after the GRIN lens, to allow for coupling directly to standard 220 nm silicon nitride (SiN) or 220 nm silicon-on-insulator (SOI) waveguides [30, 31], or other desirable material platforms such as indium phosphide (InP) or lithium niobate ($LiNbO_3$). By integrating an evanescent coupling element, not only can

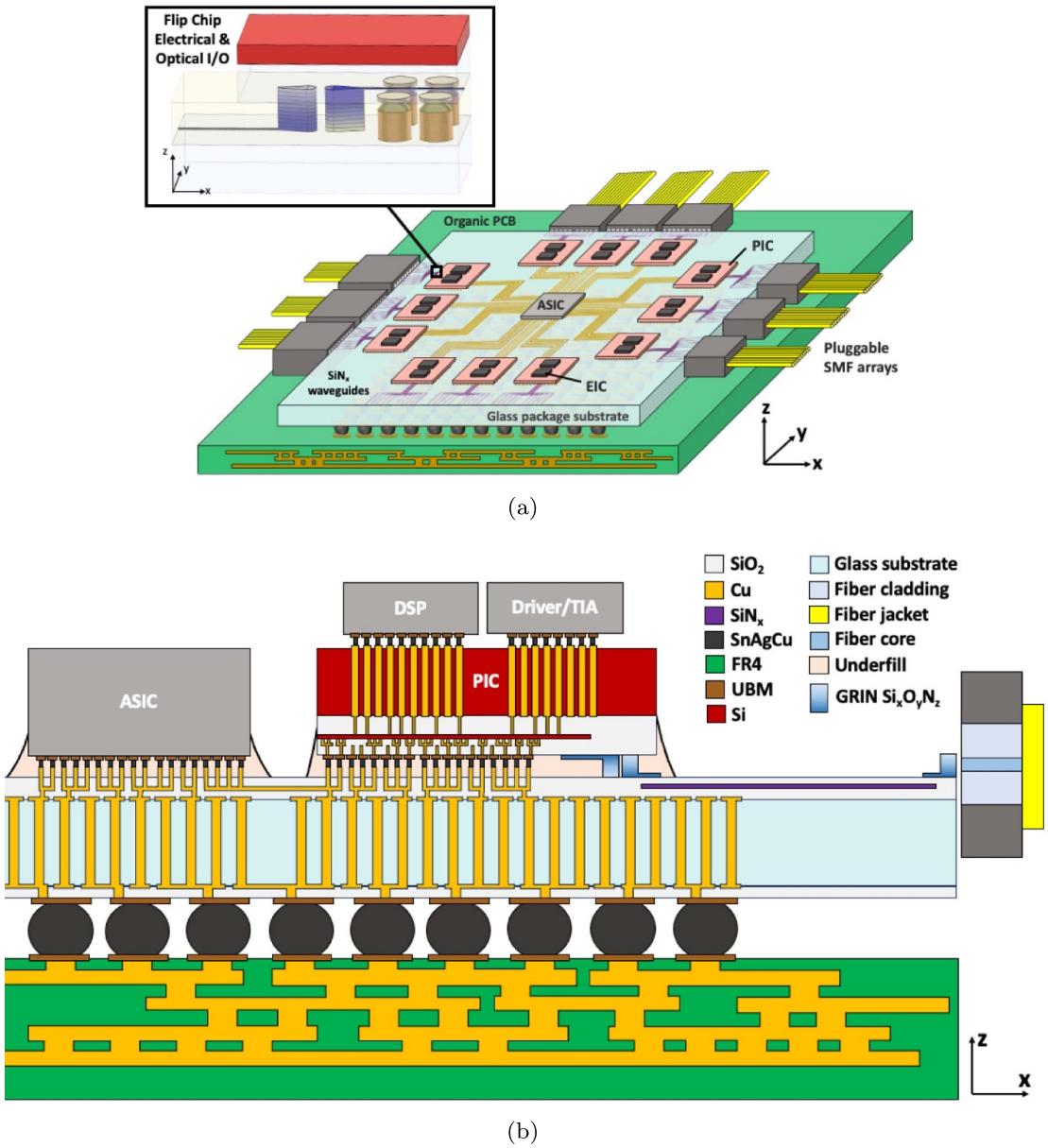

Figure 1. An example of the GRIN coupler deployed in a co-packaged optics system. In (a), a 3D view shows light entering the edge of a glass package substrate using a GRIN fiber-to-chip coupler and being transferred to a Si-PIC using a GRIN chip-to-chip coupler. In (b), a 2D cross section shows the simultaneous optical and electrical fanout occurring between the ASIC, a single Si-PIC, and a single fiber array which is enabled by the GRIN coupler. The images above were adapted from [18] to add the GRIN lens element. Reproduced from [18]. CC BY 4.0.

the input and output waveguide material be customized, but the GRIN lens can be deposited in the BEOL using only low-temperature plasma enhanced chemical vapor deposition (PECVD) processes ($<$ 350 °C) with no additional annealing. In addition, with minimum SiON feature sizes as large as 500 nm, the GRIN coupler can be patterned using more mature technology nodes such as i-line (365 nm) photolithography [32–34] with standard reactive ion etching (RIE). The aforementioned processes, along with the fact that the processing requires no metal hard masks or liftoff masks, helps maintain compatibility with microelectronic foundry tools used in CMOS process flows, leading to a decrease in fabrication complexity, and thus cost. Finally, by providing an interface for both chip-to-chip and fiber-to-chip coupling, one which is material agnostic to the input and output waveguides and can be added in the BEOL, the GRIN coupler has the potential to be seen as a universal interface. The remainder of this study will discuss how the simulations were setup and will show the final results demonstrating high coupling efficiency with widened 1 dB alignment tolerances.

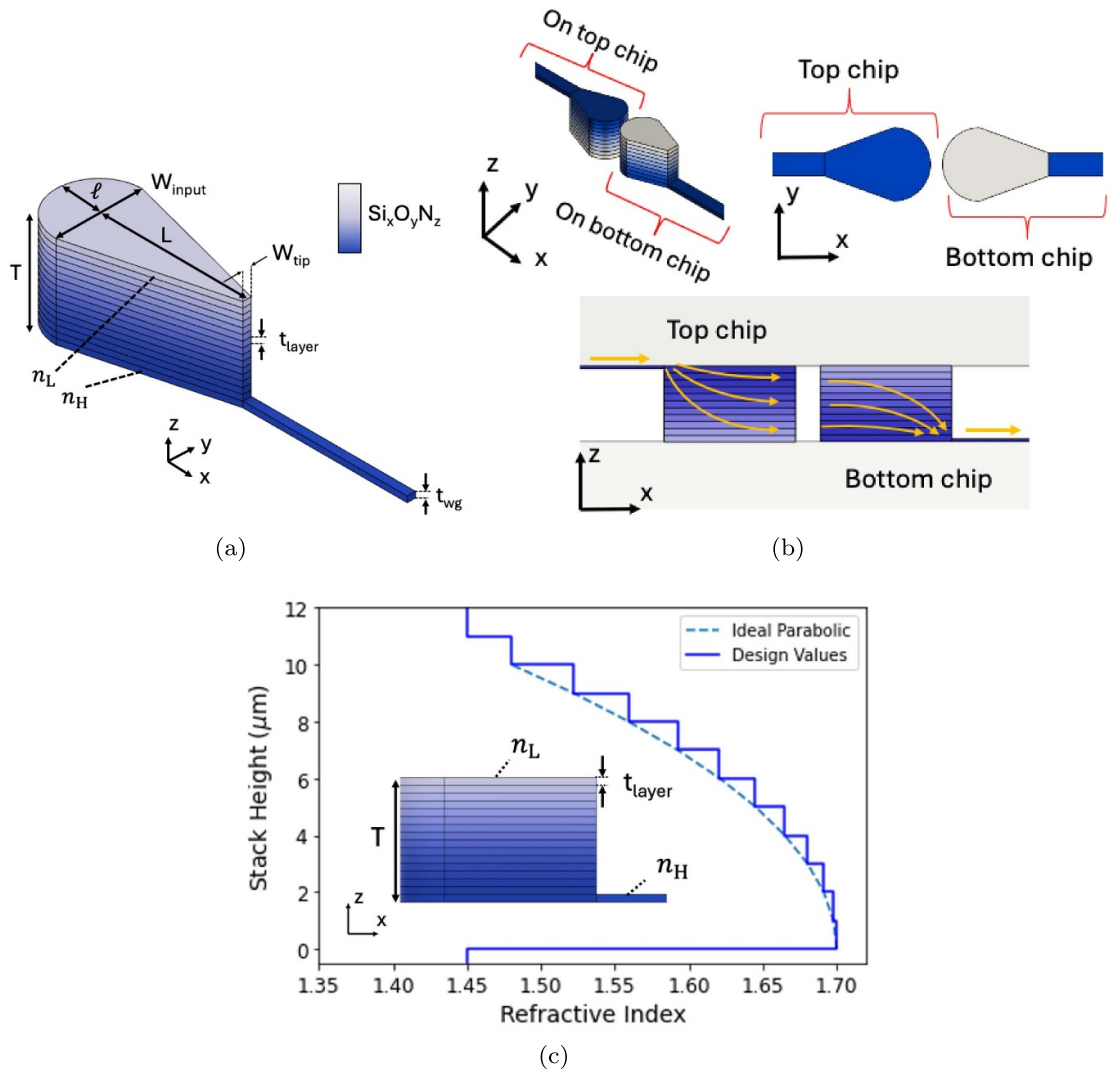

Figure 2. Schematics showing the GRIN coupler. In (a), a 3D view showing the basic building block of the GRIN coupler used for fiber-to-chip coupling [35]. Adapted with permission from [35] © The optical Society. In (b), a 3D view, top down view, and cross sectional view of how the GRIN coupler can be used for chip-to-chip coupling [35]. Reprinted with permission from [35] © The optical Society. In (c) a plot of the refractive index of the GRIN lens as a function of thickness is shown for the ideal parabolic profile and the step profile.

2. Materials and methods

2.1. Material platform constraints for SiON GRIN coupler

The design of the GRIN coupler, in theory, required the optimization of many variables; however, in practice this process was simplified by design constraints. First, the design methodology involved selecting the mode field diameter of the incoming beam (MFD_i), and the refractive index (n_{wg}) and thickness (t_{wg}) of the waveguides being coupled into. A flat facet, SMF-28 fiber with a 10.4 μm MFD was assumed, and waveguides with $n_{wg} = 1.7$ and $t_{wg} = 1\,\mu$m were chosen as the output from the GRIN coupler based on prior data for depositing and patterning NH_3 free SiON films using PECVD [20]. We would like to emphasize that selection of these three parameters (MFD_i, n_{wg}, t_{wg}) was arbitrary—the operation of the GRIN coupler and the optimization methodology described in this section can be applied to any new set of selections. With these selections, all remaining parameters including the GRIN thickness (T), GRIN width (W_{input}), number of layers (N), tip width (W_{tip}), waveguide width (W_{wg}), and layer refractive indices (n_i to n_f) were constrained, except the lens radius (r) and taper length (L), as outlined in table 1.

In particular, T and W_{input} were constrained to be approximately equal to MFD_i while W_{wg} and W_{tip} were constrained to the maximum waveguide width possible for the selections of n_{wg} and t_{wg}. To determine this maximum waveguide width, 2D finite-difference eigenmode simulations were executed which swept waveguide width assuming a cross section described by n_{wg} and t_{wg}, and surrounded by

Table 1. Summary of the design selections and constraints for parameter optimization.

	Selections			Constraints						
Parameter	MFD_i	n_{wg}	t_{wg}	T	W_{input}	N	W_{tip}	W_{wg}	n_i	n_f
Value	10.4 μm	1.7	1 μm	11 μm	11 μm	11	1.2 μm	1.2 μm	1.48	1.7

material with a refractive index equal to SiO_2 ($n_{SiO2} = 1.444$ at 1550 nm). Furthermore, N was constrained by t_{wg} and T such that the thickness of each layer in the GRIN was equal to t_{wg}. This constraint provides a reasonable minimum number of layers that should be used in the GRIN coupler which can always be increased for more advanced and optimized deposition processes. Finally, the coupler refractive index profile was parabolic from n_L to n_H, as shown in figure 2(c), using the following equation:

$$n(z) = n_H\left(1 - \frac{\alpha^2 z^2}{2}\right) \tag{1}$$

$$\alpha^2 = \frac{2\left(1 - \frac{n_L}{n_H}\right)}{T^2}. \tag{2}$$

The parabolic refractive index profile is necessary in order create the lensing effect predicted by Fermat's Principle and the ray equation [36]. With these selections and constraints, r and L were swept over using 3D-finite-difference time-domain (FDTD) simulations in Ansys Lumerical to optimize the design for maximum fiber-to-chip and chip-to-chip coupling efficiency. In order to properly form a lens with a given radius on the GRIN coupler, an equation for the lens surface needed to be developed. The lens surface is constrained such that it must intersect exactly at the edge of the GRIN at the points $(0, \frac{W_{input}}{2})$ and $(0, \frac{-W_{input}}{2})$ according to the coordinate system in figure 2(a) (assuming $(x,y) = (0,0)$ is at the center of the input of the GRIN coupler). For a circle of a given radius in the x–y plane with a center at (x_1, y_1) governed by the equation $r^2 = (x - x_1)^2 + (y - y_1)^2$, we can thus solve for the location of the center of the circle as $y_1 = 0$ and $x_1 = \sqrt{r^2 - \left(\frac{W_{input}}{2}\right)^2}$. The equation of the lens is then:

$$x = \sqrt{r^2 - \left(\frac{W_{input}}{2}\right)^2} - \sqrt{r^2 - y^2} \tag{3}$$

where $x_1 \geqslant 0$ and $x \leqslant 0$. The distance ℓ as described by figure 2(a) is obtained by inserting $y = 0$ into equation (3) and multiplying by a negative (because $x \leqslant 0$) such that:

$$\ell = r - \sqrt{r^2 - \left(\frac{W_{input}}{2}\right)^2}. \tag{4}$$

From these relationships, it is clear that the minimum r value that can be used is $\frac{W_{input}}{2}$ and as $r \to \infty$ that $\ell \to 0$ and the GRIN becomes flat faceted. This fact was used to establish bounds for sweeping the value of r during simulations to be 5.5–100 μm. Similarly, the focal length of an asymmetric GRIN lens with a parabolic refractive index profile can be approximated using the period of the ray oscillation, $\frac{2\pi}{\alpha}$, as described in [36]. The focal length of the asymmetric GRIN lens is then one quarter of the period (i.e. $\frac{\pi}{2\alpha}$). For the refractive index profile described by table 1, this indicates $\alpha \approx 0.051$ μm^{-2} and the focal length for a flat faceted GRIN is approximately 30 μm. This fact was used to establish bounds for sweeping the value of L during simulations to be 22–32 μm, centered slightly below 30 μm, since the lens section also contributes to vertical focusing.

2.2. Setup for 3D-FDTD GRIN coupler simulations

The performance metrics of interest in this study are coupling loss (in units of dB), 1 dB and 3 dB lateral alignment tolerance (in units of μm), 1 dB and 3 dB vertical alignment tolerance (in units of μm), and 1 dB bandwidth (in units of nm). Note that the simulation settings used here were derived in part from prior work [18, 37], and adjusted to fit the GRIN coupler.

For the 3D-FDTD simulation setup, override meshes which were one-fifth the minimum feature size were used in order to optimize simulation time. Convergence testing was performed by varying the override region's maximum mesh step from one-fifth to one-twentieth of the minimum feature size, with results showing coupling efficiency changed by $< 0.2\%$ from the coarsest to finest mesh. This coarse mesh was also validated by the fact that all device dimensions were > 1 μm scale. The background mesh

for the solver was set to Lumerical's preset auto-non uniform mesh with a mesh accuracy of '2' (this equates to approximately a 100 nm background mesh for a wavelength of 1.55 μm).Convergence testing was also performed for the background mesh by varying the mesh accuracy from '2' to '4' (i.e. from 100 nm to 50 nm maximum mesh step), with results showing coupling efficiency changed by $< 0.9\%$ from the coarsest to finest mesh. Moreover, perfectly-matched layer boundary conditions, which assume absorption of incident electric field, were used to account for loss due to out of plane scattering of light. For fiber-to-chip coupling, a Gaussian source with a waist radius of 5.2 μm and wavelength of 1.55 μm was placed 0.5 μm in front of the edge of the lens of the GRIN coupler. Transmission was measured through an output monitor 4 μm by 4 μm in size located 7 μm past the tip of the GRIN coupler.

For the 1 dB bandwidth calculations, the source wavelength spectrum was edited to range from 1.28 μm to 1.64 μm to reflect the wavelength regime used for tele- and data-communications. The refractive index of SiON in the wavelength regime simulated was assumed to be constant for all layers, an assumption supported by the infrared ellipsometry data presented in section 4 and in literature [38]. Because the Gaussian source does not use guided modes to create the beam, the electric and magnetic field angles of the incident beam were always perpendicular to the direction of propagation (i.e. a fundamental transverse electro-magnetic (TEM) mode). In order to accurately determine the dependence of coupling efficiency on wavelength, the fiber MFD was varied as function of wavelength as well. Specifically, the fiber MFD at the center or design wavelength of several fibers [39–43] was tabulated and fit over the wavelength regime from 530 to 2500 nm. To simulate, we used the fiber MFD from the fit equation every 50 nm from 530 to 2500 nm, running a monochromatic simulation around that MFD. The data was then smoothed afterwards using interpolation before plotting (this interpolation was simply for aesthetic reasons and had no impact on the conclusions of this report).

For chip-to-chip coupling simulations, a monochromatic transverse electric (TE) mode source with a wavelength of 1.55 μm was inserted in the input waveguide 6 μm prior to the tip of the GRIN lens. Transmission was measured through an output monitor 4 μm by 4 μm in size located 7 μm past the tip of the GRIN coupler. Similar to the fiber-to-chip coupling simulations, the 1 dB bandwidth calculations changed the source wavelength spectrum to extend from 1.28 μm to 1.64 μm with a wavelength step of 5 nm. In the chip-to-chip coupling simulations, the polarization of the mode source was also shifted from TE mode to transverse magnetic (TM) mode to determine polarization dependent losses.

To determine the 1 dB and 3 dB lateral (y), vertical (z), and longitudinal (x) alignment tolerances, sweeps were performed where the y, z ,and x misalignment of the GRIN coupler on the lower chip was varied from 0 to 3.5 μm. The y and z sweeps were performed assuming a 1 μm spacing in the x direction between the surface of the GRIN lens on either die. In terms of z alignment, the optimal position occurs when the bottom die GRIN coupler is in contact with the top die surface as shown in figure 2(b), and vice versa. The vertical distance from the top die substrate to the bottom die substrate is equal to T (11 μm). Thus, a positive vertical misalignment indicates a z offset between the two chips in addition to T.

Simulations to determine the fabrication tolerance of the layer refractive index profile and thickness for chip-to-chip coupling were also executed. These tolerances required a statistical analysis as opposed to a simple parameter sweep because during fabrication, the refractive index and thickness of all layers in the stack could be simultaneous varying. Therefore, this analysis was done using many 2D-FDTD simulations where the simulation was performed across the $y = 0$ plane. In the simulation, a sweep was performed for 0%–1.5% maximum error in the refractive index of a given layer. To do this, a maximum percent error was assigned (δ), and then N_s simulations were performed in which the refractive index of each layer of the GRIN lens was simultaneously perturbed by a different percentage randomly varying from $-\delta$ to δ (i.e. $n_{\text{layer}} = n_{\text{layer}} + Rn_{\text{layer}}\delta$ where R is a random number between -1 and 1). For our simulations, an N_s of 100 was used. An identical process was followed for random fluctuations in the thickness of each layer, except the sweep was performed from 0%–20% maximum error. Because the focal length changes slightly for the 2D versus 3D simulations (as the 2D simulations assume an infinitely wide GRIN lens), the focal length was re-optimized by performing a length sweep prior to performing any layer fluctuation simulations. Note that these simulations do not take into account the impact of random fluctuations in index or thickness on the horizontal confinement of the mode, only the vertical confinement. However, because the primary impact of a small change in index or thickness is on the vertical confinement through equations (1) and (2), these 2D simulations are valid to determine an approximate fabrication tolerance.

Along the same lines, the tolerance to lithographic misalignment was also explored using simulation. Specifically, this is the misalignment that may occur between the amorphous silicon (aSi) etch mask used for thick GRIN etching and the buried aSi etch stop mask used for defining the waveguide layer (to be discussed further in section 4). To simulate this tolerance, the GRIN output waveguide position

was shifted in the y direction in increments of 100 nm up to a maximum misalignment of 800 nm while the thick GRIN lens structure remained in the same y position. Note that the tolerance was evaluated using chip-to-chip simulations, though it was assumed to be the same as for fiber-to-chip simulations, and only the output waveguide for the lower chip was shifted (the input waveguide for the top chip remained in proper alignment). Finally, simulations to determine the allowable variation in the underfill refractive index were conducted. This was done by varying the underfill index from that of air (n_{air} = 1.0) to 1.6. During these simulations, the underfill is assumed to fill the entire gap between the two die. The results of these simulations will be presented in the following section.

2.3. Setup for 3D-eigenmode expansion (EME) evanescent coupler simulations

To simulate the loss through the evanescent coupler connecting the SiON output waveguide from the GRIN coupler to the final silicon based waveguide, the 3D EME solver was used. The evanescent coupler involved using a double taper design and optimization process developed previously in [37] and fabricated in [18], except in this case it was used for connecting SiON to SOI and SiON to SiN_x instead of SOI to SiN_x. A top down view showing the double taper evanescent coupler can be found in figure 5(a) which uses the same labeling convention as [37]. The optimization process involved running a single 3D-EME simulation for a set of $W_{SiON,\,i}$, $W_{tip,\,SiON}$, $W_{Si,\,i}$, $W_{tip,\,Si}$ values where $W_{Si,\,i}$ and $W_{tip,\,Si}$ could indicate SOI or SiN_x. Each simulation swept across taper length (L_{taper}) up to 100 μm to determine at what length an adiabatic transition is formed. These simulations were performed for a matrix of $W_{SiON,\,i}$ and $W_{tip,\,SiON}$ values ranging from 0.6–1.2 μm and 400–600 nm, respectively. A matrix of $W_{Si,\,i}$ and $W_{tip,\,Si}$ values ranging from 0.23–0.44 μm and 100–200 nm were used for SOI and values ranging from 0.55–1 μm and 100–200 nm were used for SiN_x, respectively. The vertical gap between the tapers was assumed to be 200 nm and filled with SiO_2. This assumption is based on prior fabrication processes used to build inter-layer evanescent couplers which involved SiO_2 cladding deposition followed by chemical mechanical polishing (CMP) for planarization [44]. Finally, the mode was also varied from TE to TM to determine polarization dependent losses related to the evanescent coupler.

3. GRIN coupler simulation results

3.1. GRIN fiber-to-chip coupler simulation results

A plot showing the results for coupling efficiency at 1550 nm wavelength as a function of r and L can be found in figure 3(a). The creation of this plot involved linear interpolation of the simulated data to provide a smoother image and clearly show the dependencies on L and r. Note that the reported values for coupling loss in this study were still taken from the original simulated values, while the interpolated values provided a useful means to determine approximate alignment tolerance. From the data, a peak coupling efficiency of 86.6% (0.62 dB loss) was observed for r = 5.5 μm and L = 26 μm. The allowable fabrication tolerance before 1 dB of total coupling loss was observed was approximately 2 μm for L and r based on the contour lines in figure 3(a). The coupling efficiency as a function of vertical and lateral misalignment can be found in figure 3(b), demonstrating a 1 dB lateral alignment tolerance of $\pm$ 2.88 μm. The vertical alignment tolerance depends on the direction of misalignment, since the GRIN lens is asymmetric. The 1 dB vertical alignment tolerance when the fiber is shifted in the negative z direction is $\pm$ 2.99 μm and in the positive z direction it is $\pm$ 2.58 μm.

A plot showing the modal transformation from the fiber core to the output SiON waveguide at 1550 nm for the fundamental TEM mode can be found in figure 3(c). The images detail how the 10.4 μm MFD from the SMF transitions using the GRIN lens to approximately 1.42 μm in the single mode waveguide. The modal images also involved linear interpolation to smooth the relatively coarse simulation output. Note that the wavelength dependency of the fiber-to-chip coupler can be found later in figures 6(a) and 8, demonstrating a 1 dB bandwidth of 1449 nm.

3.2. GRIN chip-to-chip coupler simulation results

A separate sweep of r and L was performed for the chip-to-chip coupler at 1550 nm wavelength, such that the optimal r and L were 6 μm and 26 μm for a peak coupling efficiency of 93.9% (0.27 dB loss) as shown in figure 4(a). The image was created using linear interpolation in an identical fashion to the fiber-to-chip simulations shown in figure 3(a). The data shows an exceptionally large fabrication tolerance of $> \pm$ 1 μm from the optimized design values for both r and L. Likewise, the 1 dB lateral and vertical alignment tolerances were determined to be $\pm$ 2.66 μm and $\pm$ 2.45 μm, respectively, using the data in figure 4(b) which shows coupling efficiency as a function of y and z misalignment (after linear interpolation).

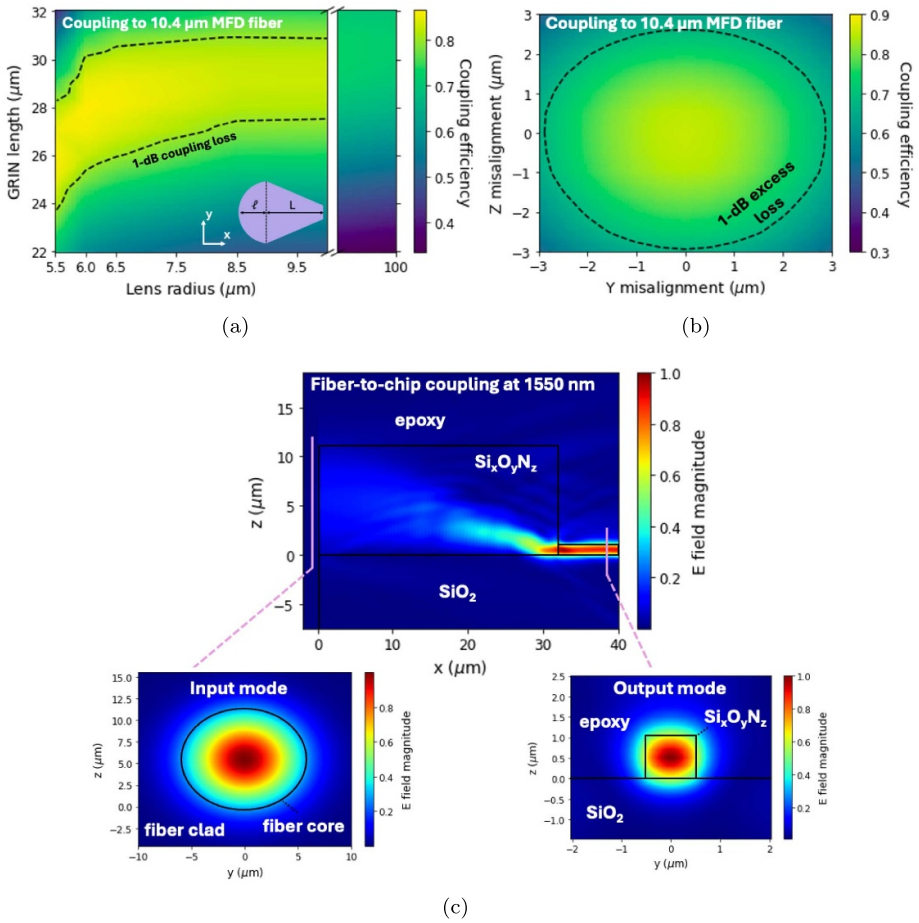

Figure 3. Simulations showing the GRIN coupler performance for fiber-to-chip coupling. In (a), coupling efficiency is shown for a 2D sweep of lens radius r and GRIN length L. The dotted contour line represents 1 dB of total coupling loss. In (b), coupling efficiency is shown for lateral and vertical misalignments. The dotted contour line represents 1 dB of additional loss from the position of maximum coupling. In (c) the transition of the optical mode from an MFD of 10.4 μm in the SMF to approximately 1.42 μm in the SiON waveguide is shown.

Using the optimized r and L, a plot showing the transformation of the fundamental TE mode during chip-to-chip coupling at 1550 nm wavelength, represented using the electric field magnitude on a linear scale, can be found in figure 4(c). The (linearly interpolated) modal images demonstrate the expansion and focusing within the GRIN lenses which resulted in successful coupling over an 11 μm vertical gap. In order to provide more accurate cross sectional modal plots, the mesh accuracy in Lumerical was also increased from '2' to '3' for the plots shown in figure 4(c). The performance of the coupler as a function of wavelength near 1550 nm and 1310 nm, and as a function of polarization, can be found later in figure 6(a). In this plot, the refractive indices of all films were assumed to be constant with wavelength (and material absorption was ignored). The data shows a 1 dB bandwidth exceeding 360 nm (1280–1640 nm) with polarization dependent losses below 0.1 dB between the fundamental TE and TM mode. Similarly, the dependence of GRIN chip-to-chip coupling as a function of the underfill epoxy refractive index is shown in figure 6(b). The plot demonstrates low coupling loss below 1 dB for epoxy refractive indices ranging from 1.3–1.5, enabling design flexibility when selecting the UV curable epoxy as well as operational robustness to changes in index incurred by thermal fluctuations imposed by dynamic environments. The dependence on the lithographic misalignment between the thick GRIN and the output waveguide masks is shown in figure 6(c). The results show that the chip-to-chip GRIN coupler coupling efficiency is $>$ 90% (or approximately 0.45 dB loss) even for lithographic misalignments of up to $\pm$ 300 nm, and misalignments up to $\pm$ 500 nm result in only an approximately 10% efficiency penalty (or around 0.5 dB loss penalty). Prior fabrication studies have shown better than $\pm$ 500 nm layer-to-layer alignment is possible for this exact GRIN process flow [45], and in general i-line stepper or contact lithography systems can achieve lithographic alignments of $<\pm$ 100 nm [34]. Finally, the effect of randomized refractive index fluctuations for each layer on the overall chip-to-chip coupling efficiency is shown in figures 6(d) and (e). Specifically, figure 6(d) shows the raw distributions of the number of 2D

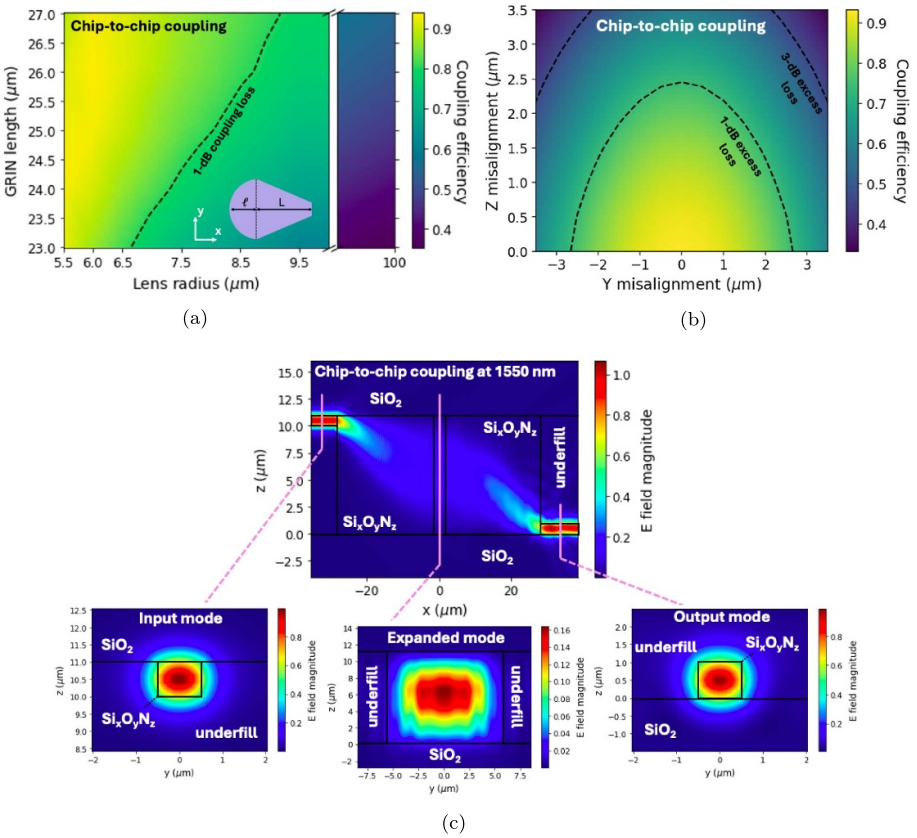

Figure 4. Simulations showing the GRIN coupler performance for chip-to-chip coupling. In (a), coupling efficiency is shown for a 2D sweep of lens radius r and GRIN length L. The dotted contour line represents 1 dB of total coupling loss. In (b), coupling efficiency is shown for lateral and vertical misalignments. The dotted contour lines represent 1 dB and 3 dB of additional loss from the position of maximum coupling. In (c) the transition of the optical mode from a SiON waveguide on one chip to a SiON waveguide on a separate chip across an 11 μm chip-to-chip gap is shown.

simulations where a given coupling loss was calculated, and how these distributions change as a function of the maximum applied percentage error. This data was then re-analyzed to plot the change in the average coupling loss (μ) with the maximum applied percentage error, and this is what figure 6(e) is highlighting. The same process was followed for random fluctuations in layer thickness, and the results from this are also plotted in figure 6(e). The shaded regions represent one standard deviation about the mean, or $\pm\ \sigma$.

3.3. Evanescent inter-layer coupler add-on for GRIN coupler

The sweeps over $W_{tip,\,SiON}$, $W_{tip,\,Si}$, $W_{SiON,\,i}$, and $W_{Si,\,i}$ resulted in optimized values of 400 nm, 100 nm, 1200 nm, and 230 nm, respectively, for coupling from SiON into SOI at 1550 nm with a 200 nm taper-to-taper gap. For coupling from SiON into SiN_x with the same simulation parameters, the optimized values for $W_{tip,\,SiON}$, $W_{tip,\,SiN}$, $W_{SiON,\,i}$, and $W_{SiN,\,i}$ were 400 nm, 200 nm, 1200 nm, and 1000 nm. A plot showing the results for evanescent coupling loss versus L_{taper} for the optimized design can be found in figure 5(b). The results show that to achieve coupling loss below 0.05 dB (>99% efficiency) at 1550 nm wavelength, the adiabatic taper length should be $> 25\ \mu$m and $> 40\ \mu$m for transfer from SiON into SiN_x or SOI waveguides, respectively. The transformation of the TE mode at 1550 nm from the SiON waveguide to a SOI wavguide can be seen in figure 5(c) using 3D FDTD simulations. The plot demonstrates high efficiency coupling using the double taper layout without substrate leakage through the BOX layer. Lastly, a plot showing the coupling loss as a function of wavelength can be found in figure 6(a). The data represents a 1 dB bandwidth of more than 360 nm.

4. GRIN chip-to-chip coupler fabrication progress

Prior work has demonstrated GRIN fiber-to-chip couplers with integrated lenses having a coupling loss of 0.4 dB from 1530–1625 nm [20]. This work intends to add to the prior work by increasing the thickness of the GRIN lens from 6 μm to 11 μm in order to couple light from flat-faceted, SMF28 fibers. In

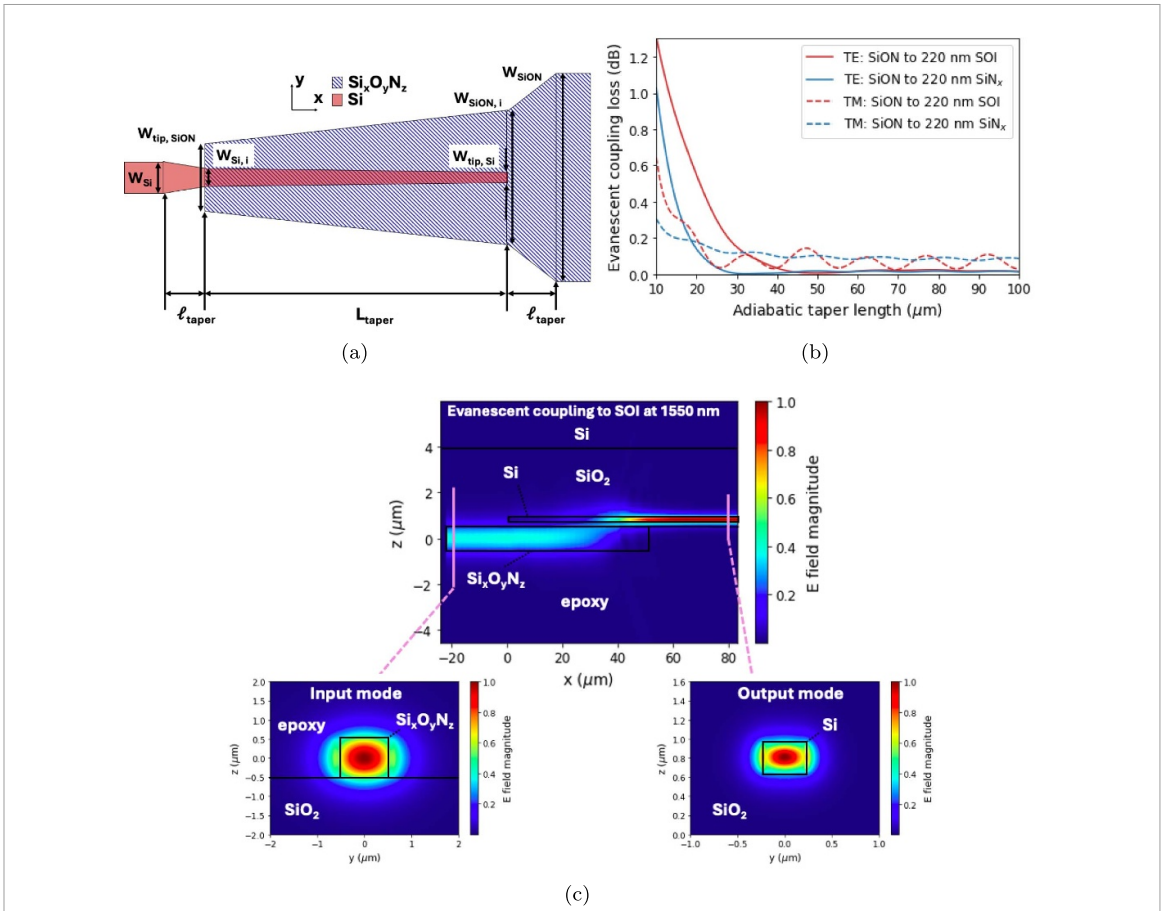

Figure 5. Simulations showing the performance of the evanescent coupler. In (a) a top down view shows the double taper design. In this figure, the label 'Si' (e.g. $W_{Si,i}$) can indicate either a SOI or SiN_x waveguide. In (b) the loss through the coupler as a function of taper length (L) is shown. In (c) a side view from a 3D FDTD simulation shows the optical mode's transition from the SiON to an SOI waveguide.

addition, the fabrication of GRIN lenses on glass substrates was explored as this is useful to the development of high performance interposers and package substrates with integrated silicon based waveguides. These two additions to prior work—an increased GRIN thickness and the use of glass substrates—presented fabrication challenges which needed to be overcome. First, a thicker GRIN lens necessitated patterning and etching a thicker aSi hard mask without losing resolution. Second, due to available tool constraints, electron beam lithography (EBL) processes for thick photoresist patterning on insulating substrates needed to be developed. This work builds on the prior work in [18] which established processes for the patterning of thin low pressure chemical vapor deposition (LPCVD) SiN_x waveguides on glass substrates. The targeted process flow is shown in figure 7 for creating the thick fiber-to-chip and chip-to-chip GRIN coupling structures on glass. This process flow can be duplicated for silicon substrates as well, assuming they contain the standard 2–3 BOX layer. It is important to note that, while the processes shown in figure 7 represent the fabrication work done in this study, additional process steps will be necessary to complete a working GRIN prototype. The most relevant of these additional steps are the deep dry etching of the glass edge facets and passive assembly using flip-chip pick-and-place die bonding with UV curable epoxy. These processes were established for flip-chip evanescent coupling and for edge coupling to LPCVD SiN_x standard tapers on glass in [18], and the application of these working processes to the GRIN coupler will be saved for future work. Thus, the following sections describe process development efforts intended to establish fabrication steps that match the performance of prior work and advance to thicker GRIN lenses on glass substrates.

4.1. PECVD of SiON films with controllable refractive index

The PECVD processes for SiON films with a controllable refractive index were developed using the a Samco PD220NL tool. The recipe used for deposition included the following parameters: 5 min, 0–300 sccm N_2O, 10 sccm SiH_4, 2 sccm NH_3, 390 sccm N_2, 13.56 MHz frequency, 350 °C, 80 Pa, and 100 W RF bias. The Samco PD220NL tool cannot reach high enough plasma densities to dissociate N_2; therefore, NH_3 needed to be added as a precursor. Depositions were carried out at 350 °C on a 6' AlN chuck

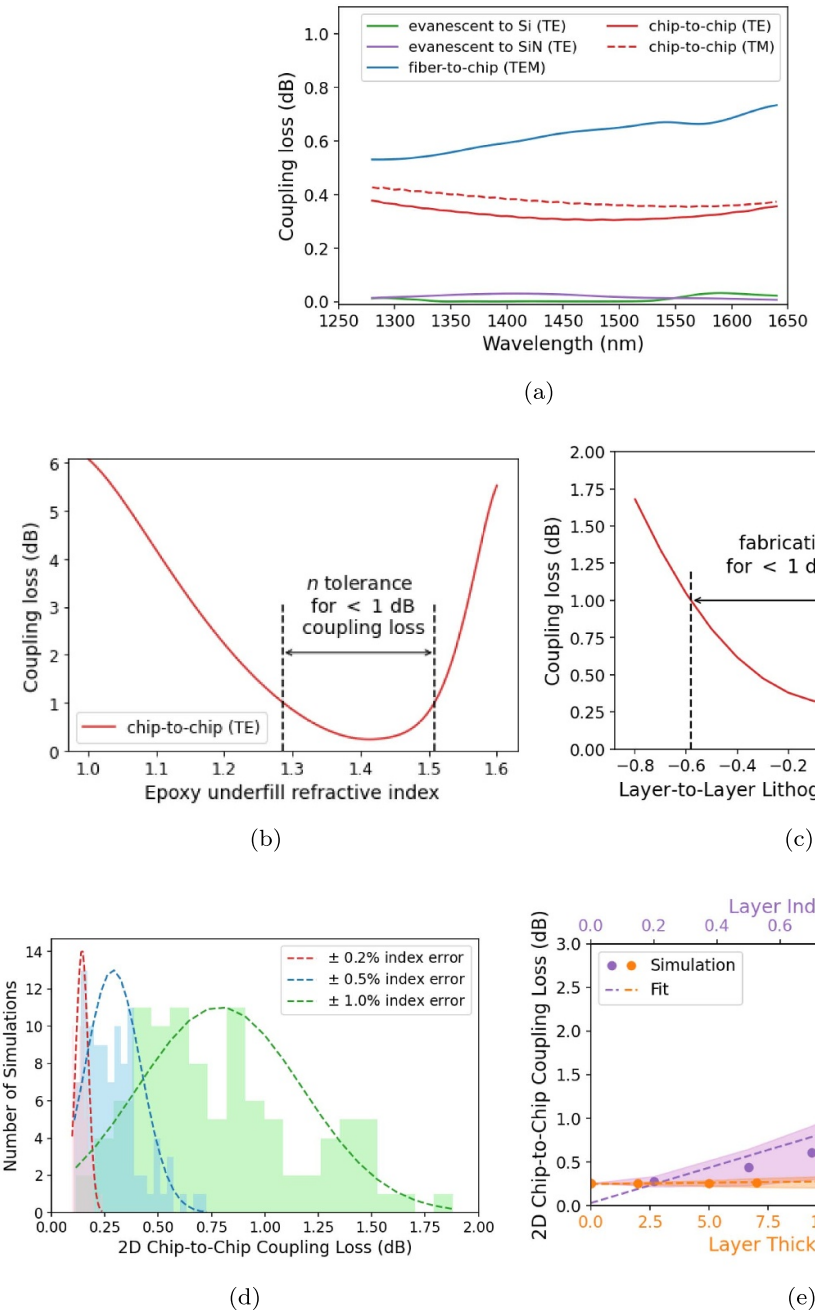

Figure 6. Simulations showing the effect of underfill refractive index, wavelength, and refractive index variation on GRIN coupling. In (a) the coupling loss is shown for the GRIN fiber-to-chip, GRIN chip-to-chip, and evanescent couplers as a function of wavelength. Note that the evanescent SOI and SiN_x tapers were of length $L = 100\,\mu$m and $\ell = 10\,\mu$m. In (b) the chip-to-chip coupling loss is shown as a function of the underfill refractive index, showing a wide 1 dB index tolerance of approximately 0.2. In (c) the GRIN chip-to-chip coupling loss is shown as a function of the misalignment induced by the layer-to-layer mask alignment process during lithography. In (d), histogram distributions show the number of 2D simulations as a function of the coupling loss. To obtain these distributions, randomized refractive index errors were applied to the GRIN coupler (with each layer having a different random error applied to it) where the maximum possible percentage error for a given layer ranged from 0.2%–1.0%. The mean and standard deviation of each distribution was then plotted in (e) as a function of the maximum percentage error and fit using linear regression.

with Si pieces approximately 15 mm by 15 mm in size which were cleaved from a 100 mm Si wafer (<100>, P type, 500 μm thick). Each deposition was carried out for the same time (5 min), but with a different N_2O flow rate. The refractive index and thickness of the films were measured using a Semilab SE-2000 spectroscopic ellipsometer. Each sample was then cross sectioned and the thickness of the thin film was measured using a scanning electron microscope (SEM). When fitting the refractive index, the thickness of the films was checked to match against the SEM measurements in order to provide a more accurate determination of the refractive index. Determining the refractive index and thickness of each film was done by measuring the reflected polarization spectrum at three different angles for

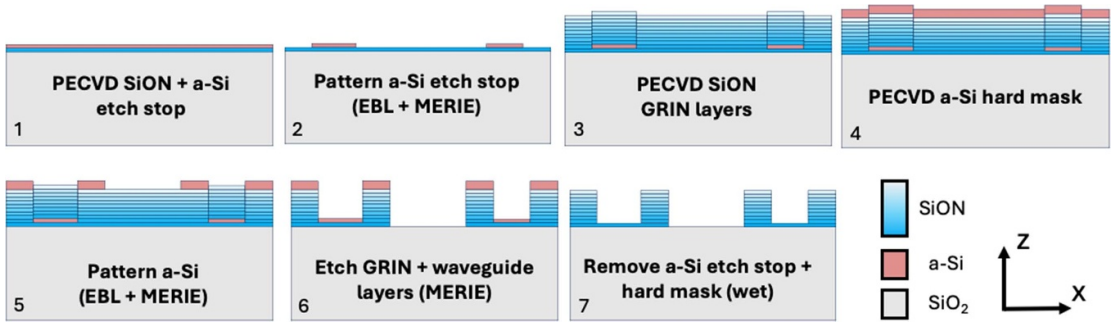

Figure 7. The process flow for fabrication of thick GRIN structures on glass substrates using EBL. This figure only shows the process steps which were executed in this report. The additional process steps which would follow step 7 would include deep dry etching to form glass edge facets for edge coupling and the flip-chip pick-and-place sequence using UV curable epoxy. These steps have been developed for flip-chip evanescent coupling as shown in [18], and future work will include transferring these processes to the GRIN prototype.

wavelengths from 400 nm to 1600 nm, and modeling the film using the two lowest order Cauchy coefficients (i.e. $n(\lambda) = n_\infty + n_1(\lambda)$). The resultant data for refractive index and thickness as a function of N_2O flow rate can be found in figure 8(b). This refractive index data was also used to simulate fiber-to-chip and chip-to-chip coupling where $n(\lambda)$ for the SiON layers was updated using the measured refractive index data shown in figure 8(a). By using the measured refractive index data, a more accurate model can be obtained for wavelengths extending beyond the 1250–1650 nm regime and into the visible, where refractive index has a stronger dependence on wavelength. Incorporating the measured data was done by determining the necessary N_2O flow rate for each layer, calculating the Cauchy coefficients for each of those N_2O flow rates, and importing the calculated n(λ) spectrum for each SiON layer into the simulation. Using this method, the data in figure 8(c) demonstrated fiber-to-SiON coupling with a coupling loss of 0.46 dB at 1310 nm, 0.64 dB at 1550 nm, and a minimum coupling loss of 0.45 dB at 1250 nm. Similar data was obtained for the chip-to-chip (i.e. SiON to SiON) coupling loss and is shown in figure 8(d), where the coupling loss at 1310 nm was 0.42 dB, at 1550 nm was 0.37 dB, and was a minimum of 0.35 dB at 1470 nm. Thus, the difference between the coupling loss for the optimized design and the updated design with experimentally obtained values was less than 0.02 dB and 0.1 dB for fiber-to-chip and chip-to-chip coupling at 1550 nm, respectively. Moreover, using the measured refractive index data and refractive index and extinction coefficient (k) data for Si and SiN_x from literature [46–48], coupler performance can be accurately simulated for wavelengths from 500 nm to greater than 2300 nm. The resultant data demonstrates an exceptionally large 1 dB bandwidth of 1562 nm for SiON to SiON, 1361 nm for SiN_x to SiN_x, and 888 nm for SOI to SOI coupling. The work in this section demonstrated successful fabrication of refractive index controllable SiON films using PECVD with standard, foundry compatible precursors and metrology techniques. In addition, performance of the GRIN coupler was verified by updating the model with experimentally meaured refractive index profiles for the SiON layers as a function of wavelength.

4.2. Electron beam lithography of thin SiON film using aSi mask

Following establishment of the refractive index profile, the processes for patterning the amorphous Si (aSi) etch stop on top of the waveguide layer were developed. For this process, 700 nm SiON was deposited using a N_2O flow rate of 10.9 sccm ($n = 1.898$ at 1550 nm) on a 3 μm SiO_2 BOX, following by the deposition of 400 nm of aSi using the same tool. The recipe for aSi deposition: 8 min 20 s, 28 sccm SiH_4, 500 sccm Ar, 100 W RF, 80 Pa, 270 °C, and 13.56 MHz frequency. The EBL to pattern the aSi builds off of the protocol established in [18] for the EBL of thin SOI and SiN_x-on-glass films using a diluted AZ nLOF 2020 photoresist. The primary change that was made was to the photoresist dilution, which was changed to 3:2 (nLOF:PGMEA) in order to increase the resist thickness to approximately 800 nm for a 2000 rpm, 60 s spin. This change was made because a 400 nm PECVD aSi hard mask was used compared to prior studies which used a 250 nm LPCVD poly-Si hard mask. The thicker etch stop was used due to the lower etch resistance of the PECVD aSi compared to LPCVD poly-Si. The aSi was etched using an Applied Materials Precision 5000 RF generated, magnetically enhanced RIE (MERIE) tool with a Cl_2/HBr gas chemistry. The Cl_2 recipe was as follows: 60 sccm Cl_2, 20 sccm HBr, 100 mTorr, 250 W, 60 Gauss. The selectivity of the photoresist was determined to be 1.58 (aSi:PR). The SiON was etched using a different chamber of the same tool with CF_4/CHF_3/Ar chemistry. The CHF_3 recipe was as follows: 155 s, 55 sccm CHF_3, 45 sccm CF_4, 100 sccm Ar, 50 mTorr, 600 W, 60 Gauss. The selectivity of the aSi was determined

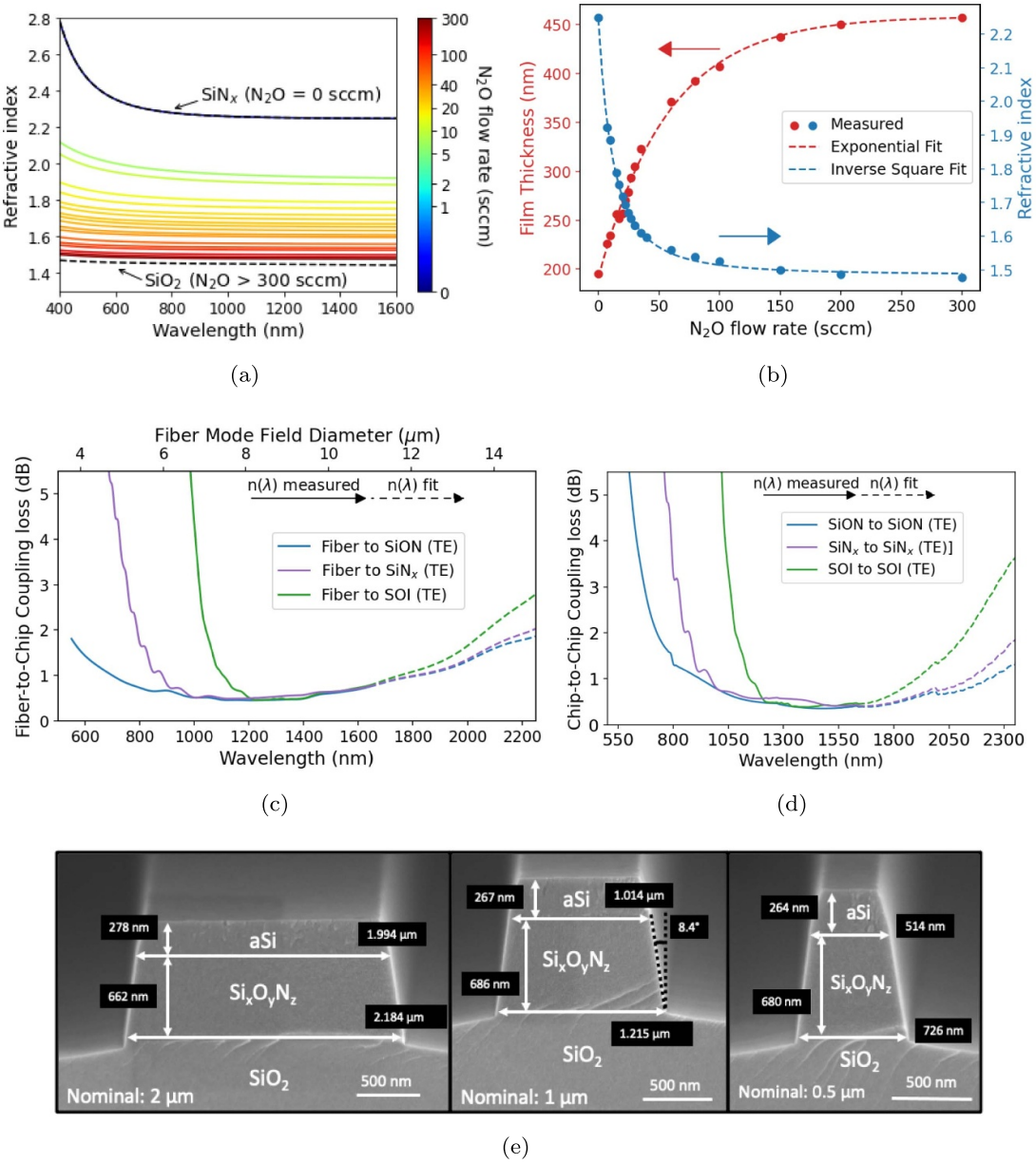

Figure 8. Experimental data for fabrication of the GRIN coupler. In (a) a plot of the measured refractive index of the SiON films as a function of wavelength for different N_2O gas flow rates. In (b) the measured thickness and refractive index of the SiON film as a function of N_2O flow rate are shown with their associated fits. In (c) and (d) simulated fiber-to-chip and chip-to-chip coupling loss, respectively, as a function of wavelength is shown. Note that these simulations were different from that found in figure 6(a) because n(λ) for all materials (SiON, Si, SiN_x, SiO_2) was imported using the measured refractive index data taken via ellipsometry in (a). In (e), cross sectional SEM images show the waveguide profile for different waveguide widths prior to removal of the aSi etch stop.

to be 9.4 (aSi:SiON). Cross sectional SEM images showing the SiON waveguide with the aSi hard mask still remaining can be found in figure 8(e), achieving widths from 500 nm to $> 1\,\mu$m with a measured sidewall slope of 8.4 °. The optimized dose for this structure was 55 $\mu C\,cm^{-2}$ with a beam current of 10 nA using an Elionix HS-50, 50 keV accelerating voltage system. The work in this section demonstrated successful EBL patterning of SiON waveguides using a PECVD aSi hard mask and a diluted, negative tone chemically amplified photoresist.

4.3. Electron beam lithography of thick SiON film on glass using aSi mask

With the refractive index profile and patterning of the aSi etch stop determined, the next step was to develop a process for patterning the GRIN lens that was $> 10\,\mu$m thick. A similar process to [20] was used, with the exception of EBL in place of i-line lithography. This was not done due to small features—the smallest feature size of the GRIN lens design is $> 1\,\mu$m—but rather the lack of access to a repeatable process for patterning 1 μm features using the UV photolithography tools within the facilities used.

Furthermore, it was known based on prior work that alignment with $< 0.5\,\mu$m precision (and preferably $< 0.2\,\mu$m precision) between the GRIN lens pattern and the etch stop pattern would be critical to achieving the low coupling loss predicted by simulation.

Like section 4.2, we followed a process similar to that used in [18] for EBL on glass substrates using AZ nLOF 2000 series photoresist. It was anticipated based on the results in section 4.2 that for Cl_2/HBr etching of aSi, the selectivity was approximately 1.58 (aSi:PR). Similarly, based on literature [49] and prior test samples, it was determined that faceting was occurring in the corners of the aSi hard mask as a result of etching the presence of a CHF_3 and Ar gas chemistry. Due to the low selectivity and presence of faceting, an aSi hard mask of 4 μm and a photoresist mask of 4 μm were targeted. The 4 μm aSi hard mask was deposited using the same PECVD recipe as in section 4.2, but for 80 min. The 4 μm thick photoresist was achieved using the same EBL steps as in section 4.2, but using undiluted AZ nLOF 2035 with a 2500 rpm, 30 s spin recipe. As in [18], a commercially available conductive polymer, ESpacer300Z, was spun at 4000 rpm for 30 s following photoresist spincoating in order to avoid charging during exposure. Immediately after exposure, but before the post-exposure bake, the glass samples were puddle soaked in DI water for 20 min to remove the ESpacer300Z. This was critical to ensure no mixing occurred between the conductive polymer and the photoresist during the post-exposure bake step, which was necessary to crosslink the resist. While the post-exposure bake was kept the same, the development time was adjusted to be 4 min. The SiO_2 pieces were then mounted on a 150 mm Si carrier wafer as in section 4.2 for subsequent etching. The Cl_2/HBr etch for the aSi hard mask was identical to that of section 4.2 aside from the time. The fluorine based etch was altered to a CHF_3/Ar only gas chemistry to increase selectivity to the aSi hard mask for the thicker GRIN lens. Based on prior results [20, 49], this change was anticipated to have little effect on the etch profile of the waveguide layer. The etch recipe that was used for the GRIN lens was as follows: 91 min, 55 sccm CHF_3, 100 sccm Ar, 50 mTorr, 600 W, 60 Gauss. The average selectivity of the aSi was determined to be 5.86 (aSi:SiON).

Several sets of SEM images can be found in figure 9 which show different aspects of the GRIN lens experimentally realized. For example, from the cross sectioned test sample shown in figure 9(a) (which used a purely photoresist mask but contained the same SiON stack), the elemental composition of the GRIN lens using energy dispersive spectrometry (EDS) can be seen. The EDS results, which also included a line scan taken from bottom to top and shown in figure 9(b), demonstrate a parabolically increasing amount of elemental oxygen when going from the bottom to the top of the GRIN lens. This reflects the parabolic increase of N_2O flow rate that was used for depositing each subsequent layer, which directly relates to refractive index. On the other hand, figure 9(c) shows a cleaved cross section with the fused silica substrate fully visible and the successful EBL patterning of a $> 10\,\mu$m stack on glass clearly represented. In addition, figure 9(c) reveals the faceting nature of the aSi hard mask mentioned earlier. Despite the faceting, the 4 μm thick aSi hard mask survived the deep etch without lateral dimension erosion affecting the stack beneath it. This is evidenced by smaller features, such as the 2.5 μm line shown in figure 9(c), maintaining shape. Finally, additional SEM images in figure 9(d), which were not full cross sections but still taken from the edge, show proper etch dimensions compared with nominal values. Specifically, the images show the top width of the GRIN lens ranging from 1 μm to 12 μm and aligning well with the design values, along with a measured sidewall slope of 6.8° for a 10.72 μm thick stack. Based on these results, which were part of a dose matrix, an optimal EBL recipe of 25 μC cm^{-2} for a 10 nA beam current was determined. The work in this section represent a step forward in terms of GRIN coupler fabrication as $> 10\,\mu$m thick lenses were able to be patterned on insulating substrates using EBL with a novel photoresist mixture.

5. Discussion of GRIN coupler dependencies

The primary factors contributing to the GRIN coupling loss are scattering losses associated with the GRIN facet interface and the output waveguide interface. Both of these losses can be attributed to imperfect modal overlap due to the parabolic GRIN profile. In the case of fiber-to-chip coupling, the GRIN facet interface involves modal overlap between the SMF and the GRIN coupler. Here, the shape of the mode inside the GRIN lens is not perfectly circular, like the mode inside the fiber as seen in figure 3(c), due to the GRIN profile having a high index material at the bottom ($n_H = 1.7$) and being rectangular in shape. In the case of chip-to-chip coupling, the modal overlap at this interface is increased since the structures are identical to one another (i.e. symmetric). The increased modal overlap at the GRIN facet interface accounts for the improvement in maximum coupling efficiency seen by the chip-to-chip coupler versus the fiber-to-chip coupler.

Similarly, for both fiber-to-chip and chip-to-chip coupling, the output waveguide interface involves modal overlap between the GRIN lens output and the output SiON waveguide. These modes are not

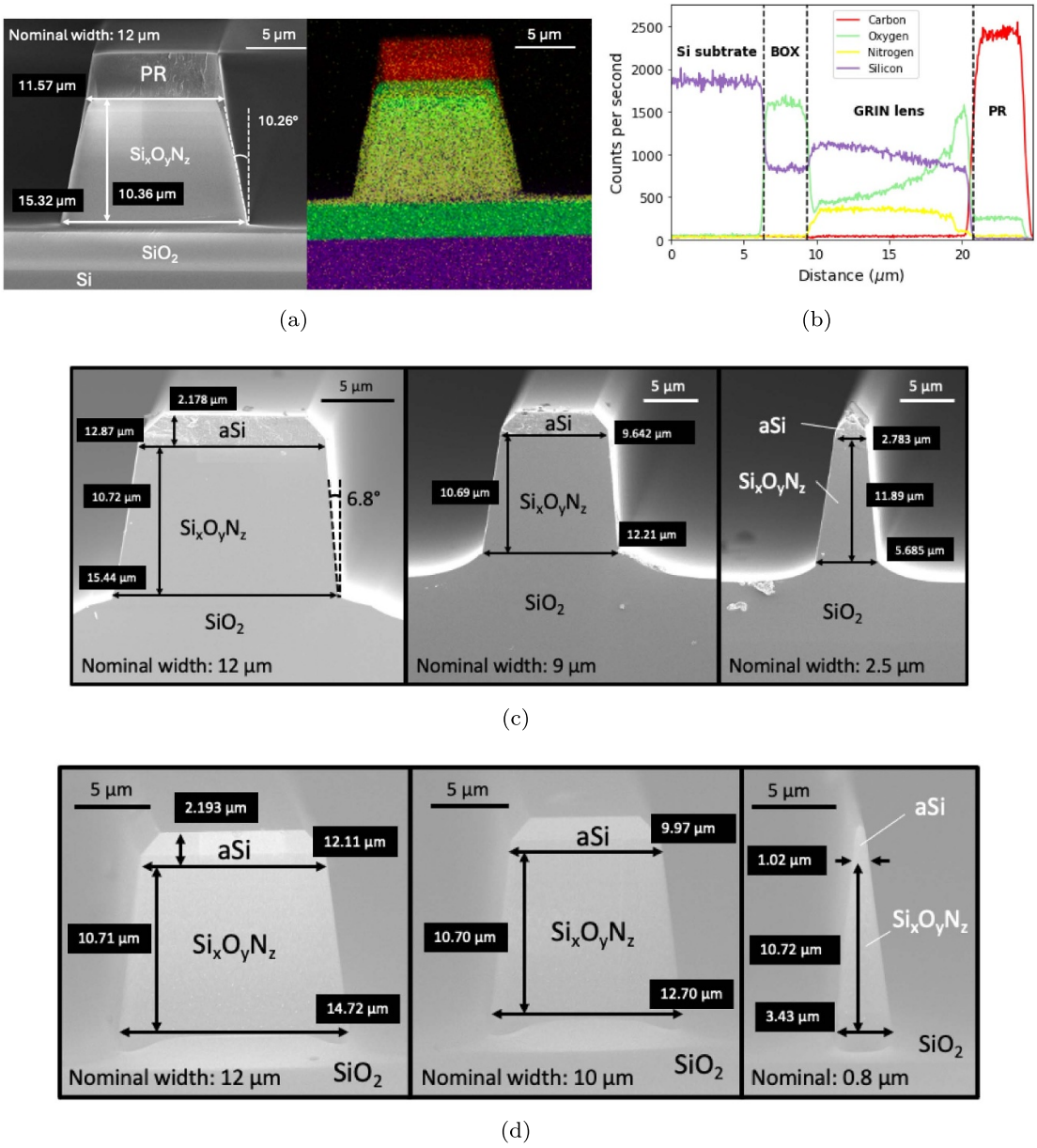

Figure 9. Experimental data showing fabrication of the GRIN lens. In (a) a cross sectional SEM image alongside a 2D EDS map are shown for a GRIN lens test sample which used a photoresist mask only. In (c) cross sectional SEM images for a GRIN lens test sample which successfully EBL to pattern the aSi hard mask and GRIN stack on a fused silica substrate. In (d) SEM images show the GRIN lens with the correct dimensions down to 1 μm following CHF_3 etching.

perfectly matched, as depicted in figures 3(c) and 4(c). This is due to the fact that the output waveguide layer and the bottom layer of the GRIN lens are the same. A GRIN coupler which can separate the GRIN lens profile (including refractive indices and layer thicknesses) from the output waveguide profile, specifically by having a higher index for the bottom layer (and thus a higher vertical confinement), may result in a higher coupling efficiency as described in [50]. However, obtaining a different refractive index and thickness for the output waveguide and the bottom layer of the GRIN lens increases the fabrication difficulty significantly, so it was not simulated in this study.

5.1. Effect of lens radius and GRIN length

The wide design and fabrication tolerance with respect to r and L as depicted by figures 3(a) and 4(a) can be explained by the the total GRIN focal length remaining approximately equal within the 1 dB coupling loss contour. As the lens radius increases, ℓ decreases, and thus the length of the tapered section of the GRIN, L, must increase to achieve the same total GRIN length equal to $\ell + L$. As the lens radius continues to increase, the GRIN facet becomes increasingly flat. When the GRIN coupler is flat, the horizontal confinement becomes entirely due to the tapered nature of the GRIN, whose length is

determined by the focal length. Because the GRIN taper is only 20–30 μm long and thus non-adiabatic, the coupling efficiency decreases, as described by the data for a 100 μm lens radius in figures 3(a) and 4(a). In other words, the use of a lens allows for independent control of the horizontal and vertical confinement which results in a higher coupling efficiency.

5.2. Effect of wavelength dependence on GRIN coupler performance

Another aspect to explain is the wavelength response of the chipt-to-chip and fiber-to-chip coupler. In the O, C, and L-bands (i.e. from approximately 1260–1640 nm), the traditional wavelength regime for data- and tele-communications applications, the coupling response for the chip-to-chip coupler is flat while the fiber-to-chip coupler showed a very slight decrease in coupling efficiency from 1280 nm to 1640 nm based on figures 6(a) and 8(c). The improvement with decreasing wavelength can be attributed to the fiber MFD more closely matching the GRIN MFD for shorter wavelengths. The overall weak wavelength dependence highlights how the focal length of the GRIN lens is independent of wavelength. This is because the focal length depends on the ratio between n_H and n_L and the thickness T, as described in section 2 and by equation (2), which remain approximately constant across the infrared spectrum for SiON films. An identical argument can be made for the chip-to-chip coupler, which sees a nearly negligible wavelength dependency from 1260–1640 nm. Similarly, the SOI and SiN_x evanescent couplers also demonstrate a relatively low wavelength dependence from 1280–1640 nm as evidenced by figure 6(a).

Outside of this wavelength window, the coupling loss remains low (<3 dB) even for wavelengths in the visible or into the mid-IR, as evidenced by figures 8(c) and (d). There are several factors which begin to limit the coupling efficiency when operating in these regimes, including material absorption, multimode propagation, and excessively large evanescent fields. In particular, when coupling to an SOI waveguide, the Si begins to absorb below approximately 1000 nm wavelength, leading to an exponential increase in coupling loss [47]. For coupling to an 220 nm thick SiN_x waveguide, it is the fact that below approximately 1 μm wavelength the waveguide begins to support multiple higher order modes which light is coupled into, leading to a decrease in simulated coupling efficiency through the evanescent coupler. In the case of coupling to SiON, it has a wider transparency window and a lower refractive index, meaning that it is able to maintain a lower coupling loss (<2 dB) when operating at wavelengths as low as 600 nm. When considering operation at longer wavelengths (>2 μm), coupling loss begins to increase significantly in the case of SOI and SiN_x as the optical supermode in the overlapped taper section interacts with the discrete tip due an excessively large evanescent field between the waveguides [37]. This effect is more pronounced in the SOI due its higher refractive index, thus increasing coupling loss in this regime compared to the SiN_x. Even with this increase in coupling loss, when coupling to SiN_x the 1 dB bandwidth extends to an upper limit wavelength of 2257 nm. Likewise, the coupling loss in the SiON case increases for these longer wavelengths as well, but the 1 dB bandwidth extends to an upper limit wavelength of 2360 nm and the 3 dB bandwidth extends to wavelengths $> 3\,\mu$m (not shown in figure 8(d)).

5.3. Effect of epoxy and layer refractive index variation

While the GRIN coupler demonstrated a wide 1 dB tolerance to epoxy refractive index changes of approximately $\pm$ 0.1 from the initial value of $\sim$ 1.44, there is a clear increase in coupling loss for refractive indices $<$ 1.3 or $>$ 1.5. For epoxy refractive indices $>$ 1.5, the epoxy begins to become a higher index than n_L, the lowest refractive index layers of the GRIN. For layers which have a lower refractive index than the epoxy refractive index, they effectively become part of the cladding and no longer contribute to GRIN lensing, causing n_L/n_H to approach unity and $\alpha \to 0$ according the equation (2). The GRIN focal length effectively increases and coupling loss increases as a result. An analogous argument can be made for indices $<$ 1.3 - n_L/n_H effectively increases causing α to increase (and the GRIN period to decrease) causing additional coupling losses.

The introduction of random fluctuations on the layer refractive index also induced additional chip-to-chip coupling losses as evidenced by figures 6(d) and (e). The coupler was more sensitive to index fluctuations compared to thickness fluctuations since the GRIN lens period is directly correlated to the refractive index profile (it is proportional to α^{-1}) and correlated indirectly with layer thickness (t_{layer}) through the total thickness T ($\alpha \propto T^{-2}$). The 1 dB tolerance for refractive index error per layer was $\sim \pm$ 1% based on figure 6(e). This equates to approximately $\pm$ 0.015–0.017 in terms of the refractive index control necessary during the PECVD process. While $\pm$ 1% seems like extremely tight control, data for similar processes such as inductively coupled plasma PVD has standard refractive index control of $<$

Table 2. Summary of loss contributions through GRIN fiber-to-chip, chip-to-chip coupler and evanescent coupler at 1550 nm and 1310 nm wavelengths for the TE mode.

Component	Loss (dB)			
Wavelength	1310 nm		1550 nm	
Final waveguide material	SOI	SiN_x	SOI	SiN_x
Fiber-to-chip coupler				
Single GRIN lens	0.46		0.64	
Evanescent coupler[a]	0.02	0.08	0.03	0.02
Total	**0.48**	**0.54**	**0.67**	**0.66**
Chip-to-chip coupler				
Two GRIN lenses	0.42		0.37	
Evanescent couplers[ab]	0.03	0.15	0.05	0.04
Total	**0.45**	**0.57**	**0.42**	**0.41**

[a] Assuming a 100 μm long adiabatic taper for SOI and SiN_x.

[b] Includes evanescent coupling loss at GRIN lens input and output (i.e. 2 evanescent couplers).

$\pm$ 0.3% over $>$ 75 wafers using commercially available tools [51]. On the other hand, the 2D chip-to-chip coupling loss was essentially unchanged by layer thickness errors as large as $\pm$ 20%, or roughly $\pm$ 200 nm.

5.4. Effect of refractive index on evanescent coupler taper length

The evanescent coupler design used in this study was described extensively in [18, 37] for SOI to SiN_x coupling. However, one point to elaborate on in is the improvement seen in SiN_x compared to SOI for the same adiabatic taper length as depicted by figure 5(b). This coupling efficiency improvement can be attributed to the lower refractive index of SiN_x compared to the SOI, which more closely matches that of the SiON. The lower refractive index means larger feature sizes can be used to achieve the same effective refractive index in SiN_x. Thus, these larger lateral feature sizes mean the shape of the mode in the SiN_x more closely matches that of the SiON prior to the mode entering the adiabatic region of the taper. Therefore, a faster transition can be used for SiON to SiN_x compared to SiON to SOI to achieve the same coupling loss.

6. Comparison to other types of chip-to-chip couplers

Using the updated data from figures 8(c) and (d), which includes the experimentally measured refractive index profiles for the SiON layers, the total coupling loss was compiled in table 2 for fiber-to-chip coupling from an SMF to SOI or SiN_x and for chip-to-chip coupling from SOI to SOI or SiN_x to SiN_x (or any combination thereof). From the data in the table, it can be see that the maximum fiber-to-chip coupling loss is 0.67 dB for SOI at 1550 nm, the maximum chip-to-chip coupling loss is 0.57 dB for SiN_x at 1310 nm, and the maximum combined fiber-to-chip and chip-to-chip loss is only 1.11 dB for SiN_x at 1310 nm. This data implies that the GRIN coupler design can potentially support optical fanout to Pbps optical I/O with a roughly 1 dB aggregate interfacial loss contribution to the total loss budget using the layout described by figure 1, especially if SiON waveguides are used at the interposer or package substrate level. Moreover, this value can be driven below 1 dB by using the optimized refractive index profiles for the SiON layers, as alluded to in section 4.1. By obtaining total insertion losses of $<$ 1 dB including the combined fiber-to-interposer and chip-to-interposer coupling loss, this coupler thus overcomes a critical IPSR-I challenge for interconnect packaging [10].

In order to evaluate the relevance of these results, we can compare them against similar designs for chip-to-chip optical couplers found in literature. A brief review of the performance metrics for alternate vertical couplers is presented in table 3 and in the radar plot found in figure 10(a). In comparing the values for coupling loss, alignment tolerance, and bandwidth associated with the GRIN structure from this study, our coupler stacks up well to peer innovations while overcoming several limitations associated with other designs. First, in terms of coupling loss, our GRIN chip-to-chip coupler displayed a coupling efficiency of approximately 92%, or 0.37 dB of loss, at 1550 nm wavelength. This is competitive compared to the other high performance couplers which also have coupling losses below 1 dB at 1550 nm. However, this coupler achieves the sub dB loss while simultaneously allowing for vertical chip-to-chip coupling gaps of $>$ 10 μm using entirely parallel fabrication processes and CMOS foundry compatible

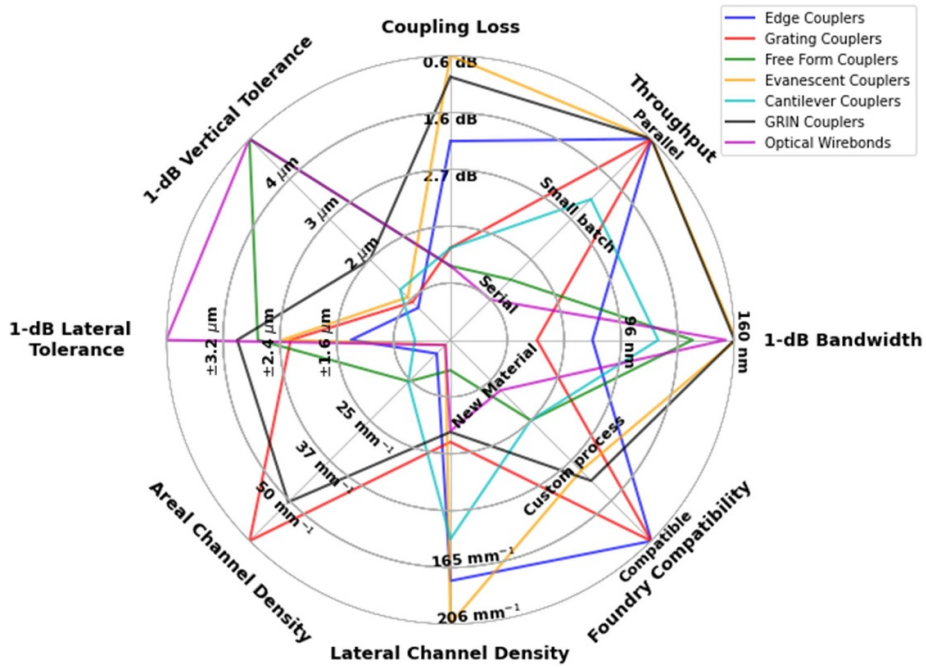

Figure 10. A radar plot comparing different chip-to-chip coupling strategies in silicon photonics in terms of performance metrics relevant to data- and tele-communications applications and scaling to high volume manufacturing.

toolsets. If we consider other couplers from table 3, those that are able to achieve vertical coupling gaps $> 10\,\mu$m rely on serial TPP processes for fabrication, while those using parallel processing have a maximum vertical coupling gap of only around $1\,\mu$m. Enabling a gap $> 10\,\mu$m is essential, because emerging state-of-the-art solder-based electrical μ-bumps [25, 26] and solderless Cu μ-pillar bumps [24] used for forming electrical connections after thermocompression bonding have been shown to achieve heights of $< 10\,\mu$m. In addition to the large vertical coupling gap, our widened translational alignment tolerances above $\pm$ 2.4 μm compare favorably to other evanescent, edge, or grating coupler designs which are typically less than $2\,\mu$m. A lateral alignment tolerance of $\pm$ 2.4 μm is wide enough to use current automated pick-and-place die bonders for passive assembly in high volume manufacturing [27–29].

Another aspect to compare is the 1 dB bandwidth, and to do this it is important to understand the limitations of other designs. In general, grating couplers are typically bandwidth limited (e.g. 21 nm [52]) due to the need to fulfill the Bragg condition for efficient coupling [36]. Evanescent couplers, while demonstrating wide bandwidths of 160–400 nm [18, 53], can become bandwidth limited due to the decrease in MFD size at shorter wavelengths (say, outside of the datacom or telecom regime), impacting coupling if the distance between waveguides is on the micron scale. Free form designs can achieve operation into the visible [54], but are fabrication limited as mentioned above. Finally, prior edge coupling designs have demonstrated broadband operation in the datacom or telecom regime (120 nm [55]), but have low allowable vertical coupling gaps of $< \pm 0.5\,\mu$m and have been limited to the edge facet of the chip. This GRIN based design has simulated 1 dB bandwidths of > 800 nm for SOI-to-SOI, $>$ 1300 nm for SiN_x-to-SiN_x, and > 1500 nm for SiON-to-SiON. Using table 3, it can be seen that prior SiN_x-to-SiN_x and SOI-to-SOI designs have a maximum simulated or measured bandwidth of 400 nm and 21 nm, respectively. Thus, this design provides a 3 fold and 40 fold bandwidth improvement for SiN_x-to-SiN_x and SOI-to-SOI chip-to-chip coupling, respectively. By extending from the visible to the mid-IR wavelength regime, this coupler meets the IPSR-I bandwidth standard target for 2040 mentioned in section 1—providing a solution for datacenter transceivers and emerging applications in quantum photonics and biochemical sensing.

Furthermore, the performance advantages of this design would not be practically useful unless the design could be fabricated, packaged, and assembled in method scalable to high volume manufacturing. This study demonstrated the feasibility of fabricating monolithic, thick GRIN structures approximately $11\,\mu$m in total height using standard, controlled microelectronics foundry BEOL processes and materials. This is contrasted by couplers which are fabricated using TPP techniques, a CMOS foundry incompatible process with significantly lower throughput due to the sequential patterning of optical components with repeated exposures. The parallel, foundry compatible processes developed here also showed the coupler

Table 3. Summary of recent examples of chip-to-chip optical coupling schemes. This list does not include all chip-to-chip coupling schemes and is only meant to yield a general idea of competing designs and performance. Blue shaded cells represent where only simulation data was available. For the coupler presented in this work, experimental coupling results have not been measured yet because additional fabrication processes which have been separately developed need to be integrated into the GRIN process flow to make it complete. Specifically, as mentioned in figure 7, these processes include the deep dry etching to form glass edge facets and the flip-chip pick-and-place sequence using UV curable epoxy (developed originally for flip-chip evanescent coupling [18]). Additionally, chemical mechanical polishing to planarize the cladding layer and allow for intra-chip evanescent coupling needs to be integrated (previously demonstrated with an intra-layer evanescent coupler using the same CMOS foundry compatible fabrication equipment used in this work [44]).

			1 dB Misalignment Tolerance (μm)				
Package	Coupler	CL^{1}_{1550}(dB)	Lateral	Vertical	1 dB Bandwidth (nm)	L × W (μm)	reference
InP to SOI	Edge	0.25	± 0.7	± 0.5	120 (1510–1630)	75 × 0.4	[55]
InP to SOI	Edge	0.9	± 1.7	± 0.5	120 (1510–1630)	250 × 0.4	[55]
SOI to SOI	Photonic wirebond	1.6	/	/	> 300 (1280–1580)	2 (W)	[58]
SOI to polymer	Evanescent	1.25/0.5 (TE/TM) < 0.5 (TE/TM)	± 2 /	/	[b]± 60 (1310) ± 70 (1550)	1500 × 6.5	[59]
Polymer to polymer	Free form	0.22 (TE) 0.25 (TM)	± 1.3	35	± 200 (850)	10 × 30	[54]
SOI to polymer	Evanescent	0.2	> ± 5 ± 1.5°(yaw)	0.5	± 100 (1550)	200 × 15.3	[60]
SOI to IOX	Evanescent	< 1 (TE/TM)	± 4	3	± 30 (1550)	1500 × 12	[57]
Si_3N_4 to IOX	Evanescent	0.7	> ± 4	< 2	75 (1515–1590)	2000 × 11	[14]
Si_3N_4 to Si_3N_4	Evanescent	0.54	< ± 2	< 0.8	400 (1200–1600)	1000 × 3	[53]
SOI to SOI	Grating	0.94	/	/	21 (1539–1560)	20 × 20	[52]
Si_3N_4 to SOI	Evanescent	0.39 (TE)	± 1.56	> 1.1	160 (1480–1640)	520 × 1	[18]
SiON to SiON	**GRIN**	**0.37 (TE) 0.49 (TM)**	**± 2.66**	**± 2.45 11 (rise)**	**1562 (798–2360)**	**29.6 × 11**	**this work**
SiN_x to SiN_x	**GRIN**	**0.41 (TE) 0.69 (TM)**	**± 2.66**	**± 2.45 11 (rise)**	**1361 (896–2257)**	**129.6 × 11**	**this work**
SOI to SOI	**GRIN**	**0.42 (TE) 0.59 (TM)**	**± 2.66**	**± 2.45 11 (rise)**	**888 (1122–2010)**	**139.6 × 11**	**this work**

[1] CL_{1550} = coupling loss at 1550 nm wavelength (except for entries from [59] and [54] which shows data for 1310 nm and 850 nm, respectively).

can be fabricated on multiple different types of substrates (silicon and glass), without using any metal hard or liftoff masks, and without having any process temperature be > 350 °C. Other GRIN structure designs have only been proposed for fiber-to-chip coupling (not chip-to-chip coupling), and of those designs they are either roughly half the thickness [19, 20] or require metal hard masks or metal liftoff films [21–23]. In terms of packaging, the simulations performed here also showed wide tolerances for critical packaging materials such as the UV curable epoxy, with < 1 dB coupling loss possible for refractive indices between 1.3 and 1.5. An ultra-wide refractive index tolerance of 0.2 is critical for two reasons, the first being that it enables compatibility with a wide range of commercially available UV-curable

epoxies [56]. The second advantage is that it ensures that the coupler performance will remain stable as the refractive index shifts during operation either due to the package heating and cooling, or due to the possibility of multiple wavelengths being present in a single channel as a result of using wavelength division multiplexing. For context, transceiver and interconnect devices in switch packages must maintain stable performance for temperatures up to 85 °C without additional cooling according to the targets for the next 5 years set by the IPSR-I committee [10]. In comparison, other couplers in table 3, including evanescent couplers and free form couplers, often have stringent requirements on the cladding refractive index (for some this tolerance can be < 0.001 [57]). Moreover, because the coupler is fabricated using standard silicon based materials, it also means the device is reflow temperature compatible and not subject to the same mechanical, thermal, or humidity based reliability problems which may arise for the polymer based structures made using TPP.

When it comes to footprint and pitch, the $< 30\,\mu$m length and $11\,\mu$m width of the SiON GRIN lens makes it compact, especially compared to some evanescent designs requiring greater than 1 mm in length, over 30 times as long, to achieve a lower than $\pm\ 2\,\mu$m lateral tolerance. Even in the case of coupling to SOI or SiN_x, or any combination thereof, the total length is $< 140\,\mu$m including the GRIN lens and the evanescent coupler. The only other couplers with a similar footprint again require TPP, limiting their scalability in high volume manufacturing. Finally, because the GRIN coupler width was $11\,\mu$m and the optical mode was highly confined within the GRIN, even during expansion, our lateral pitch can be made significantly compared to free form couplers which expand the mode to $> 100\,\mu$m in diameter. A finer I/O pitch directly equates to a higher I/O density along the shoreline of the Si PIC, and thus a higher possible data capacity. For example, a coupler pitch of $20\,\mu$m equates to an I/O density of 50 couplers/mm whereas a fiber array pitch of $127\,\mu$m equates to an I/O density of only about 8 fibers/mm; thus, the GRIN coupler could provide a 6 times improvement in connection density. This connection density can be further increased by placing the GRIN couplers in a 2D array format along the PIC shoreline, potentially enabling final waveguide pitches (i.e. the waveguide pitch output from the 2D array) down to $10\,\mu$m or a linear I/O density of 100 couplers/mm—over an order of magnitude increase compared to direct fiber-to-chip V-groove based connections. Thus, our coupler may provide more rapid, less costly scaling to high volume manufacturing applications requiring high density integration which is especially crucial in the context of scaling to greater than 1 Pbps datacom or telecom co-packaged systems.

7. Conclusion

In this study, the design and simulation of a novel GRIN coupler for chip-to-chip coupling was presented and demonstrated to achieve sub-dB coupling loss with broadband and alignment tolerant operation. This high performance can be achieved while coupling over a significant vertical chip-to-chip gap of $> 10\,\mu$m. In terms of adoption to high volume manufacturing, the coupler can be fabricated during, or after the completion of, typical BEOL steps using standard, low-temperature foundry compatible materials and processes, and can be used to connect waveguides standard to silicon photonic PDKs. The coupler can be fabricated at the wafer or panel level using parallel, standard thin film fabrication methods, and can be packaged using passive assembly with automated flip-chip die bonders. When placed at a $20\,\mu$m pitch within a 2D array, this coupler offers a density of 100 couplers/mm, a $12\times$ improvement over systems directly connecting fibers to Si-PICs. In essence, this coupler will help enable the mass parallelization and cost-effective scaling of optical I/O in co-packaged optics systems.

Data availability statement

The data cannot be made publicly available upon publication because they contain commercially sensitive information. The data that support the findings of this study are available upon reasonable request from the authors.

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Conflicts of interest

The authors declare no conflicts of interest.

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