A Multi-Level Pseudo-Resonant Switched-Capacitor Gate Drive IC with Sub-Nanosecond Step Tuning

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***Abstract*—This work presents a highly-integrated switched-capacitor gate drive integrated circuit (IC) that can provide tunable multi-step driving of the gate voltage waveform. By using flying capacitors to deliver and recovery the gate energy, hard-charging loss can be reduced by roughly the number of steps of the SC converter. The tuned multi-level operation can also leverage parasitic gate-loop inductance to further reduce gate drive loss while preventing ringing and overshoot of the gate voltage. The proposed driver, implemented in 130nm SOI CMOS, achieves per-step timing resolution below 50 ps and multiplies the single 1.0 V power supply to $\sim$5 V_{pp}, suitable for a range of low-R_{DSon} GaN and silicon power devices. Measured results show the design can achieve comparable gate and drain slew rates to conventional gate drivers while reducing power consumption by 2-7$\times$ for a range of loop impedance and gate charge.**

***Index Terms*—Gate Driver, Switched-Capacitor, DC-DC converter, Multi-Level, Resonant Converter, Domino Logic.**

I. Introduction

GATE driving is a critical function required for power semiconductor devices including field-effect transistors (FETs) that involves reliably and rapidly slewing the gate to the desired on or off voltage while minimizing detrimental transient effects (ringing, over-voltage, off-state holding, and electromagnetic interference, etc) [2]–[5]. Recent years have seen major advances in power semiconductor devices including wide-bandgap technologies (*i.e.* gallium nitride GaN and silicon carbide SiC) which has led to better device figures-of-merit, higher breakdown voltage, and higher frequency operation. However, gate driving loss is still significant and limits overall power conversion efficiency [6]–[8]. Modern gate drive circuits are therefore challenged to provide gate energy efficiently, but also adapt to different operating conditions and parasitic elements in the gate-drive loop.

Fig. 1 shows a representative scenario where a power field effect transistor (FET) is driven through a gate loop impedance Z_g, where L_g represents the parasitic loop inductance and R_g represents the overall loop resistance including resistance of the gate driver, interconnect, and power FET internal gate resistance. When turning on, the gate driver delivers (reactive) energy of $E_{gg} \approx Q_{gg}V_{gg}$, where V_{gg} is the gate-drive supply voltage and Q_{gg} represents the total gate charge needed to turn on the device, which is commonly expressed as:

$$Q_{gg} \approx C_{gs}\Delta V_{gs} + C_{gd}\Delta V_{gd}. \tag{1}$$

To turn off the device, the gate driver discharges gate capacitance, sinking the stored reactive gate energy. Thus most traditional gate drivers incur average power loss of

$$P_{gg} \approx Q_{gg}V_{gg}f_{sw}, \tag{2}$$

where f_{sw} is the switching frequency.

This perspective highlights that gate drive power is typically dominated by reactive energy. Most conventional gate drivers are effectively hard-switching, with gate energy provided through a switched resistive or current source path [3]. In most examples in the literature, hard-switching gate-drive power is assumed to be an intrinsic loss mechanism and a major component of frequency-dependent switching losses [9]–[11]. Gate-drive power is often traded off against resistive conduction loss when choosing or sizing power devices [10]. With device sizes optimized to minimize overall power loss,

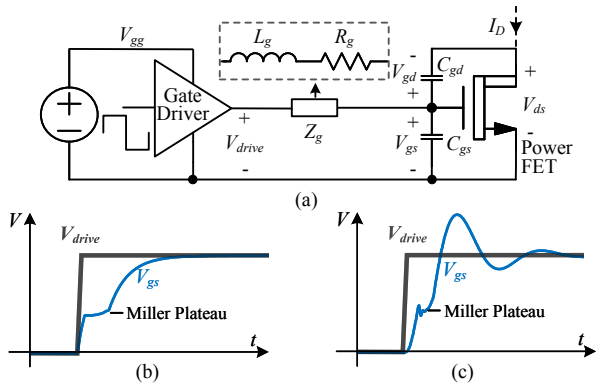

Fig. 1. Conventional hard-switching gate driver, (a) schematic with gate-loop parasitics, (b) gate voltage with resistive-dominant (overdamped) impedance, (c) gate voltage with inductive-dominant (underdamped) impedance.

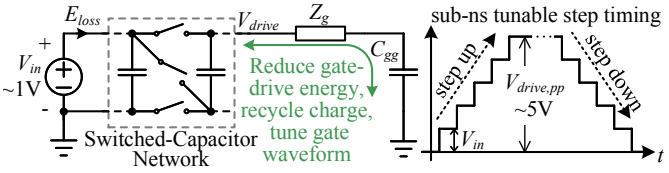

Fig. 2. Conceptual schematic of the proposed switched-capacitor gate driver.

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gate drive power may approach half of the total loss, and is therefore a major limitation on efficiency [11].

Fig. 1 shows example gate waveforms highlighting that there are a range of resistively dominated (overdamped) and inductively dominated (underdamped) driving scenarios that can affect timing, reliability, electromagnetic interference (EMI), and other aspects of the gate drive design [5], [12]. The drain-source voltage swing impacts Miller charge and is a key factor that also determines power loss and EMI. To reduce gate drive power, there are examples of resonant or soft-charging gate drivers that use an inductive impedance to efficiently charge the gate capacitance [2]–[4], [13]–[19]. As discussed in [2], these may use an explicit inductor or use the parasitic gate-source loop inductance. Challenges in the approach include the need for a relatively large inductance or quality factor (Q) to efficiently deliver and recover gate energy. With a conventional approach, it is also difficult to tune the gate or drain slew rate when using resonant driving which may limit the power savings and EMI performance [20].

This work presents a switched-capacitor (SC) based gate driver that can address the challenges discussed above. Illustrated conceptually in Fig. 2, the approach uses a network of flying capacitors that are sequentially switched to provide gate charge in small increments. Assuming a predominantly resistive gate loop, the smaller gate voltage steps reduce overall hard-switching loss. When the gate voltage is discharged, the flying capacitors recover a portion of the energy stored in the gate dielectric, reducing overall power consumption. In previous work, this process has been described as pseudo-resonant [21] or pseudo-adiabatic [22] because energy loss is reduced and partially recovered, with overall power savings going with the number of switching steps.

However, compared to [22], [23], gate driving requires over 1000× faster switching speeds and fine grain control of the gate waveform. To address the need for fast rise and fall time as well as tunability and control of gate signals, this work uses a high-speed delay structure with sub-ns resolution to adjust the duration of each switching step. Semiconductor devices with predominantly resistive gate-source loops can be operated in slow-switching limit (SSL) and fast-switching limit (FSL) regimes [24], trading speed for power savings. For scenarios with modest (nH-range) loop inductance, the tuned switching sequence provides an additional degree of freedom to use resonant gate driving to save power while also reducing or eliminating inductive gate-source ringing. The 130nm silicon-on-insulator (SOI) integrated circuit (IC) requires only a single low-voltage CMOS-compatible supply; the SC stage multiplies this supply to generate the gate drive voltage.

Compared to [1], this paper expands on the topology description and modeling in Sections II and III including limitations of finite flying capacitance, timing of the switching waveform to resonate with gate loop inductance, and more details on power loss in slow- and fast-switching limit operation. Section IV presents more details of circuit implementation for the delay and timing circuitry. In section V we provide a discussion of test parasitics and how those affect high dV/dt gate and drain voltage measurements; with slight measurement modifications we show cleaner measured results than previous

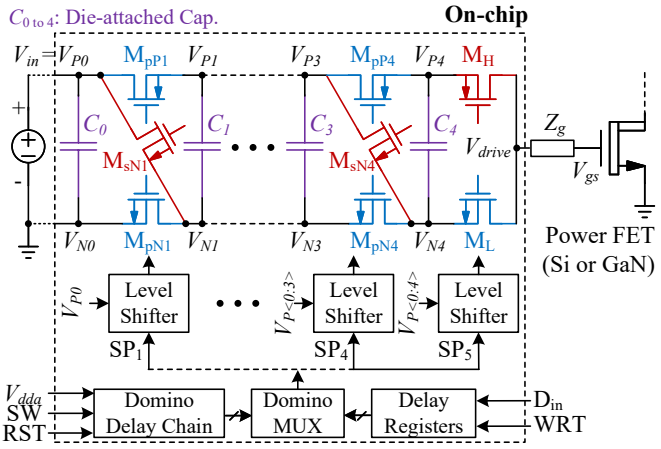


Fig. 3. Top level schematic of the proposed SC gate driver.

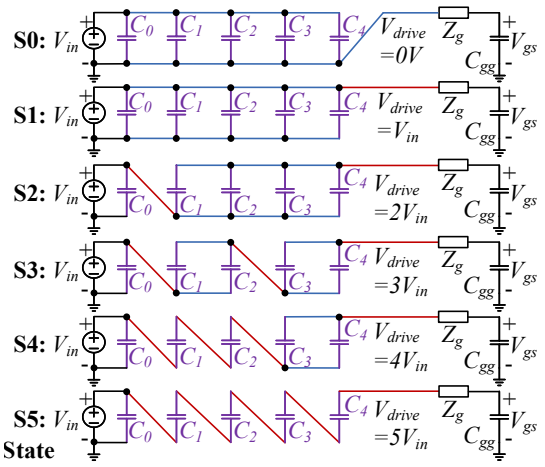


Fig. 4. The equivalent circuit and sequence of each switching state.

work [1] for the same scenarios. We provide a more comprehensive review of the literature for both integrated and discrete solutions including resonant gate drivers.

Going forward we will use the metric power reduction factor (PRF) to quantify the energy savings of the proposed gate drive circuit compared to a conventional hard switching driver:

$$PRF = \frac{P_{HS}}{P_{supply}} \approx \frac{Q_{gg} V_{gg} f_{sw}}{P_{supply}}, \tag{3}$$

where P_{HS} is the power consumption of an ideal hard-switching driver and P_{supply} is the power consumption of the gate driver under evaluation. Compared to previous metrics [14], (3) provides a standard benchmark to compare solutions either by knowing the load condition (gate charge) or having a hard-switching reference design [4]. In past work, conventional gate drivers have PRF ranging from 0.1 to 0.3 [5], [12], [25]–[29]. Past work with resonant gate drivers has demonstrated PRF from 2-6 depending on inductor size and quality factor [2]–[4], [14]. Next we will describe the topology and operation of the proposed gate driver as well as tradeoffs, challenges, and opportunities to improve PRF and other performance metrics.

II. Topology Overview

Fig. 3 shows a high-level schematic of the proposed gate driver. The switch network uses five switching cells that together represent a *reconfigurable series-parallel (SP) SC driver*. Each switching cell controls the series or parallel configuration of an associated capacitor C_{0-4}, where C_0 is an input bypass capacitor and the rest are flying capacitors. In each cell, a series switch M_{s*} or M_H (red) is complementary with respective parallel switch(es) M_{p*} and M_L (blue). A fast domino delay-line and multiplexer is used to control the independent state, switching sequence, and timing of the different switching cells, interfaced through a low-latency level shifter. The overall circuit runs on a low-voltage supply $V_{in} \sim 1\,V$ and multiplies the gate voltage to $\sim 5\,V_{in}$

The switching sequence used in this work is shown in Fig. 4. Here, switching states $S0-S5$ correspond to the configuration of individual switching cells and equivalent circuits. In state $S0$, all parallel switches are on and V_{drive} is held to $0\,V$; all capacitors are in parallel, charged to V_{in}. In this state, the power device is off with V_{gs} held to zero through NMOS devices $M_L \ldots M_{pN1}$. All of these devices are low-voltage rated and have combined pull-down resistance $R_{PD} \approx 0.1\,\Omega$ to strongly hold the gate low during the off state.

In $S1$, M_H is on, connecting V_{drive} to V_{in}. In $S2$, M_{sN1} turns on, charging V_{drive} to $2\,V_{in}$. In $S3$, M_{sN3} turns on, charging V_{drive} to $3\,V_{in}$. This process repeats until the gate is fully charged to $V_{gs} \approx 5\,V_{in}$. To turn off (discharge) the gate, the reverse sequence is used, with the gate voltage being sequentially stepped down and gate charge flowing back into the flying capacitor network. Following the discussion in related work [21], assuming linear capacitance C_{gg} and large flying capacitance in SSL operation, the ideal power savings of the switched-capacitor gate driver go as

$$PRF_{ideal} = \frac{C_{gg} V_{gs,pp}^2 f_{sw}}{P_{in}} \approx 5, \tag{4}$$

where, similar to (3), $V_{gs,pp}$ represents the peak-peak gate voltage. Certain non-idealities can impact PRF, and among those are nonlinear capacitance and charge-flow (*i.e.* Miller) effects, which will be discussed in the next section, and the finite value of flying capacitance as compared to load capacitance C_{gg}. To maximize performance, the proposed switching sequence approximates the 'binary switching' concept from [30], which maximizes the equivalent capacitance of the SC driver as presented to gate capacitance C_{gg} across the switching interval. This optimizes capacitor utilization, minimizes voltage droop at the output, ensures uniform voltage stress, and matches level-shifter timing among switching cells in the converter. Even with the optimum switching sequence, the ratio of flying capacitance C_f to load capacitance C_{gg} can still impact the PRF. As shown in Fig. 5, for the switching sequence in Fig. 4, PRF falls rapidly for $C_f/C_{gg} < 10$; in this work, a ratio of $C_f/C_{gg} > 50$ is used such that the ideal PRF > 4.9. However, to drive discrete power FETs with nF-range capacitance (10's of nC gate charge), the use of on-chip capacitance is impractical, so the design uses high-density small form factor 015008 footprint $0.125\,\text{mm}^2$ die-attached multilayer ceramic capacitors.

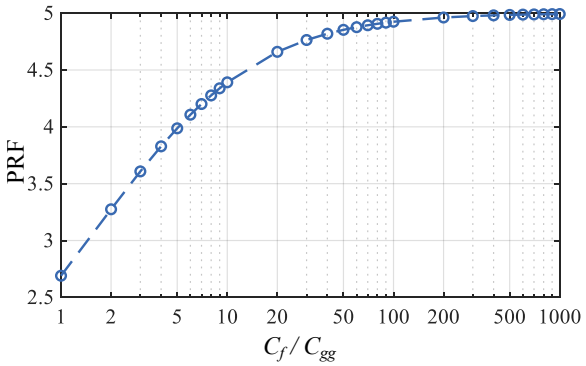


Fig. 5. Power reduction factor (PRF) versus flying capacitance to load capacitance ratio C_f/C_{gg} in SSL operation.

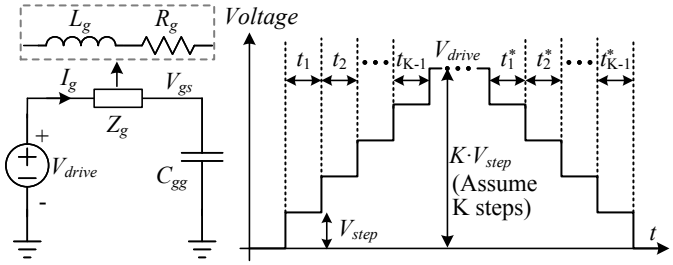


Fig. 6. Simplified circuit model and tunable gate-drive voltage waveform.

III. Multi-mode Operation for Different Loop Impedances

This section will analyze and discuss the opportunities for tunable multi-mode driving that can tradeoff speed for power savings, and use stray inductance to achieve fast and reliable resonant driving. To analyze different options for gate waveform timing, we will assume a large ratio of C_f/C_{gg}. As shown in Fig. 6, this allows us to model the circuit as a multi-level voltage source with variable timing increments. Illustrated in Fig. 6, each of the step-up timing intervals t_1 to t_{k-1} and step-down timing intervals t_1^* to t_{k-1}^* are individually and separately tunable. In this case, we are interested in the duration of timing increments and how these affect performance for different gate impedance scenarios; however, we will primarily discuss the step-up (power device turn-on) scenario to illustrate the concept. We assume gate impedance Z_g simplified as a lumped resistance R_g in series with inductance L_g. The voltage source has K voltage steps, corresponding to K switching cells.

When $K = 1$, it models a conventional hard-switching driver where the drive voltage can be expressed as

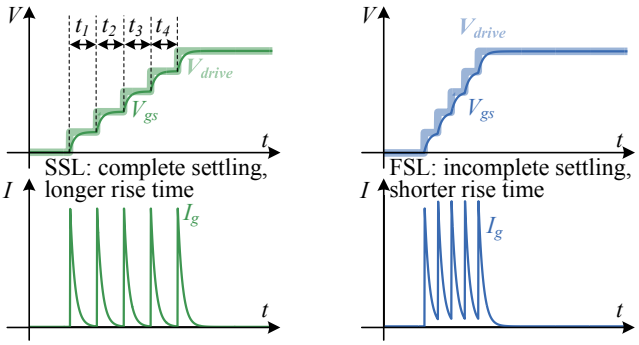
$$V_{drive} = V_{gg} U(t), \tag{5}$$

where $U(t)$ is the unit step function. Assuming a resistively dominated (overdamped) loop, the gate voltage goes as

$$V_{gs} = V_{gg}(1 - e^{-\frac{t}{R_g C_{gg}}}). \tag{6}$$

For an underdamped loop, the gate voltage is expressed as

$$V_{gs} = V_{gg}(1 - e^{-\frac{R_g}{2L_g}t}[cos(\omega_0 t) + \frac{R_g}{2L_g\omega_0} sin(\omega_0 t)]), \tag{7}$$



(a) Slow switching limit (SSL) (b) Fast switching limit (FSL)

Fig. 7. Slow- and fast-switching limit operation with overdamped gate loop.

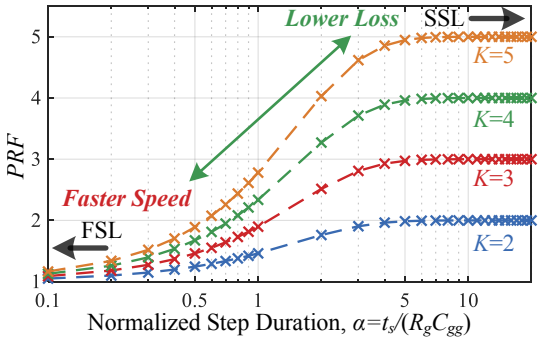


Fig. 8. The PRF of the proposed SC gate driver with overdamped gate driving loop versus normalized step duration for different number of steps.

where $\omega_0 = \sqrt{\frac{1}{L_g C_{gg}} - (\frac{R_g}{2L_g})^2}$ is the natural frequency of the gate driving loop. As illustrated conceptually in Fig. 1, in certain scenarios, unavoidable parasitic inductance including wire-bond, packaging, or PCB trace inductance, can resonant with the gate capacitance, leading to overshoot and ringing, which can degrade reliability and EMI of the device.

A. Overdamped Gate Driving Loop

For the SC driver stage, assuming equal step duration, t_s, The driving voltage can be expressed as:

$$V_{drive} = V_{step} \sum_{i=0}^{K-1} U(t - i \cdot t_s). \tag{8}$$

In an overdamped scenario, the duration of the switching states t_s relates to different operation in slow- and fast-switching regimes (SSL and FSL). As shown in Fig. 7a, for long t_s the voltage fully settles and gate current goes to zero; otherwise, the SC gate driver runs in FSL, as shown in Fig. 7b corresponding to incomplete settling in each timing interval. The corresponding gate voltage and current follow as

$$V_{gs} = V_{step} \sum_{i=0}^{K-1} (1 - e^{-\frac{t - i \cdot t_s}{R_g C_{gg}}}) U(t - i \cdot t_s), \tag{9}$$

$$I_g = \frac{V_{step}}{R_g} \sum_{i=0}^{K-1} e^{-\frac{t - i \cdot t_s}{R_g C_{gg}}} U(t - i \cdot t_s). \tag{10}$$

Assuming linear capacitance and ignoring quiescent and operational bias power, without loss of conceptual generality, across both phases, the total loss (power drawn from the supply) of the proposed SC gate driver goes as

$$P_{supply} = C_{gg} V_{step}^2 f_{sw} \cdot \beta, \tag{11}$$

where

$$\beta = \sum_{m=1}^{K-1} [(\sum_{i=0}^{m-1} e^{i\alpha})^2 (e^{-2\alpha(m-1)} - e^{-2\alpha m})] + (\sum_{i=0}^{K-1} e^{i\alpha})^2 e^{-2\alpha(K-1)}. \tag{12}$$

and

$$\alpha = \frac{t_s}{R_g C_{gg}}. \tag{13}$$

Compared to (4), this gives a more accurate expression of the power savings (PRF) that depends on the gate rise and fall time with respect to the actual gate-voltage time constant which can be expressed as

$$PRF = \frac{K^2}{\beta}. \tag{14}$$

The impact of step duration to the PRF of the SC gate driver with an overdamped gate driving loop is shown in Fig. 8, which shows the tradeoffs between speed and power loss. This can be compared to a conventional hard-switching driver to assess realistic power savings for given timing constraints. For the same R_g, a traditional single-step hard-switching driver will always have the shortest rise time. However, the multi-step driver can achieve significant power savings with only modest increases in rise-time. Also, the modified series-parallel design in Fig. 3 can be implemented with all low-voltage CMOS devices which can have low resistance. This allows the design to operate with low R_g while still modulating the rise time through digital control of the switching waveform.

B. Underdamped Gate Driving Loop

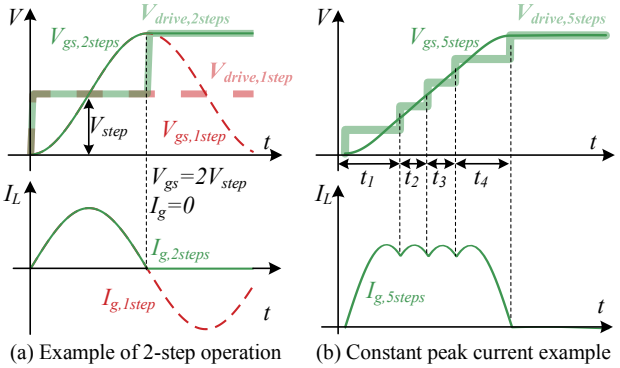
In scenarios where inductance dominates the loop impedance, another advantage of the proposed SC gate driver is that, by tuning the step timing, the circuit can provide additional degrees of freedom to modulate the gate current (inductor current). This allows a tunable controller to shape the gate voltage waveform to achieve zero or minimum overshoot while also leveraging the inductor to save additional energy.

For a high-Q scenario where R_g can be ignored, the state transition expression from step $k-1$ to step k is

$$I_{g,k}(t) = I_{k-1} cos(\omega_0 t) + C_{gg} \omega_0 (k V_{step} - V_{k-1}) sin(\omega_0 t), \tag{15}$$

$$V_{gs,k}(t) = k V_{step} - (k V_{step} - V_{gs,k-1}) cos(\omega_0 t) + L_g \omega_0 I_{k-1} sin(\omega_0 t), \tag{16}$$

where I_{k-1} and V_{k-1} is the gate current and voltage at the end of step $k-1$ respectively. To ensure zero overshoot at the



(a) Example of 2-step operation (b) Constant peak current example

Fig. 9. Example voltage and current waveforms for resonant operation.

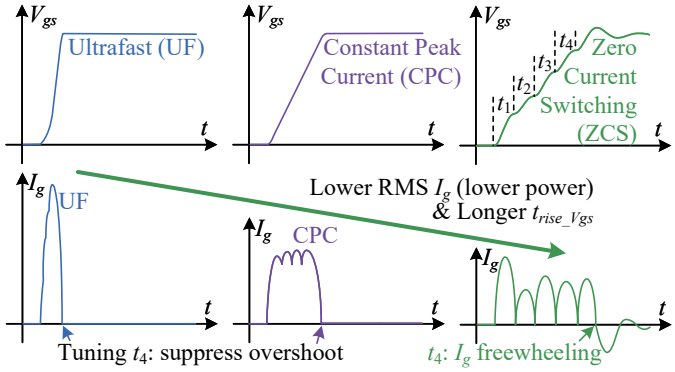


Fig. 10. Representative multi-mode operation of the proposed SC gate driver for underdamped loop.

end of the last switching step, the condition that gate driver needs to achieve at the end of the next-to-last step is that:

$$I_{K-1} = 0, V_{K-1} = kV_{step}. \tag{17}$$

Fig. 9a provides an example of 2-step (*i.e.* 3-level) operation ($K = 2$). With 2 steps, if the gate driver switches to the second step when $t = \pi/\omega_0$, where $I_g = 0$ and $V_{gs} = 2V_{step}$, there is no overshoot of the gate voltage. This can be appreciated as a zero-current and zero-voltage switching process that leverages the loop inductance to resonate with the gate capacitance. In ideal circumstances this can be a lossless process, yet allows the gate to be driven without overshoot or ringing.

Expanding and generalizing the underdamped scenario, using (15), (16) and (17), the general solution for the time durations of each step, $t_1, t_2, \ldots, t_{K-1}$, need to satisfy:

$$\begin{cases} \sum_{m=1}^{K} sin[\omega_0(\sum_{i=m}^{K} t_i)] = 0 \\ \sum_{m=1}^{K} cos[\omega_0(\sum_{i=m}^{K} t_i)] = -1 \end{cases}. \tag{18}$$

With more than 2 steps, there are multiple solutions for (18) that present different opportunities and tradeoffs for SC-gate drive timing. One example we will describe as *constant peak current (CPC)* driving. As shown in Fig. 9b, in this case, the goal is to keep the resonant peak current the same during each switching interval, yet, in the next-to-last interval, switch such that the final current is zero and the gate voltage achieves its final value (KV_{step}). Since all the middle steps are equivalent, this imposes additional constraints, $I_1 = I_2 = \ldots = I_{K-1}$. Then (18) can be solved for the individual time durations, t_k:

$$t_k = \begin{cases} \frac{2\pi}{3\omega_0}, k = 1, K-1 \\ \frac{\pi}{3\omega_0}, k = 2, 3, \ldots, K-2 \end{cases} \tag{19}$$

In the limit with a large number of steps, the gate current approximates a square wave, thus the gate voltage linearly ramps up with a nearly constant slew rate.

To speed up the process and achieve a faster rise-time, the switch state timing can be adjusted to ramp up the gate current by switching the first several sequences t_1, t_2, t_3 faster (providing more voltage across the gate-loop inductance). Similar to CPC, the next-to-last interval t_4 can still be tuned such that the inductor current reaches zero and gate voltage reaches its desired value at the last switching step. Termed *ultrafast (UF)* mode, this sequence results in higher RMS current, therefore higher loss and lower PRF, but achieves faster gate rise times without ringing or overshoot.

A final limiting case is termed *zero-current switching (ZCS)*. In this case, the longest reasonable switching intervals are used, which is the case where the inductor current reaches zero at the end of each interval. This results in a longer rise-time, but the lowest achievable RMS current and therefore lowest loss or highest PRF. One tradeoff is this does not allow a degree of freedom to eliminate ringing and overshoot as the last step is freewheeling, however the overshoot is small as the voltage applied across the loop inductance is much less than the total gate peak-peak voltage.

It should be noted that this analysis assumes linear gate capacitance to simplify the discussion. However, the concept shown in Fig. 9b and additional switching modes in Fig. 10 present flexible timing that can accommodate longer intervals during miller plateau periods and adjustment for nonlinear capacitance. As will be shown in the next section, slight variations in the timing can be used to achieve very similar waveforms and performance without loss of generality. We will also show that the concept does not require large inductance values to be practical. As long as the gate loop has low resistance, the concept can leverage parasitic trace or package inductance in the nH regime.

IV. Circuit Implementation

To achieve the proposed multi-mode operation, accurate timing and tuning are essential. Shown in Fig. 3, the SC gate driver uses a low-voltage on-chip controller that interfaces with the SC powertrain through a series of level shifters. The controller achieves high-resolution (short time durations) by using a multiplexed domino delay chain. The domino stage provides 5-bits of digital delay control and fine analog delay tuning. The initial rising and falling switching transitions and each of the eight timing delays $t_1 \ldots t_4$ and $t_1^* \ldots t_4^*$ are set independently by the digital controller. The SC powertrain including level shifters and timing circuitry are all implemented in low-voltage CMOS. The deep-trench SOI process allows for stacking power domains in series and affords high speed with low parasitic capacitance. The low-voltage powertrain allows the gate driver to have low effective resistance with net pull-

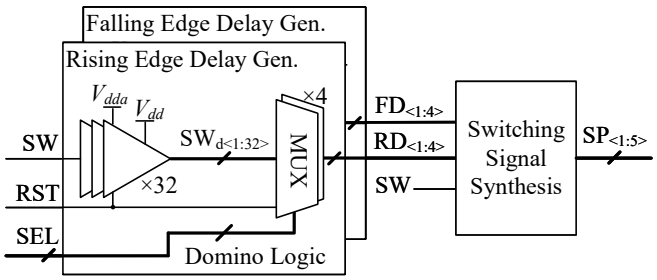


Fig. 11. The block diagram of delay generation.

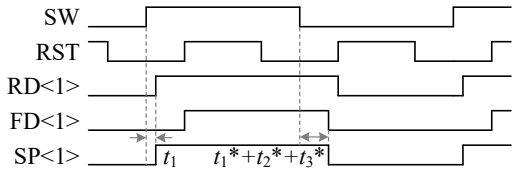


Fig. 12. A representative for the timing diagram with an example of generating the control signal for switching cell 1.

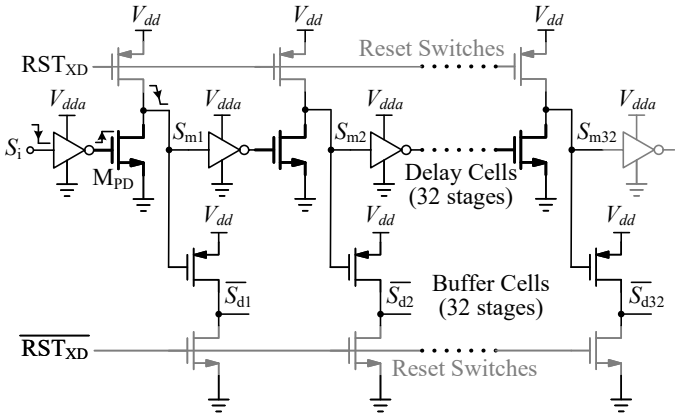


Fig. 13. The schematic of the 32-stage domino delay chain.

up/down resistance $R_{PU/PD} \approx 0.3\Omega/0.1\Omega$ to achieve $> 3\,A$ average pull-up current and strong off-state holding.

A. Timing Generation

As shown in Fig. 11, two delay blocks are used to generate the timing for the rising edge $(t_1 \ldots t_4)$ and falling edge $(t_1^* \ldots t_4^*)$ independently. Fig. 12 shows the timing diagram of delay generation. Passing through the domino logic delay chain and multiplexer, the delayed rising edge and falling edge of SW is passed to RD and FD respectively. As RST is used to reset the delay chain and the MUX, the falling edge of RD and the rising edge of FD are set by RST. Then, combinational logic is used to generate the switching cell control signal, SP. In this way, the rising and falling edges are set independently with high timing resolution.

The schematic of the domino delay chain is shown in Fig. 13. This circuit has several advantages compared to conventional delay lines or static-CMOS inverter-based delay lines. The domino structure allows for lower capacitance on each unit delay cell, resulting in shorter delay and lower power. The structure affords analog delay tuning (through

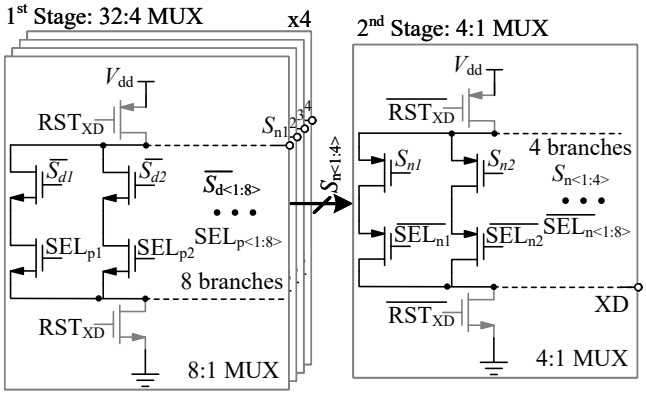


Fig. 14. The schematic of the 2-stage 32:1 MUX in domino logic.

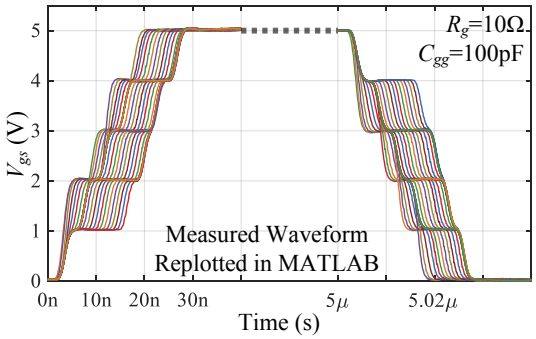


Fig. 15. Measured waveform when driving a dummy capacitive load; all rising and falling time intervals can be independently tuned.

V_{dda}) with built-in level shifting and guaranteed monotonicity. The domino delay-line can outperform a typical static-CMOS tapped-inverter chain by roughly a factor of 2×, with per-tap least-significant-bit (LSB) delay below 50 ps in the 130nm process. This is critical to achieve the short timing intervals required for the gate-drive application.

The domino circuit works with a reset phase when RST_{XD} is low, which sets intermediate nodes S_{m*} high and $\bar{S}_{d*}$ low. Prior to switching, RST_{XD} goes high and the intermediate node voltages are held by parasitic capacitance pending the state of the switching signal rippling through the delay line. This happens when S_i, goes low, then gate of M_{PD} is pulled up to V_{dda} which pulls down intermediate node S_{m1}. This signal is passed to the next delay cell via the same process controlled by the parasitic capacitance on the S_{m*} intermediate nodes and strength of pull-down transistors set by V_{dda}. This allows the total delay rippling down the delay line to be set by voltage V_{dda}, with individual delay taps selected digitally. The domino-based buffer cells recover the logic level of the delayed signals and pass them to the multiplexer. Similar to conventional domino logic, the reset switches can be very small (low capacitance); the sizing of the intermediate static inverters can be skewed, and overall delay can be tunable with high resolution and low power consumption.

The delay-line signals are passed to the input of a 2-stage domino multiplexer shown in Fig. 14. The first stage includes four 8:1 multiplexers, whose output is passed to second stage 4:1 multiplexers. With the control signal, SEL_{pl} and SEL_{nl},

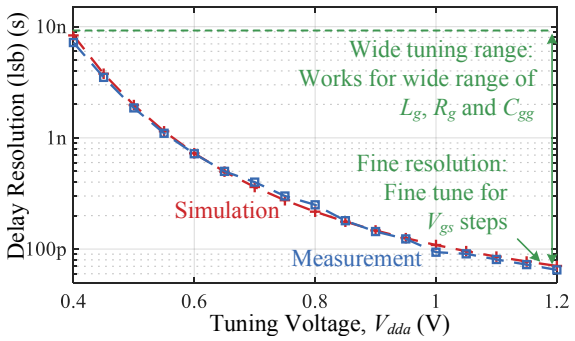


Fig. 16. Simulated and measured delay resolution.

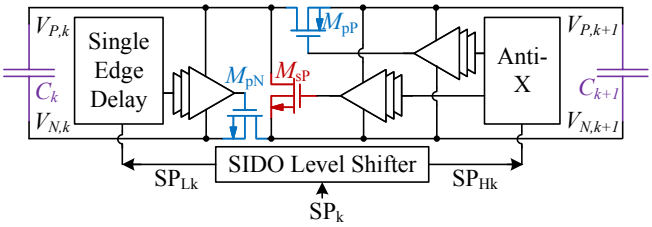


Fig. 17. Block diagram of a SC switching cell.

the desired delayed signal XD is sent out. The number of stages and the number of inputs of each stage is optimized such that the multiplexer achieves the shortest delay with minimum logical effort. Similar to the delay chain, RST_{XD} is used to reset the multiplexer.

Fig. 15 shows the output of the SC gate driver, measured in the lab, with each of the four rising and four falling timing intervals adjusted independently with the digital controller. To provide clean waveforms for delay characterization, the circuit is driving a $10\,\Omega$, $100\,pF$ capacitor load (see next section for high-frequency instrumentation considerations). Each of the timing intervals demonstrates monotonic delays with 5b control. The overall delay is set by analog voltage V_{dda}. Fig. 16 shows the delay resolution of a single time interval, *i.e.* the least-significant-bit lsb of digital control, versus tuning voltage V_{dda}. At the maximum supply voltage $V_{dda} = 1.2\,V$, the circuit achieves monotonic lsb below 50 ps. With lower V_{dda}, the circuit demonstrates 2 orders-of-magnitude tunability in high agreement with simulation. While in this work V_{dda} is tuned manually, the delay line is amenable to closed loop regulation using a delay-locked loop as in [31], which can mitigate process and temperature variation of the gate drive waveform using a reference clock or timing circuit.

B. SC Switching Cell

As shown in Fig. 17, each SC switching cell comprises three power switches, two NMOS and one PMOS, timing and driving circuitry for each switch, and a level shifter to interface the switching signals with the low-voltage digital control signal SP. Each switching cell floats independently due to SOI isolation, with the sources of the switches referenced to different voltage domains. Each level shifter and buffer chain is powered from an adjacent flying capacitor so no bootstrapping is required. However, ensuring low-latency with

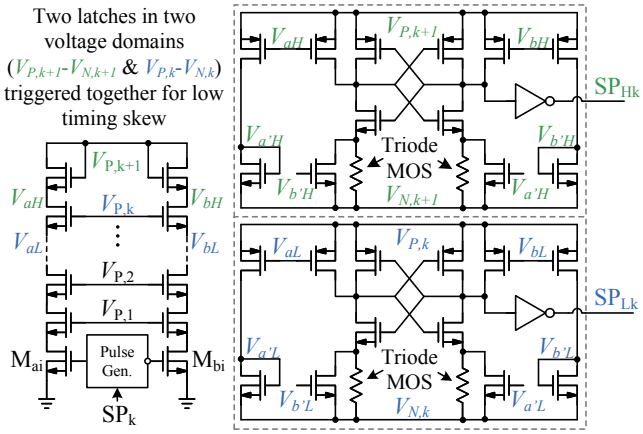


Fig. 18. The schematic of the single-input-dual-output SIDO level shifter.

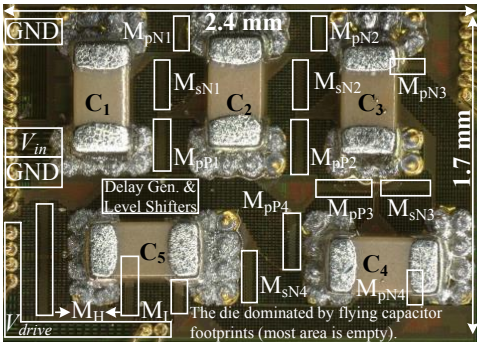


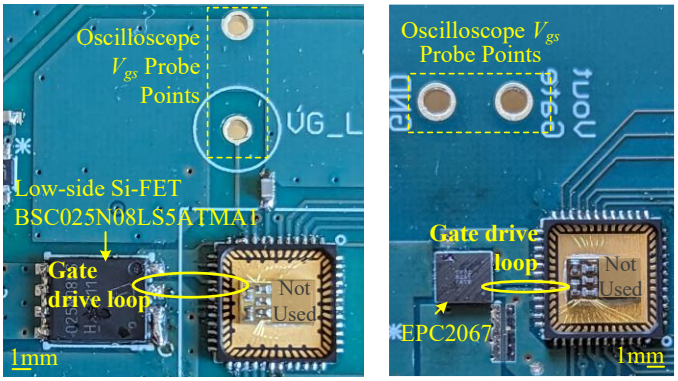
Fig. 19. Die micrograph.

minimum deadtime and no cross-conduction is critical, which warrants a special consideration for the level shifter.

In this work, we designed a single-input-dual-output (SIDO) level shifter, shown in Fig. 18, to operate safely with low latency and minimum deadtime. The SIDO level shifter is pulse based and operates in current mode with a cascode stack that passes the pulse current to latches in the floating SC cell voltage domains. The single cascode stack has outputs in each of the k^{th} and $k+1^{th}$ voltage domains. Therefore when SP_k goes high, both V_{aL} and V_{aH} are pulled down. In each of the latches, this flips the state of the latch and sets SP_{Lk} and SP_{Hk} high. When SP_k goes low, both V_{bL} and V_{bH} are pulled down, setting SP_{Lk} and SP_{Hk} low. Each differential cross-coupled latch uses triode degeneration to ensure the output can be easily flipped with low switching latency (180 ps typical, 440 ps worst case voltage, temperature and corners) and high common-mode transient immunity (CMTI). The pulse-based, latching structure eliminates quiescent current from the high voltage rail to achieve low power consumption.

V. Experimental Results

The proposed gate driver is implemented in a 130 nm SOI CMOS process. The die micrograph is shown in Fig. 19. All the control circuits, level shifter, power train are on chip; capacitors (015008 footprint) are directly soldered on the die. The specifications for off-chip components and test devices



(a) Silicon FET test setup (b) GaN FET test setup

Fig. 20. Board setup for driving MOSFETs.

are shown in Table I. The total die area is 4.1 mm^2; the used active area is much smaller, ∼1.5 mm^2.

To evaluate the energy reduction of the proposed gate driver, we compared the proposed design with a reference gate driver operating under the same conditions. The selected reference gate driver LTC4440 allows the gate driving energy to be separated from its internal quiescent bias power, which allows for a better comparison to ideal hard-switching drivers in terms of power reduction factor PRF. Test results were completed for two candidate off-chip power devices, silicon and GaN (EPC2067), shown in Fig. 20. Each of these devices has relatively high gate-charge (∼ 20-50 nC) representative of modern low threshold, low $R_{ds,on}$ power devices used for point-of-load DC-DC converters. The silicon and GaN devices have different internal parasitics, specifically internal gate resistance R_g and inductance L_g that motivate different test configurations discussed in the next sections.

A. Silicon FET Buck-Converter Configuration

The gate driver was characterized using both double-pulse (Fig. 22) and buck converter (Fig. 21) configurations. The main difference between these tests is the polarity of drain-source current during power device switching. The buck configuration is useful to characterize low-side switch operation (negative

TABLE I
SUMMARY OF THE DEVICES USED IN TESTING.

Devices	Specifications
Flying capacitors GRMMDXR60J105ME05	015008, 0.125 mm^2 6.3V, C_{eff}=796nF (derated to 1V)
Reference driver LTC4440-5	High side NMOS gate driver, 8.1 mm^2 R_{PD}=1.85 Ω, I_{PU}=1.1 A, I_{dc}=250 μA
Load GaN FET EPC2067	40V, V_{th}=1 V, R_g=0.4Ω, 4.8 mm^2 @ V_{gs}=5V: $R_{ds,on}$=1.55 mΩ, Q_{gg} ≈ 20 nC
Load Si FET BSC025N08LS5ATMA1	80V, V_{th}=1.7 V, R_g=1.7Ω, 30 mm^2 @ V_{gs}=4.5V: $R_{ds,on}$=2.6 mΩ, Q_{gg} ≈ 50 nC
Power inductor SER1390-473ML	47 μH, R_{dc}=23.1 mΩ, I_{sat}=2.6 A 1.82 cm^2
Diode (double pulse) PMEG40T30ERX	40 V, 3 A, 560pF @ 1 MHz SOD123W
High-side Si FET (buck) ISZ106N12LM6	120 V, V_{th}=1.7 V, R_g=0.96 Ω, 10.9 mm^2 @ V_{gs}=4.5 V: $R_{ds,on}$=12 mΩ, Q_{gg} ≈ 10 nC

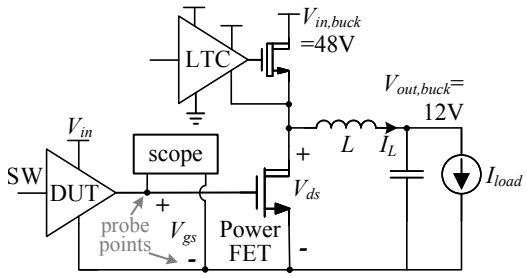


Fig. 21. Low-side switch buck converter test setup.

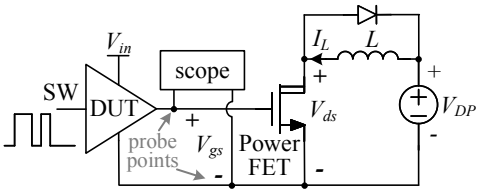


Fig. 22. Double-pulse test setup.

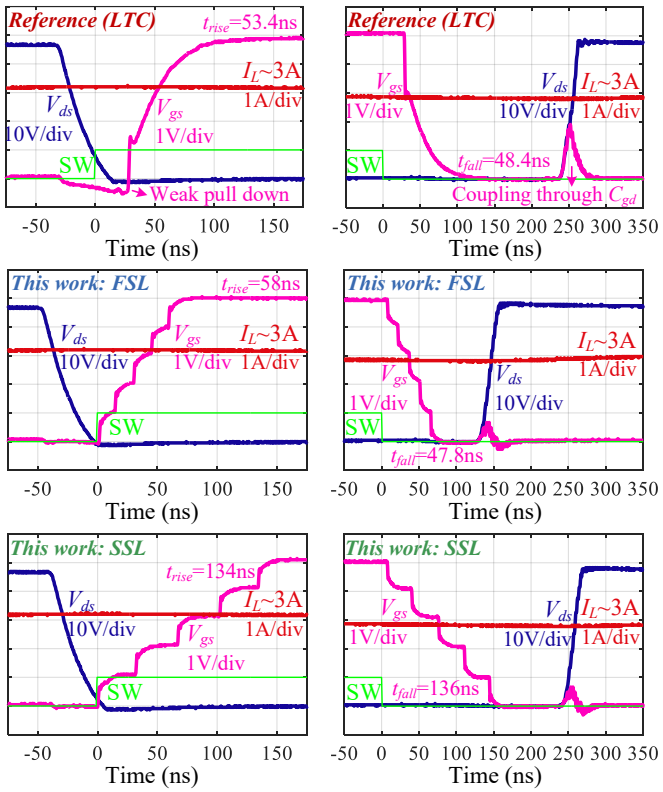


Fig. 23. Measured waveform for the reference and proposed gate drivers in buck configuration (48 V-to-12 V) with ZVS operation (I_{load} = 3 A).

I_{ds}) with and without zero-voltage switching (ZVS), which is critical for high-step-down point-of-load DC-DC converters. In the experiment, the low side device was driven by the device under test (DUT) including the proposed and reference gate driver. Here, the high side device is operated with a conventional gate driver to provide PWM operation with 48V-to-12V conversion at 3 A load current.

Fig. 23 shows the measured gate and drain voltage wave-

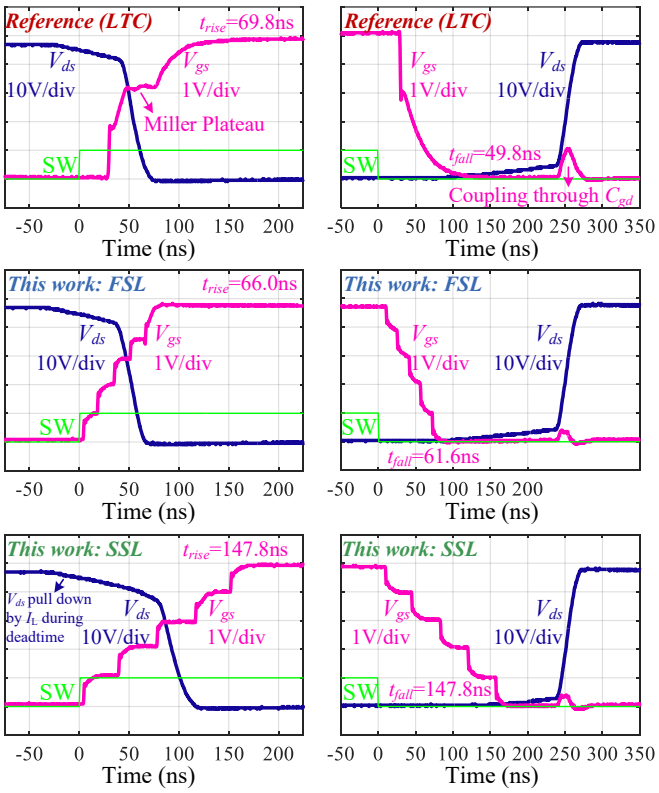


Fig. 24. Measured waveforms for the reference and proposed gate drivers in buck configuration (48 V-to-12 V) without ZVS operation (I_{load} = 0 A).

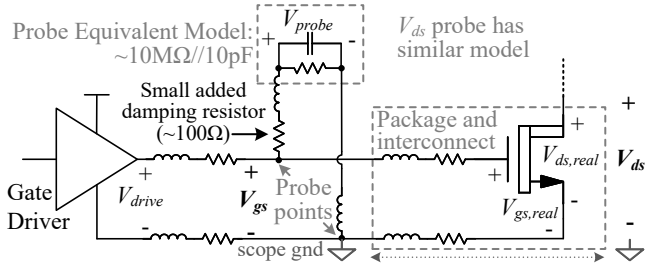
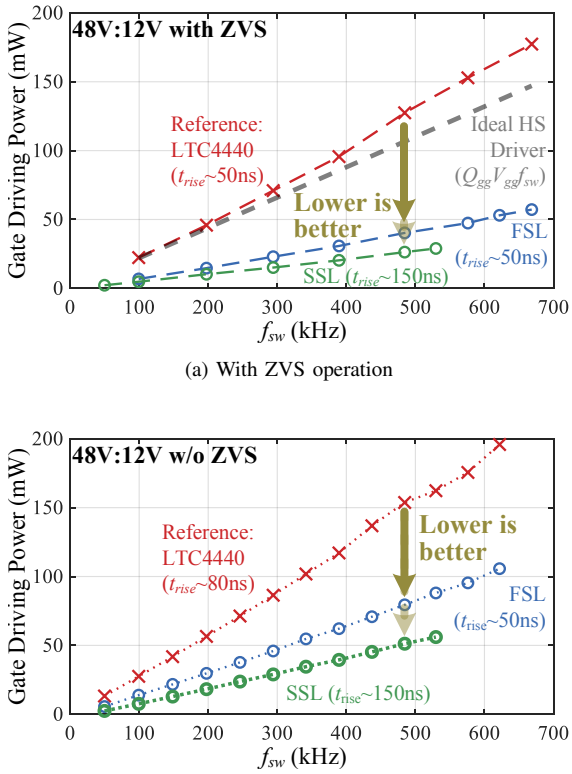


Fig. 25. Measurement setup parasitics and impact on measurement.

forms for the reference and proposed gate drivers with zero-voltage-switching (ZVS), *i.e.* $V_{ds} \approx 0\,V$ at switch turn on. With ZVS, there is no Miller charge and so the comparison to hard-switching versus the proposed circuit operating in SSL and FSL matches the description in Section III. The proposed driver can be tuned for a range of gate and drain slew rates and has stronger on- and off-state holding strength due to lower output resistance than the reference design. Fig. 24 shows the gate and drain waveforms without ZVS. Here the Miller plateau is seen in the reference driver waveform. For the proposed circuit, the Miller charge is provided by the SC circuit in roughly the t_3 time interval and is merged with the SC step. Thus, while the Miller charge affects the charge-flow out of the SC stage, it is accommodated by the stepped voltage waveform, which can provide the same or faster rise/fall times than the reference hard-switching driver.

High frequency measurement artifacts can occur due to the location and dynamics of the oscilloscope probe. Shown in



(a) With ZVS operation

(b) Without ZVS operation

Fig. 26. Measured gate drive power consumption under different conditions.

Fig. 25, this is due to the distributed impedance of the gate switching loop and ringing within the scope probe itself which adds its own capacitance and inductance. Here, the silicon FET has internal gate resistance of $\sim 1\,\Omega$; when the gate driver switches, there can be a steep rise initially, some ringing in the measurement, then a slow rise to the eventual steady state voltage. The ringing is due to internal scope probe inductance and capacitance outside the natural frequency of the gate loop. The steep initial step is due to the resistor divider between the driver and the power FET internal resistance. There are similar considerations for V_{ds} related to the probe location that can impact high dV_{ds}/dt measurements, especially in the presence of drain-source loop inductance. To mitigate spurious measurement artifacts, we added a 100 Ω resistor in series with the oscilloscope probe. This has a negligible impact on measurement bandwidth but damps internal scope probe ringing to provide clearer gate and drain voltage measurements.

Fig. 26 shows measured gate-drive power for the reference and proposed gate drivers versus switching frequency. The reference driver closely matches an ideal hard-switching driver with slightly higher deviation (higher power) at high frequency. In FSL, with gate and drain slew rates comparable to those of the reference driver, the SC driver achieves ~3× lower power consumption with ZVS and ~2× power reduction without ZVS, the difference between these is related to Miller charge. With slightly longer rise times, operating in SSL, the SC driver achieves peak $PRF \approx 4.8$ in ZVS operation.

Fig. 27 characterizes the SC gate driver slew rate modulation using double-pulse testing. By operating in FSL, the SC gate

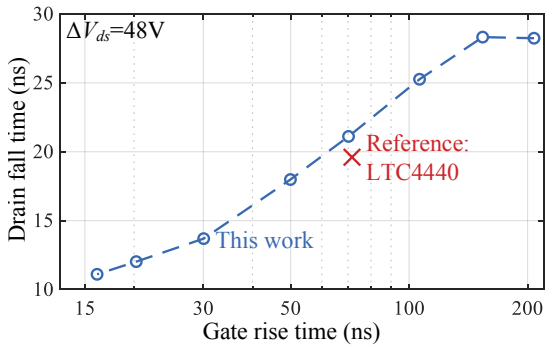


Fig. 27. Drain fall time versus gate rise time using double pulse testing.

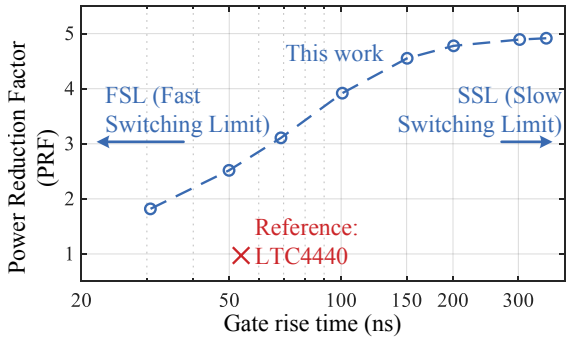


Fig. 28. Power reduction factor PRF versus gate rise time.

driver can achieve 16 ns gate rise time with 11 ns drain fall time, which is faster than the reference design. Both the gate and drain slew rates can be adjusted through the control circuit timing. Seen in Fig. 28, faster rise and fall times relate to lower power savings, but with longer rise times, the PRF approaches its ideal value.

B. GaN Device Testing

As seen in Fig. 20b, the drive IC was wirebonded in an open-cavity QFN, soldered within several mm of the GaN FET. While this results in a small gate-source loop, there is still several nH gate loop inductance, which leads to a moderately underdamped ($Q \sim 3$) driving loop. The GaN FET was tested in a standard double pulse setup for both the proposed SC gate driver and the reference gate driver. The test voltage V_{DP} was set to 48 V. The first pulse width was adjusted for inductor current of 2 A during turn on. The voltage waveform of the gate, drain, and the power consumption of the two gate drivers were compared.

Fig. 29 shows the measured waveforms under double pulse testing for different operating modes. The reference driver achieved gate rise time of 28 ns and drain fall time of 6 ns. In ultrafast mode, the proposed design achieved rise time of 10.7 ns and drain fall time of 2 ns, roughly three times as fast. However, as shown in Fig. 30, at the same switching frequency, the power consumption is reduced by roughly 2×. With slightly slower response, the proposed driver can operate in the constant-peak-current (CPC) mode, achieving

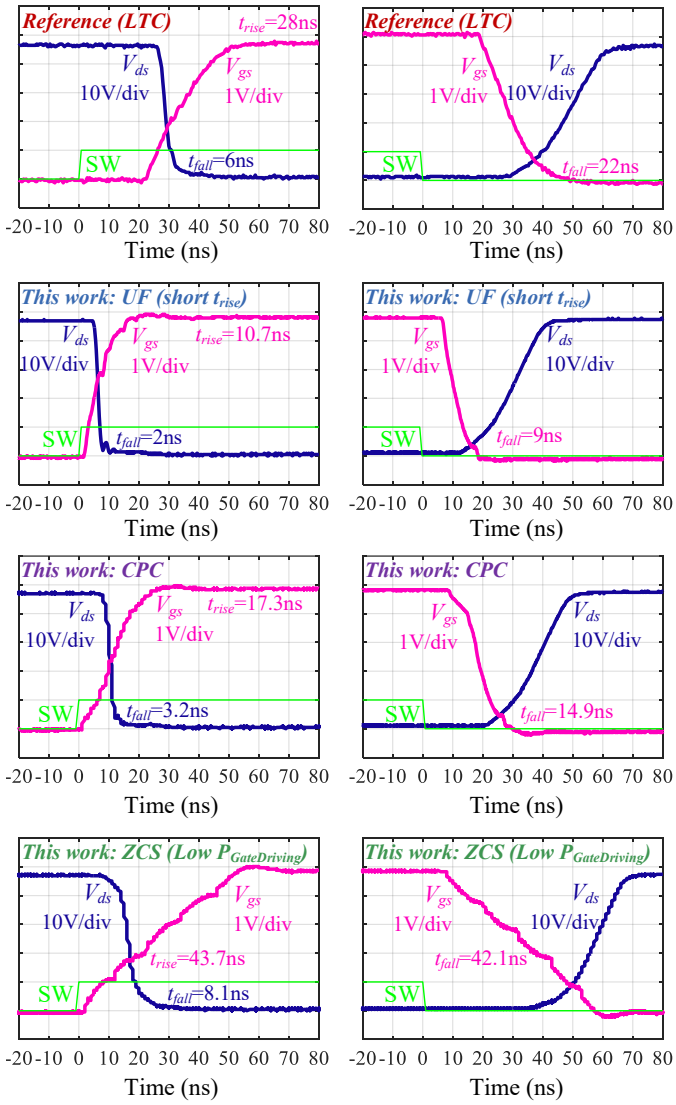


Fig. 29. Measured waveforms for GaN device V_{gs} and V_{ds} with double pulse testing configuration.

nearly comparable gate and drain slew rates to the reference LTC4440, but with roughly 3× lower power consumption. In the ZCS mode of operation, the proposed design operates with slower rise and fall times, but with even lower power consumption, achieving a power reduction factor of $PRF \approx 7$, by leveraging the parasitic loop inductance in resonant mode. In ZCS mode, V_{gs} has slightly higher overshoot compared to other modes, due to inductor current free wheeling, as discussed in section III-B. Fig. 31 combines the results for PRF at 1 MHz switching frequency. Most importantly, this shows the ability of the proposed driver to reduce gate drive power compared to the conventional hard-switching design. It also shows the ability of the driver to operate in multiple modes to trade off dynamic switching speed for power savings.

C. Comparison to Prior Art

Table II compares this work with prior art, including representative hard-switching and resonant gate drivers that are

TABLE II
COMPARISON TO PRIOR ART DISCRETE MOSFET GATE DRIVERS

	Ke ISSCC'16 [28]	Zan TPEL'20 [26]	Seidel JSSC'18 [29]	Eberle TIE'08 [13]	Tong ECCE'19 [15]	Reference (LTC4440)	This Work
Topology	Hard-switching	Hard-switching	Resonant	Resonant	Resonant	Hard-switching	Multi-level resonant driver
Process	350 nm HV BCD	Discrete	180 nm BCD	Discrete	Discrete	not reported	130 nm SOI
Area	0.5 mm^2	11.9 cm^2	11.3 mm^2	not reported	9.5 cm^2	8.1 mm^2	4.1 mm^2
Load Device	GaN	GaN	GaN GIT (1)	Si	SiC	GaN & Si	GaN & Si
V_{gs} up slew(2)	5 V / 2 ns(3) (2.5 V/ns)	3.3 V / 0.2 ns (16.5 V/ns)	7 V / 7.8 ns(3) (0.9 V/ns)	5 V / 60 ns (0.08 V/ns)	27 V / 11 ns(3) (2.5 V/ns)	5 V / 28 ns (0.18 V/ns)	5 V / 10.7 ns (0.47 V/ns)
Q_{gg} up slew ($I_{g,ave,max}$)	0.13 nC / 2 ns(3) (0.07 A)	0.08 nC / 0.2 ns (0.45 A)	11.6 nC / 7.9 ns(3) (1.5 A)	80 nC / 60 ns (1.33 A)	10.8 nC / 11 ns(3) (0.98 A)	49 nC / 53.4 ns (0.92 A)	49 nC / 16 ns (3.06 A)
V_{ds} down slew(2)	40 V / 1.2 ns (33 V/ns)	45 V / 0.7 ns(3) (62 V/ns)	80 V / 2.8 ns(3) (29 V/ns)	not reported	not reported	48 V / 6 ns (8 V/ns)	48 V / 2 ns (24 V/ns)
PRF	0.51(4)	0.05	not reported	1.85(4)	5.86(5) 0.86(4)	0.94(4)	7.0 (high-Q)(4) 4.8 (low-Q)(4)

(1) Gate-injection transistors: have constant I_g during on-state
(2) V_{gs} and V_{ds} slew rates depend on the power device under test; larger load devices will have lower slew rates and vice versa.
(3) Estimated from reported data and plots.
(4) Best estimate of PRF based on reactive power calculations using $Q_{gg}V_{gg}f_{sw}$
(5) Referenced to hard-switching driver IXRFD630

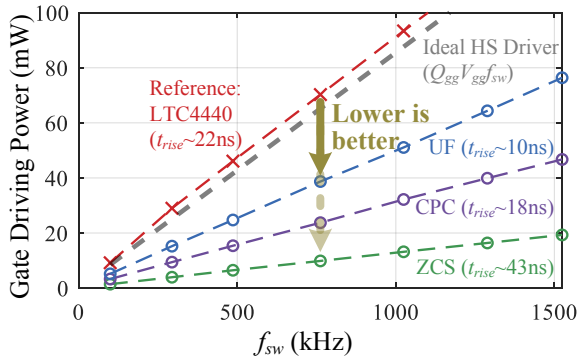


Fig. 30. Measured power consumption for the reference gate driver and the SC gate driver with different operation modes when $V_{DP} = 0$ V.

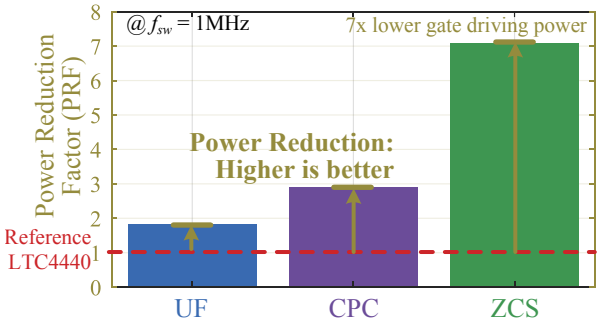


Fig. 31. The PRF of the SC gate driver referenced to LTC4440 when drivers a GaN FET.

designed to drive off-chip (discrete) power devices. While this work achieves comparable gate and drain slew rate to state-of-the-art hard-switching drivers, these metrics depend heavily on the load device and loop parasitics. A more relevant metric is the gate charge slew rate or average drive current. In this regard, the proposed design achieves high drive current relative to academic or industry benchmarks. This shows that fast rise and fall times can be achieved with the multi-step SC driver for relatively high gate charge, low R_{dson} power devices. Thus, driving speed and slew rates need not be sacrificed when using the multi-level SC drive concept.

Compared to prior art resonant drivers, this work has smaller area by roughly 2-orders-of-magnitude; it does not require discrete inductance and is nearly fully-integrated, whereas most prior work resonant drivers require large or discrete inductance. The high-energy-density ceramic capacitors have combined area less than 1 mm^2, comparable to the area of a single bootstrap capacitor for a conventional gate driver. Compared to past resonant gate drivers, this work provides faster rise times and tunable gate waveform control to operate with different gate loop impedance and mitigate parasitic effects. The fast response and variable timing is a significant improvement compared to conventional resonant drivers that have a limited degree of freedom to modulate rise and fall times when using resonant operation. Also, this work demonstrates energy savings up to 4.8× even in scenarios without any loop inductance or when the dominant loop impedance is resistive.

Table II also includes two ways of calculating PRF: using the power consumption of a reference gate driver and using a best estimate of the reactive load power $Q_{gg}V_{gg}f_{sw}$ to calculate. The benefit of using a reference driver is that it provides a straightforward and rapid comparison under a range of operating conditions. However, the accuracy of this method depends on the reference driver, which can have additional sources of power consumption and loss that are difficult to calibrate, so both methods are shown in some circumstances. Compared to prior art, this work achieves the highest PRF, achieving the highest power reduction for both overdamped and underdamped gate driving loops, while providing multi-mode operation and waveform tunability to provide power

savings with fast driving capability.

VI. Conclusion

This paper presented a pseudo-resonant switched-capacitor gate driver achieving power reduction by stepping the gate voltage with small increments. In the reconfigurable series parallel converter, flying capacitors are used to deliver and recover gate charge energy with variable per-step tuning that affords a range of multi-mode switching operation. In the 130nm SOI CMOS IC, a multiplexed domino delay line achieves variable sub-ns step tuning. The proposed gate driver was tested in various setups with silicon and GaN power devices to characterize the performance with a range of loop impedances. Compared to a conventional hard-switching gate drivers, this work achieved 2-7$\times$ power reduction for the same or faster gate rise time with the ability to modulate the slew rate of the gate and drain voltages. With a small form factor, no discrete inductors, and high-resolution gate and drain waveform tuning, this work demonstrates a viable pathway to small, efficient, flexible, and effective resonant gate driving.

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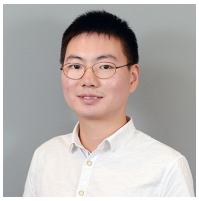

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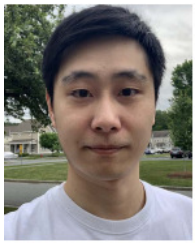

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