High Power Characterization of SIW-based D-band Traveling Wave Amplifiers

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***Abstract*— The high-power performance of a D-band (110–170 GHz) traveling wave amplifier (TWA) is reported. The amplifier was designed and fabricated using a GaN-on-SiC high-electron mobility transistor (HEMT) technology integrated with a substrate integrated waveguide (SIW) structure for low-loss on-chip power combining. Active injection load-pull measurements of both discrete HEMTs as well as the completed MMIC TWA were performed. The discrete HEMT measurements at D-band supplement the available design data for these scaled GaN HEMTs. The TWA achieved a peak power-added efficiency (PAE) of 9.1% at 145 GHz. The available output power exceeded 23.5 dBm from 135-145 GHz, with a maximum output power of 24.7 dBm (295 mW) at 140 GHz.**

***Keywords*—millimeter wave, MMICs, power amplifiers, HEMT, load pull, high power, high efficiency.**

I. Introduction

The D-band frequency range (110 GHz-170 GHz) is critical for next-generation wireless communications due to its large available bandwidth, low atmospheric absorption, and potential to support ultra-high data rates up to 100 Gbps [1], [2]. These characteristics enable transformative applications such as high-speed wireless communication, automotive radar with enhanced resolution, precision sensing for industrial automation, immersive holographic communication, and secure satellite communication [3], [4].

However, realizing the full potential of D-band communications requires advanced amplifier and signal processing technologies to efficiently handle the demanding bandwidth and power requirements. Distributed amplifiers are particularly attractive for wideband applications such as millimeter-wave communications due to the wide frequency response that can be achieved [5].

To overcome the limitations of microstrip and coplanar waveguide-based TWAs due to transmission line loss at mm-wave frequencies, substrate-integrated waveguides (SIWs) provide an ideal solution. SIWs combine low insertion loss, minimal crosstalk, and high power-handling capacity, ensuring efficient power transmission and robust performance in high-frequency and high-power systems. These attributes make SIWs an attractive choice for integrating distributed amplifiers and other components in next-generation millimeter-wave and sub-terahertz communication networks [6].

A proof-of-concept D-band SIW-based traveling wave amplifier (TWA) was reported in [7]. While this previous work demonstrated that transistors can be effectively embedded along a SIW to achieve low-loss power combining at D-band, the demonstrated performance was constrained by the unavailability of D-band large-signal high-electron mobility transistor (HEMT) performance data, as well as equipment limitations during the circuit performance testing. To address these issues, this work experimentally evaluates the large-signal performance of the scaled HEMTs in the fabrication process used for the microwave monolithic integrated circuit (MMIC) TWAs. In addition, on-wafer high-power characterization of the TWA was performed. The transistors exhibited a saturated output power (P_{out}) density of approximately 2 W/mm and power added efficiency (PAE) of 17.1% at 140 GHz. For the SIW-based TWAs, the low loss of the SIW output line enabled a PAE of 9.1% at 145 GHz and a P_{out} of 24.7 dBm (295 mW) at 140 GHz.

II. Characterization Approach

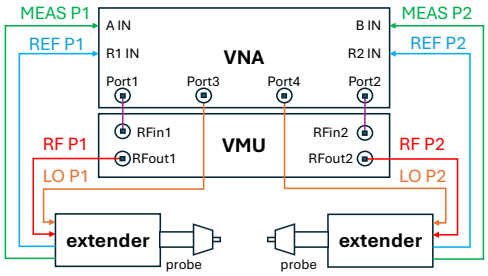
The measurement system diagram that was used for the small- and large-signal characterization is shown in Fig. 1(a) [8]. The system includes a Keysight N5245B vector network analyzer (VNA), a Vertigo vector modulator unit (VMU), two VDI WR6.5VNATxRxM-4HP frequency extenders, and FormFactor I170-S-GSG-50-BT probes. For transistor measurements, the DC bias was applied through the internal bias tees of the probes; for MMIC characterization, DC bias was supplied through additional FormFactor I67-A-GSG-100 probes (Fig. 1b) and Anritsu V251 bias tees with 50 Ω terminations applied to suppress oscillation.

To enable accurate power and active load pull measurements with appropriate reference planes, calibration of the system includes three major steps:

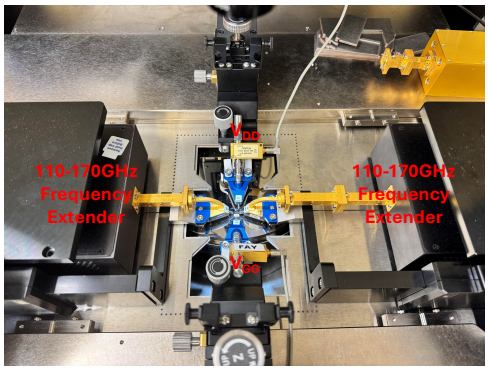
- First-tier two-port TRL waveguide calibration with WR6.5 calibration kits to place the reference planes at the WR6.5 waveguide extender flanges
- Waveguide port power calibration and leveling using a VDI Erickson PM5B power meter
- Second-tier two-port TRL calibration with on-wafer calibration standards, placing the reference plane for subsequent measurements at the middle of the on-wafer through standard.

After calibration, the system can supply up to 22.9 dBm to the device under test at the second-tier calibration reference plane (achieved at 140 GHz, the middle of D-band). In addition, active load pull measurements of the on-wafer through were

performed to validate the system performance; the measured power error was found to be within ±0.3 dB as shown in Fig. 2.



(a)



(b)

Fig. 1. (a) System architecture [8]; (b) Measurement configuration for MMIC testing.

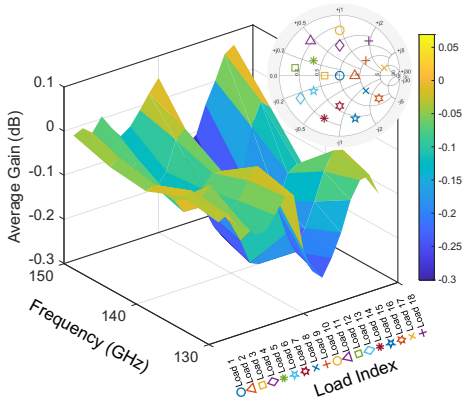
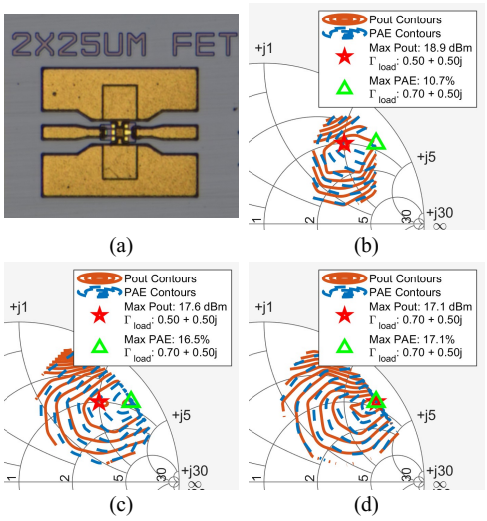


Fig. 2. Load pull validation on Thru with P_{in} from -10 to 20 dBm for frequencies from 130 to 150 GHz.

III. Transistor Characterization

For discrete transistor evaluation, transistors fabricated in HRL Laboratories' "T3" 40-nm GaN-on-SiC HEMT technology were used. This process provides nominal f_t's of 200 GHz and f_{max}'s of 400 GHz [9]. The devices tested were configured with two 25 µm wide gate fingers, as shown in Fig. 3(a).

To explore the performance limits of the technology, the HEMTs were measured under large signal conditions with active injection to control the effective load impedance. The load pull was measured up to $|\Gamma_{load}| \sim 0.9$, which is not practical with passive tuners in D-band and is a key advantage of the active injection approach. Figure 3(b)-(d) shows the measured load-pull contours at 140 GHz, sliced at the 3 dB compression point for quiescent drain current (I_d) densities of 50, 100, and 200 mA/mm and a drain voltage (V_{ds}) of 12 V. As can be seen, the optimal load for peak PAE is $\Gamma_{load} \sim 0.7 + 0.5j$ for the single FET, largely independent of bias over the range explored here. The load for maximum output power was found to be ~ 0.5 + 0.5j, in close proximity to the peak PAE load. The power sweep at the optimal Γ_{load} for maximum PAE was analyzed and compared in Fig. 4. Under this load condition, for a drain current bias of 200 mA/mm, a small-signal gain of 7 dB, with a peak PAE of 17.1% and a 3 dB compressed output power (P_{3dB}) of 17.1 dBm and maximum saturated output power of 19.5 dBm were obtained at 140 GHz. Similar output power, but lower small-signal gain, was achieved at lower drain bias current density (Fig. 4). This data will be valuable for improving the performance of future D-band circuits based on this transistor technology.



(a) (b) (c) (d)

Fig. 3. (a) Micrograph of a 2x25 µm HEMT; Load pull contours at 3 dB compression of a 2x25 µm FET at 140 GHz with V_d of 12V: (b) I_d = 50 mA/mm; (c) I_d = 100 mA/mm; (d) I_d = 200 mA/mm.

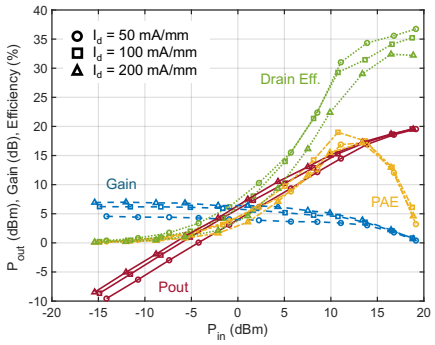


Fig. 4. Power Sweep of a 2x25 µm FET at 140 GHz with the optimal Γ_{Load} of 0.7+0.5j.

IV. TWA Characterization

Based on this transistor technology, a SIW-based TWA was designed, fabricated, and characterized (Fig. 5) [7]. However, limited by the available input power, the amplifier could not be driven into gain compression. Using the present measurement

setup, Figure 6 shows the small-signal S-parameters of a typical TWA; at the bias applied for these measurements the HEMT drain current density is approximately 200 mA/mm and V_{ds} is 12 V. The amplifier exhibits a peak small-signal gain of 3.5 dB at 145 GHz; the 3 dB bandwidth is over 20 GHz.

Using active signal injection into the output port, the load pull power sweep for the TWA was further investigated. Figure 7 shows the measured load-pull contours of the TWA at 135, 140, 145, and 150 GHz. The gain inferred from the large-signal power sweeps shows a peak gain of 3.2 dB at 1 dB compression point at 145 GHz, in reasonable agreement with the measured S-parameters. Furthermore, the load-pull contours indicate that although the TWA is designed to match 50 Ω at 140 GHz (the center of D band), the best power and efficiency is achieved at 145 GHz. This shows that the load pull measurement can be used to fine-tune the amplifier design.

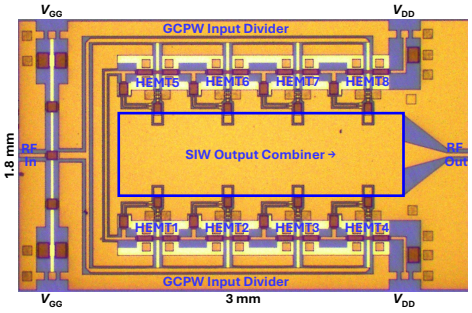


Fig. 5. Micrograph of a TWA chip [7].

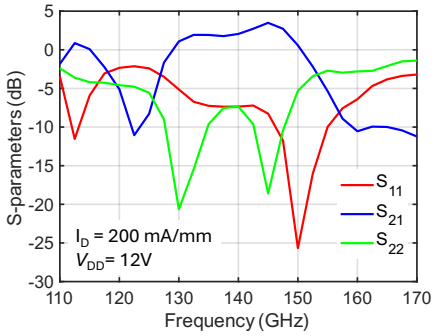


Fig. 6. Small signal measurements of a TWA.

The power sweeps at the optimal Γ_{load} for PAE are further compared with 50 Ω power sweeps in Fig. 8, for 135, 140, 145, and 150 GHz across the amplifier bandwidth. A peak gain of 4.2 dB was obtained at 145 GHz with a measured PAE of 9.1%, setting a new PAE benchmark for D-band GaN power amplifiers at 145 GHz, as shown in Table 1 [10]. Furthermore, the measured saturated P_{out} of 24.7 dBm (295 mW) at 140 GHz also represents a record output power for GaN-based power amplifiers. By using the large-signal characterization approach described here, a higher available power and improved power level control enables more detailed device and circuit characterization at input power levels at the DUT input of up to 22.9 dBm. This allows the performance of scaled GaN HEMTs in D-band to be more clearly evaluated. The transistor- and circuit-level characterization provides direct evidence of the potential of this technology for D-band communication systems.

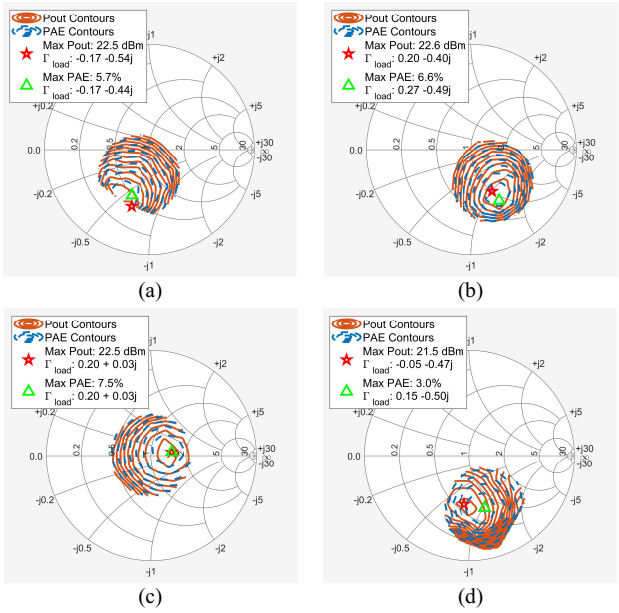


Fig. 7. Load pull contours of a TWA: (a) 135 GHz at 1 dB compression point; (b)140 GHz at 1 dB compression point; (c) 145 GHz at 1 dB compression point; (d) 150 GHz at 0.6 dB compression point.

Table 1. Performance Comparison of D-band GaN Power Amplifiers [10].

Year	Freq. (GHz)	Psat (dBm)	PAEmax (%)	P1dB (dBm)	PAE at 1dB (%)	Gain (dB)	Ref.
2018	115	20.3	–	15.5	–	30	[11]
2018	120	17.4	4.3	–	–	18	[12]
	147	18.2	1.7	–	–	17	
2019	120	26.4	16.5	25	13	26	[13]
2022	140	15.9	9.1	–	–	12	[14]
2022	166	21.5	–	–	–	20	[15]
2022	133	19.9	6.5	13.5	–	13	[16]
	137	18.5	4.7	16.1	–	21	
2022	136	23.5	7.9	19.7	–	10.5	[17]
2024	140	19	–	–	–	–	[7]
	135	23.5	6.5	22.5	5.7	3.3	This work
	140	24.7	7.5	22.6	6.6	3.6	
	145	24.0	9.1	22.5	7.5	4.2	

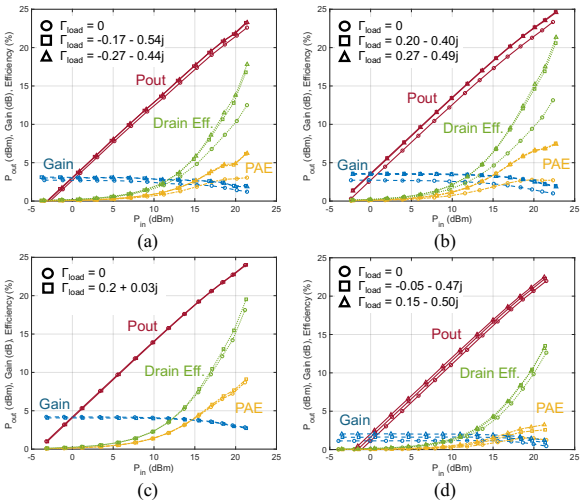


Fig. 8. Power sweep of a TWA for optimal Γ_{load} and 50 Ω: (a) 135GHz; (b) 140 GHz; (c) 145 GHz; (d) 150 GHz.

V. Conclusion

This work comprehensively explores the high-power performance of the scaled GaN-based HEMTs and SIW-based TWAs in more detail than was previously possible. The HEMT technology demonstrates D-band output power density of up to 2 W/mm and PAE of 17.1%, with 7.0 dB small-signal gain. This transistor technology was integrated with low-loss on-chip SIW-based power combining in a TWA. The large-signal characterization of TWAs made with this technology achieved a maximum P_{out} of 24.7 dBm at 140 GHz, and a PAE of 9.1% at 145 GHz, demonstrating the potential of this technology for future-generation millimeter-wave systems.

Acknowledgment

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