A Fully-Integrated Backscatter Modulation System with High Image Rejection and Near Zero Power Wake-up Receiver Offset Cancellation

Shen Shen[1], Yiming Han, Jiankun Li, Yaoyao Jia[2]
University of Texas at Austin, USA
[1]shenshen@utexas.edu, [2]yjia@austin.utexas.edu

2024 IEEE Biomedical Circuits and Systems Conference (BioCAS) | 979-8-3503-5495-9/24/$31.00 ©2024 IEEE | DOI: 10.1109/BioCAS61083.2024.10798411

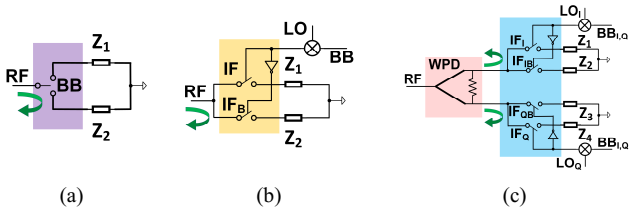
***Abstract*—This paper presents a design of a spectral efficient backscatter modulation system with integrated Wilkinson power divider (WPD) and novel wake-up receiver calibration technique. This structure consumes 44.5 µW and occupies an effective area of 0.77×0.88 mm² which achieves about 1,000 times footprint reduction compared to off-chip WPD implementations, making it applicable in implantable biomedical devices. The innovative RF front-end, featured a quadrature load combination using a capacitive path and a short circuit path, along with a symmetric multiplexer-based single sideband intermediate frequency mixer, achieves high image rejection for enhanced spectral efficiency. The pseudo-differential wake-up receiver that employs an offset cancellation technique presents ~20 dB enhanced sensitivity. This work is verified in standard 0.18-µm CMOS technology. Silicon measurement results demonstrate a 31.4 dB image rejection ratio and -39.9 dBm receiver sensitivity. Then, data recovery in a software-defined radio (SDR) setup is carried out to demonstrate its functionality in real-time transmission.**

***Keywords*—implantable, backscatter, image rejection, single sideband, Wilkinson power divider, wake-up receiver, PLL.**

I. Introduction

Backscatter modulation system enables low-cost wireless communication in applications where power consumption and footprint are of critical concern, such as IoT, wearable and implantable biomedical devices. Fig. 1 depicts some of the backscatter modulation techniques. Compared to direct load modulation [1] in Fig. 1a, baseband data can be upconverted to an intermediate frequency (IF) before modulating the RF front-end to avoid the self-interference issue [2], as shown in Fig. 1b. However, it creates double sidebands including an image band that interferes with other channels. A quadrature load modulator similar to the Hartley architecture is thereby proposed in [3] for image cancellation wherein quadrature sets of RF switches are driven by quadrature IF frequencies, as shown in Fig. 1c. Incident waves needed by the two sets of RF switches are generated through a Wilkinson power divider (WPD) that also serves as a power combiner that recombines the reflected signals [4]. However, the WPD implementation typically requires two segments of λ/4 transmission line (T-line) [5]. For sub-3GHz carrier frequencies, T-line takes up a substantial area on PCBs that would impede the industrial adoption of such techniques.

Moreover, the passive envelope detector, e.g., the Dickson structure, dominates in the µ-watt wake-up receivers (WuRX) owing to its superior sensitivity and free of 1/*f* noise [4], [6]. However, the inevitable input-referred offset associated with the baseband gain stage or comparator following the envelope detector could degrade the WuRX sensitivity significantly.



(a) (b) (c)

Fig. 1. Backscatter modulation approaches. (a) Direct load modulation. (b) Frequency-translated load modulation. (c) Quadrature load modulation with transmission-line-based WPD.

To address these challenges, we present a backscatter design (Fig. 2) that features an integrated WPD and a novel RF front-end, achieving a significant footprint reduction and high image rejection. Furthermore, the pseudo-differential WuRX, built on the Dickson structure, incorporates a novel offset cancellation technique, offering significantly improved sensitivity at a cost of near zero extra power.

II. Design of Backscatter Modulation System

A. Design of On-chip Wilkinson Power Divider

T-line-less WPD can be built out of the T-line-based approach with each λ/4 T-line segment replaced with C-L-C π-network [5], as shown in Fig. 3a.

For inductor implementations, Fig. 3b and 3c depict two layout options with the current direction shown: differential vs single-ended. In the case of power dividers, the single-ended structure is superior in terms of meeting an inductance target with decent Q and high self-resonance frequency. This is because in Fig. 3b, the magnetic fields induced by I_2 and I_3, respectively, oppose each other, causing each individual self-inductance diminished by their mutual inductance. By contrast,

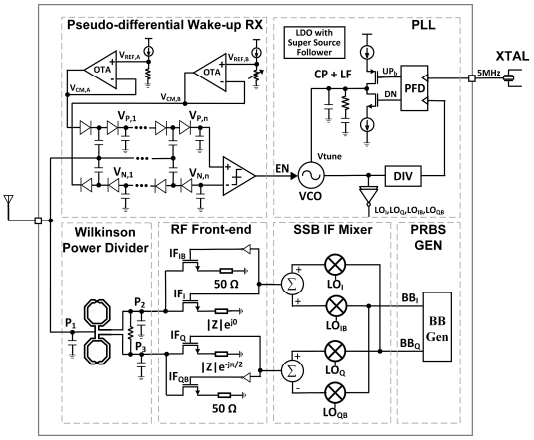


Fig. 2. Proposed backscatter architecture.

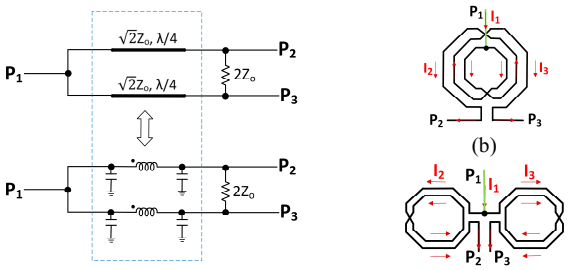


Fig. 3. Wilkinson power divider: (a) T-line and lumped elements equivalent. (b) differential inductor layout and (c) single-ended inductor layout.

in Fig. 3c, the magnetic field induced by I_2 and I_3, respectively, aid each other. Moreover, along the symmetry axis, magnetic fields induced by both inductor coils get canceled. This facilitates the RF signal routing without interference concerns.

At 2.4 GHz, the inductance of each coil and the shunt capacitance are calculated in theory as 4.69 nH and 938 fF, respectively. The shunt capacitor is implemented with MIM capacitors. The inductor is designed and optimized with Cadence EMX, where the S-parameters of the WPD are extracted together with the RF traces and ESDs.

B. Proposed RF Front-end

From an RF perspective, the modulated load impedances would change the reflection coefficient Γ, given by definition:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{1}$$

One implementation of quadrature loads in [4] consists of an open circuit (O.C.) path to generate $e^{j0°}$ and a capacitive path for $e^{-j90°}$, as shown in Fig. 4a. For the O.C. path, $\Gamma_{OC} = 1\angle 0°$. For the capacitive path (C.P.), the finite R_{on} of the RF switch and the termination capacitor C_L form an R-C network and therefore alters Γ_{CP} in such a way that:

$$\Gamma_{CP} = \frac{(Z_{R_{on}} + Z_{C_L}) - Z_0}{(Z_{R_{on}} + Z_{C_L}) + Z_0} \tag{2}$$

Considering the trade-off between R_{on} and LO driver strength, this design selects R_{on} at 5 Ω. Meanwhile, C_L is 1.33 pF so that $1/(2\pi f C_L)$ equals ~50 Ω. Since WPD is matched across all ports, Z_0 is assumed to be 50 Ω. Then, based on (2), Γ for the capacitive path is calculated as:

$$\Gamma_{CP} = 0.0045 - j0.9 \approx 0.9\angle -89.7° \tag{3}$$

Unlike the ideal capacitor that gives $\Gamma_{CAP} = 1\angle -90°$, lagging the O.C. path by exactly 90° with unity magnitude, (3) reveals that due to R_{on}, the reflected wave experiences ~90° phase shift but also amplitude loss. Since the image sideband is suppressed by summing up the reflected signals RF_I and RF_Q, the phase variation and the amplitude mismatch between the quadrature paths literally degrade the suppression effect.

To address this limitation, the proposed RF front-end incorporates modifications of replacing the O.C. path with a short circuit (S.C.) path and swapping the capacitive path and the S.C. path to maintain the π/2 phase relationship, as shown in Fig. 4b. In this configuration, to eliminate the amplitude mismatch of Γ between the S.C. path and the capacitive path, $|\Gamma_{SC}|$ should be equal to $|\Gamma_{CP}|$, as Γ_{CP} is obtained in (3), thus:

$$|\Gamma_{SC}| = \left|\frac{Z_{SC} - Z_0}{Z_{SC} + Z_0}\right| = |0.9\angle -89.7°| = 0.9 \tag{4}$$

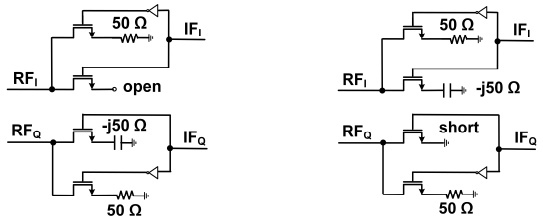


Fig. 4. Quadrature RF front-end configurations: (a) open circuit path and capacitive path to form quadrature load combination. (b) proposed capacitive path and short circuit path to form quadrature load combination.

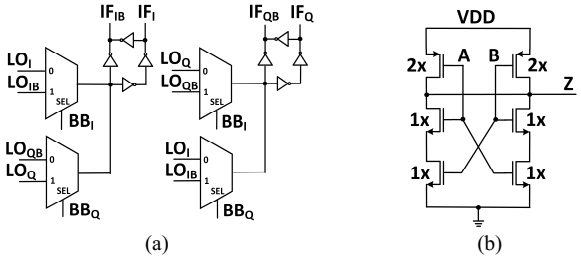


Fig. 5. (a) MUX-based SSB IF mixer. (b) Symmetric NAND logic cell.

where Z_{SC} is the impedance needed from the S.C. path. Solving (4), Z_{SC} equals 950 Ω. For an ideal S.C. path, this cannot be achieved since Z_{SC} is 0 Ω. However, since the RF switch on the S.C. path controls its on and off, the 950 Ω can be realized with R_{on} of that switch. As a result, the π/2 phase relationship is guaranteed, as well the amplitude mismatch is well canceled.

C. Design of PLL

In the single sideband (SSB) IF mixer configuration, four quadrature clock phases, LO_I, LO_Q, LO_{IB}, LO_{QB}, at 25 MHz each spaced 90° apart are synthesized from charge pump (CP) based phase-locked loop (PLL), in which the voltage-controlled oscillator (VCO) is implemented with a two-stage differential ring oscillator.

To achieve >20 dB power supply rejection (PSR) across the entire frequency band, a low drop-out (LDO) voltage regulator with super source follower is implemented [7].

D. Design of SSB IF Mixer

The SSB IF mixer is implemented with MUX cells, as shown in Fig. 5a. BB_I and BB_Q are generated by retiming the baseband data stream with the divided clocks of LO_I and LO_Q.

The MUX cell is built with 2-input NAND logic only. To eliminate the rising or falling time skew between the two inputs due to internal node charges, Fig. 5b shows a fully symmetric NAND gate, in which both inputs experience the same parasitic delay.

III. Wake-up Receiver with Offset Cancellation

A. Proposed Comparator Offset Cancellation

In Dickson-based WuRX configurations, N-stage envelope detector (ED) units are cascaded in a chain for voltage gain boosting whereas the input RF signal is equally AC coupled to each stage. In addition, the pseudo-differential structure provides 2x more gain where the polarity of diodes is reversed

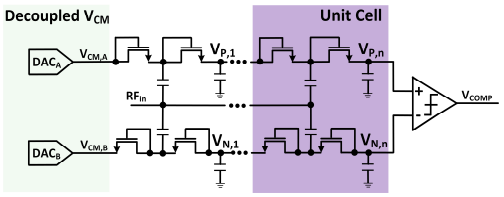


Fig. 6. Proposed wake-up receiver comparator offset cancellation.

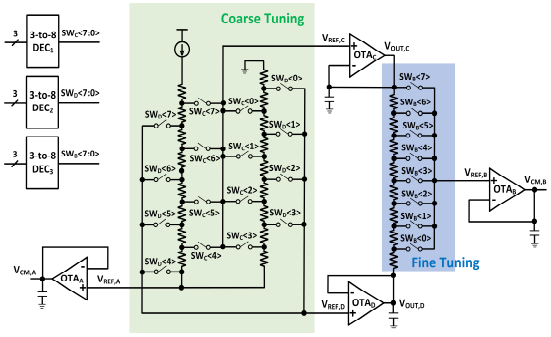


Fig. 7. Two-stage resistive DAC for common-mode voltage generation.

in the complementary path. However, the comparator offset can adversely affect the WuRX sensitivity advantage.

To reduce the comparator offset, instead of applying cancellation techniques such as current digital-to-analog converter (DAC), auto zeroing, or chopping that typically requires either high quiescent current or complementary clock phases, we propose a simple but nontrivial comparator offset cancellation topology (Fig. 6). It biases the common-mode levels of the pseudo-differential paths with two independently controlled DACs. The calibration is done by fixing the DAC_A code to the mid-code and adjusting the DAC_B code with respect to the DAC_A code to make the comparator output toggle. As a result, the comparator offset can be compensated and reduced to less than one least significant bit (LSB).

B. DAC Implementation

The DACs are implemented as a two-stage resistive ladder with coarse tuning and fine tuning, as shown in Fig. 7. Switches $SW_{B\text{-}D}$<7:0> are driven by one-hot 3-to-8 decoders $DEC_{1\text{-}3}$, respectively. Four operational transconductance amplifiers (OTA) are configured as unity-gain voltage buffers, where OTA_A and OTA_B outputs are connected to the envelope detectors, and OTA_C and OTA_D define the fine-tuning range.

C. Calibration Procedure

Despite its simplicity, the calibration procedure needs to be carefully designed as all the OTAs in DAC suffer from offsets. Before the RF signal arrives, the calibration procedure is described below.

1) STEP I: Calibration of Offsets Between OTA_C and OTA_D

This is achieved by reading the voltage difference $V_{\text{diff,CD}}$ between OTA_C and OTA_D via on-chip MUX and test pads. By switching DEC_1, DEC_2 respectively, different $V_{\text{REF,C}}$ and $V_{\text{REF,D}}$ get selected to bias OTA_C and OTA_D. The criteria to mark the completion is when both (5) and (6) are satisfied.

$$LSB_c < |V_{\text{diff,CD}}| \le 2LSB_c \tag{5}$$

$$\{V_{\text{out,C}} < V_{\text{CM,A}} \le V_{\text{out,D}}\} \text{ or } \{V_{\text{out,D}} < V_{\text{CM,A}} \le V_{\text{out,C}}\} \tag{6}$$

where LSB_c denotes the resolution of the coarse tuning. (5) ensures that the fine tuning would have >1 LSB_c tuning range. (6) guarantees $V_{\text{REF,B}}$ sitting around $V_{\text{CM,A}}$. More importantly, the code difference between DEC_1 and DEC_2 should be recorded and stay constant in all the following operations.

2) STEP II: Calibration of Offsets Between OTA_A and OTA_B

Although $V_{\text{REF,B}}$ is close to $V_{\text{CM,A}}$, owing to the offsets between OTA_A and OTA_B, the voltage difference $V_{\text{diff,AB}}$ between $V_{\text{CM,A}}$ and $V_{\text{CM,B}}$ may be greater than one LSB_c. This can be corrected by incrementing or decrementing the DEC_1 and DEC_2 simultaneously until (7) is met. It is noted that the DEC_1 and DEC_2 code difference obtained in Step I should be maintained and DEC_3 is still fixed at its mid-code.

$$|V_{\text{diff,AB}}| \le LSB_c \tag{7}$$

3) STEP III: Calibration of the Comparator Offset

The comparator output should be recorded once all the OTAs have been calibrated. Then the decoders DEC_1 and DEC_2 should be adjusted again until the comparator output gets flipped, indicating the input-referred offset is found. Next, the DEC_3 controlling SW_B<7:0> comes into play for fine tuning until the comparator output is observed flipped again. This marks the completion of the entire calibration process.

The post-calibration residual offset at the comparator input $V_{\text{res-os,p-n}}$ is given in (8), where LSB_c and LSB_f denote the LSBs of the coarse tuning and fine tuning, respectively.

$$V_{\text{res-os,p-n}} \le 2LSB_c \cdot \frac{1}{Fine\text{-}tune\ Level\ No.} = 2 \times LSB_f \tag{8}$$

Another key observation is that the total offset referred to the tap-point of the coarse resistor ladder that matters in determining the coarse tuning range is given in (9).

$$V_{\text{tot-os,1}\sigma} = \sqrt{V_{\text{os,COMP,1}\sigma}^2 + 2 \cdot V_{\text{os,OTA,1}\sigma}^2} \tag{9}$$

Equation (9) assumes that all four OTAs are identical which is the case in this design. Meanwhile, each of the OTAs only consumes 0.5 µA quiescent current. $V_{\text{os,COMP,1}\sigma}$ is 9.9 mV and $V_{\text{os,OTA,1}\sigma}$ is 7.1 mV based on the Monte Carlo simulations. From (9), the 3σ of the total offset is 42.2 mV and therefore the coarse tuning range is designed to cover ±50 mV around the nominal Vcm of 500 mV. Moreover, there are 16 voltage levels on the coarse tuning and 8 levels on the fine tuning. Based on (8), the residual offset is bounded within 1.56 mV.

A calibration algorithm implemented in Verilog-A proves the effectiveness of such technique and has achieved about 20 dB improvement of receiver sensitivity as shown in Fig. 8.

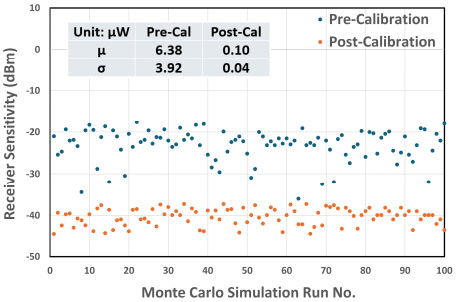


Fig. 8. Comparison of receiver sensitivity over Monte Carlo runs.

Table 1. Comparison with State-of-the-Art Backscatter Modulation Systems.

	ISSCC 2015 [2]	SenSys 2016 [3]	ISSCC 2019 [1]	JSSC 2020 [4]	**This Work**
Process (nm)	65	N/A	65	65	**180**
Center Frequency (GHz)	5.8	2.4	Ultrasound	2.4	**2.4**
Chip Core Area (mm^2)	0.26	N/A	0.25	0.34	**0.68**
Wake-up RX Sensitivity (dBm)	- 23	N/A	N/A	- 42.5	**- 39.9**
Power Divider	No	Yes	No	Off-chip	**On-chip**
SSB Modulation	No	Yes	No	On-chip	**On-chip**
Image Rejection Ratio (dB)	N/A	>20	N/A	17	**31.4**
Backscatter Power (µW)	113	33	28.8	28	**38.7**
Incident Wave Source	Single-tone CW	WiFi	Short pulse	WiFi	**Single-tone CW**
Reflected Wave RX	RFID reader	WiFi	ASIC	WiFi	**SDR**

IV. Characterization and Measurement Results

The backscatter IC is fabricated in standard 0.18-µm CMOS technology with a core area of 0.68 mm^2. With a 1.5 V supply, the wake-up receiver consumes 5.8 µW and the backscatter modulation system consumes 38.7 µW excluding the PLL. The PLL draws 35.1 µA from the on-chip LDO and exhibits -114.5 dBc/Hz phase noise at 1 MHz offset frequency.

To observe the frequency translation and characterize the image rejection, a 3-dB hybrid coupler is surface mounted on the PCB test board. It is configured to route the RF incident wave to the WPD through the 0^o port, and the reflected signal to the spectrum analyzer for observation at the isolated port. As a result, the path loss in addition to the signal power loss owing to backscatter modulation leads to a measured reflected power 19.65 dB lower than the incident power in Fig. 9, where the incident wave is sent at 2.4 GHz, the baseband data is an 800 kHz clock signal, and the reflected signal thus appears at 2.3742 GHz.

To verify the full functionality in real-time transmission mode, the backscatter system is tested with a commercial off-the-shelf software-defined radio (SDR), in which the SDR receiver front-end is tuned to 2.375 GHz and the SDR is configured as a quadrature direct-conversion demodulator. Fig. 10 demonstrates that the demodulated received data is a successful recovery of the transmitted data originating from the baseband pseudorandom binary sequence (PRBS) generator embedded in the backscatter IC.

V. Conclusion

This paper presents a prototype of a miniature backscatter IC working at 2.4 GHz with superior image rejection and excellent receiver sensitivity. Compared to other state-of-the-arts (see Table 1), our proposed design has achieved full functions by integrating Wilkinson power divider, backscatter modulation system, wake-up receiver, frequency synthesizer and LDO. The backscatter IC fabricated in the 0.18-µm CMOS process demonstrates a 31.4-dB IRR and -39.9 dBm sensitivity for the 2.4 GHz incident wave. It occupies a core area of 0.77×0.88 mm^2 and consumes only 44.5 µW excluding the PLL and LDO. Such highly integrated design allows the backscatter system to be directly integrated with the on-chip analog front-end and data digitizer for applicability in IoT, wearable and implantable biomedical devices.

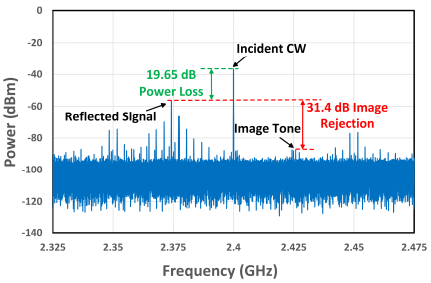


Fig. 9. Measured spectrum of incident and reflected waves.

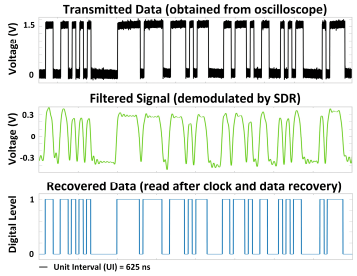


Fig. 10. Waveform of transmitted and received data.

References

[1] M. M. Ghanbari, D. Piech, K. Shen, S. F. Alamouti, C. Yalcin, B. C. Johnson, J. M. Carmena, M. M. Maharbiz, and R. Muller, "17.5 A 0.8mm^3 Ultrasonic Implantable Wireless Neural Recording System With Linear AM Backscattering," *2019 ISSCC*, pp. 284–286.

[2] A. Shirane, H. Tan, Y. Fang, T. Ibe, H. Ito, N. Ishihara, and K. Masu, "13.8 A 5.8GHz RF-powered transceiver with a 113µW 32-QAM transmitter employing the IF-based quadrature backscattering technique," *2015 ISSCC Digest of Technical Papers*, pp. 1–3.

[3] P. Zhang, D. Bharadia, K. Joshi, and S. Katti, "HitchHike: Practical backscatter using commodity WiFi," *Proc. ACM Conf. Embedded Netw. Sensor Syst. (SenSys)*, pp. 569–571, Nov. 2016.

[4] P. P. Wang, C. Zhang, H. Yang, M. Dunna, D. Bharadia, and P. P. Mercier, "A Low-Power Backscatter Modulation System Communicating Across Tens of Meters With Standards-Compliant Wi-Fi Transceivers," *IEEE JSSC*, vol. 55, no. 11, pp. 2959–2969, Nov 2020.

[5] F. Wang and H. Wang, "An N-way transformer based Wilkinson power divider in CMOS," *2016 IEEE MTT-S IMS*, pp. 1–4.

[6] J. Moody and S. M. Bowers, "Triode-mode Envelope Detectors for Near Zero Power Wake-up Receivers," *2019 IEEE MTT-S International Microwave Symposium (IMS)*, pp. 1499–1502.

[7] Y. Lu, Y. Wang, Q. Pan, W. H. Ki and C. P. Yue, "A Fully-Integrated Low-Dropout Regulator With Full-Spectrum Power Supply Rejection," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 3, pp. 707–716, March 2015.