Demonstration of Effective Intrinsic Electron Velocity $>10^7$ cm/s in Ultrawide Bandgap $Al_{0.64}Ga_{0.36}N$ Channel HEMTs

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***Abstract*— This article reports on the effective intrinsic electron velocity exceeding 10^7 cm/s in high-composition $Al_{0.64}Ga_{0.36}N$ channel high-electron-mobility transistors (HEMTs) at peak f_t. The small-signal two-port *s*-parameter measurements were employed at peak f_t bias, which enabled us to compute the small-signal parameters and determine the total transit delay. A device with ∼245-nm gate length yielded a total transit delay of 8.04 ps corresponding to a peak f_t of 19.8 GHz. By segregating the delay components, the intrinsic delay was estimated to be 6.22 ps. However, this intrinsic delay includes the effect of fringe capacitances that were further decoupled to yield the intrinsic transit time. The transit time under the gate was estimated to be 2.12 ps, and thus, the peak effective intrinsic electron velocity was determined to be 1.15×10^7 cm/s. These findings offer crucial insights for optimizing the design and performance of high-composition AlGaN channel HEMTs at RF power frequencies.**

***Index Terms*— AlGaN, electron velocity, high-electron-mobility transistor (HEMT), small signal, transit delay.**

I. Introduction

AlGaN channel high-electron-mobility transistors (HEMTs) are increasingly studied due to their superior properties over GaN. While GaN HEMTs have shown promising characteristics, such as breakdown fields in the range of 1–1.5 MV/cm, state-of-the-art transport properties with mobilities up to 2000 $cm^2/V{\cdot}s$, and electron saturation velocity (v_{sat}) up to $\sim 2 \times 10^7$ cm/s [1], [2], [3], [4], AlGaN channel HEMTs have the potential to offer superior performance due to its wider bandgap and higher critical electric field, reaching up to 4 MV/cm [5], [6]. This is further validated by the higher Johnson's figure of merit (JFOM $= E_{crit} \cdot v_{eff}/2\pi$) observed for AlGaN channel with Aluminum composition >50% compared to GaN [7], [8], [9], [10]. Consequently, there have been multiple reports of AlGaN (Al > 50% channel) channel HEMTs; however, the development as well as performance is still in the early stages [5], [11], [12], [13], [14], [15], [16], [17].

The cutoff frequency (f_t) directly depends on the electron velocity and is hence considered to be a crucial parameter to evaluate the suitability of a semiconductor for high-frequency operation. One of the widely used methods for determining peak electron velocity follows Moll's analysis based on f_t, although this is limited to one bias condition for peak velocity [18], [19]. In addition, techniques, such as two-terminal transmission line model (TLM)-like structures and Hall measurements, aim to construct velocity-field curves but rely on assumptions regarding channel charge density remaining constant at both low field and high field regimes [4], [20]. In this regard, drain delay analysis is a robust method that isolates the electron velocity constituents by examining the time delay between drain current onset and voltage application. Although this method requires precise analysis of the device parasitics, it can be well established as the measured *s*-parameters can be used to compute the small-signal parameters and thereby estimate the effective intrinsic electron velocity [15], [22], [23], [24]. Another advantage of this drain delay analysis is that this method accounts for delays due to various scattering mechanisms and hence need not be modeled separately. The drain delay method has been utilized extensively in GaN channel HEMTs to estimate the effective intrinsic electron velocity [21], [22], [23], [24].

In AlGaN channel HEMTs, extrinsic electron velocity has been estimated by a few studies, and however, there is no report of experimental studies on evaluating as well as extracting the intrinsic velocity of AlGaN channel HEMTs [10], [25], [26]. The intrinsic velocity is an important parameter to

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validate the theoretical advantage offered by AlGaN channel HEMTs. Nanjo et al. [25] have demonstrated extrinsic electron saturation velocity of 4.3 × 10^6 cm/s in 40% AlGaN channel HEMT for 1-μm gate length device with f_t of 7 GHz. Another study by Ye et al. [26] has demonstrated extrinsic effective channel velocity up to 2.66 × 10^6 cm/s for short gate length devices (<1 μm) in 45% AlGaN channel HEMTs [26]. In the high-composition regime, Klein et al. [10] have shown an extrinsic saturation velocity of 3.6 × 10^6 in 70% AlGaN channel HEMTs. The reported numbers are still far lower than the theoretical predictions from Monte Carlo, which demonstrates the saturation velocity between 2 × 10^7 cm/s and 2.25 × 10^7 cm/s for AlGaN channel HEMTs with AlGaN composition from 20% to 80% [27], [28]. One of the main reasons for this discrepancy is because the measured velocity still accounts for device parasitics, which needs to be modeled and accounted for to determine the actual time required to cross the gate length.

This work demonstrates a peak intrinsic velocity up to 1.15 × 10^7 cm/s in $Al_{0.64}Ga_{0.36}N$ channel HEMTs for a 245-nm gate length device using a drain delay analysis. This is one of the highest reported experimental electron velocities for AlGaN channel HEMTs. This velocity is close to the highest experimental velocity that has been achieved in GaN ~1.9 × 10^7 cm/s, validating the potential for higher JFOM in AlGaN owing to its wider bandgap and higher critical field [4], [7].

II. Epitaxial Structure and Device Fabrication

The epitaxial layers for the devices used in this analysis were grown using metalorganic chemical vapor deposition (MOCVD) on AlN on sapphire template [Fig. 1(a)]. A 23-nm-thick n-type doped $Al_{0.87}Ga_{0.13}N$ barrier was deposited, with a 30-nm heavily n-type doped reverse-graded layer from 87% to 40% for the ohmic contact. More details on the growth process and material properties can be found in [5]. The device fabrication process started with the fabrication of source and drain ohmic contacts. These were formed using a Zr/Al/Mo/Au metal stack followed by rapid thermal annealing (RTA). The details of the ohmic contact fabrication process can be found in [6]. The mesa isolation was achieved through a low damage chlorine-based reactive ion etching [29]. An I-shape gate was defined using electron beam lithography and PMMA/MMA bilayer resist stack followed by e-beam evaporation of Ni/Au (500/1500 Å). Probe pads were added using a Ti/Au (500/1500 Å) metal stack. The fabricated device with pads is shown in Fig. 1(b).

III. Results and Discussion

The reported devices in this work have a gate width (W_g) of 2 × 50 μm. Devices of varying gate lengths (L_g) between 210 and 275 nm were chosen for this study. The fabricated devices were first tested for ohmic contact linearity using a four-probe TLM. Linear ohmic contacts with a contact resistance (R_c) of 4.53 Ω·mm and sheet resistance (R_{sh}) of 2028 Ω/sq were obtained. These values are comparable to the state of the art R_c and R_{sh} reported previously [30], [31], [32],

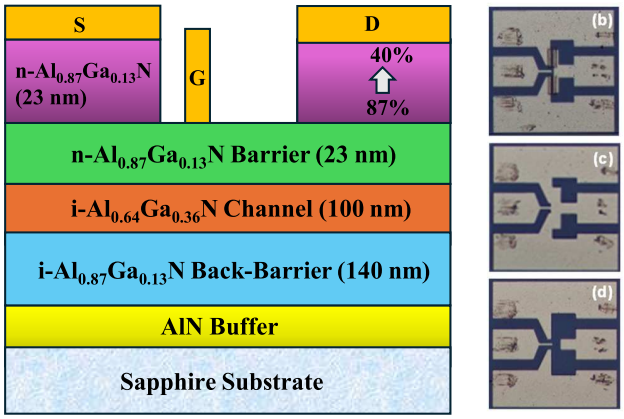

Fig. 1. (a) Device heterostructure of the 64% AlGaN channel HEMT. (b) Fabricated device with pads (W_g = 2 × 50 μm). (c) Deembedding structure for "short." (d) Deembedding structure for "open."

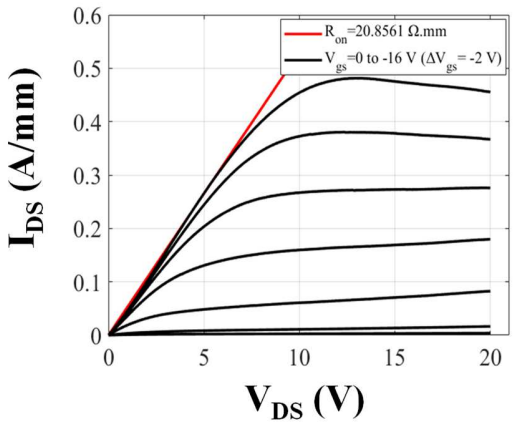

Fig. 2. I_d (A/mm) versus V_{DS} (V) for the $Al_{0.64}Ga_{0.36}N$ channel HEMT with I_{dmax} = 0.48 A/mm and R_{on} = 20.85 Ω and L_g = 245 nm.

[33]. For a device with L_g = 245 μm, the source-to-drain (L_{sd}) and source-to-gate (L_{sg}) lengths were measured as 3.15 and 0.87 μm, respectively. The dc output and transfer characteristics are shown in Figs. 2 and 3, respectively. The measured peak current density was around 0.48 A/mm, and R_{on} was 20.8 Ω. The devices had superior leakage characteristics and the ON/OFF current ratio (I_{on}/I_{off}) > 10^6 and limited by the noise floor of the instrument.

Small-signal two-port s-parameter measurements were performed to determine the peak f_t of the devices. The network analyzer was calibrated at the probe tips using the short-open-load-thru (SOLT) method with a commercial impedance standard substrate (ISS). On-wafer open and short structures employed for pad de-embedding are shown in Fig. 1(c) and (d). Fig. 4 displays the f_t and f_{max}, gain versus frequency plot for the different gate length devices biased at peak f_t.

For the previously reported device, the peak f_t measured was 19.8 GHz at a gate-to-source voltage (V_{GS}) of −6 V and drain-to-source voltage (V_{DS}) of 16 V. Fig. 5 portrays the contours of f_t at different bias conditions on the I–V plane. The measured s-parameters for this device are shown in Fig. 6. The small-signal parameters computed from the measured

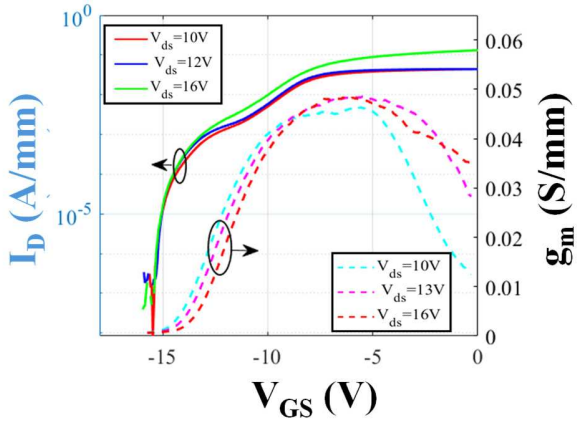

Fig. 3. DC transfer characteristics with I_d (A/mm) in log scale, $I_{on}/I_{off} > 10^6$, and transconductance g_m (S/mm) in linear scale.

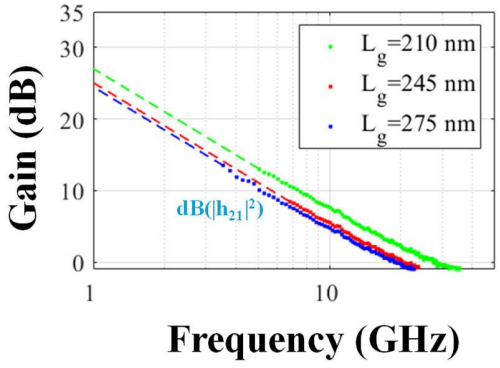

Fig. 4. Unilateral gain (U) and current gain $|h_{21}|$ measured at peak f_t bias versus frequency for different gate length devices selected for the analysis.

TABLE I
SMALL-SIGNAL PARAMETERS

Small Signal Parameters	Lg=210 nm	Lg=245 nm	Lg=275 nm
f_t (GHz)	25.3	19.8	19.2
g_m (mS)	6.80	5.77	5.62
C_{gs} (fF)	24.39	25.34	26.13
C_{gd} (fF)	10.02	10.58	11.01
C_{ds} (fF)	11.37	10.74	10.19
R_s (Ω)	65.27	63.04	71.35
R_d (Ω)	77.42	86.66	78.21
R_{ds} (Ω)	1012.69	1002.07	1060.48

s-parameters resulted in $C_{gs} = 25.34$ fF, $C_{gd} = 10.58$ fF, and $g_m = 5.77$ mS. R_s, R_d, and R_{ds} were found to be 63.04, 86.66, and 1002.07 Ω, respectively. Table I summarizes the small-signal parameters for different gate length devices selected for this work.

The velocity extraction procedure presented here is based on the delay model discussed [23]. The standard formation for f_t for a scaled FET is given by the following equation:

$$f_t = \frac{g_m}{2\pi\left[(c_{gs}+c_{gd})\left(1+\left[\frac{R_s+R_D}{R_{DS}}\right]\right)+g_m c_{gd}(R_s+R_D)\right]}. \quad (1)$$

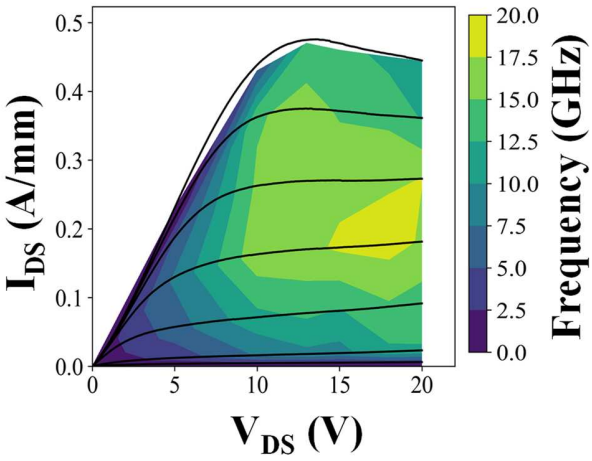

Fig. 5. Contours of f_t at different bias conditions, $V_G = 0$ to -16 V and $\Delta V_G = -2$ V.

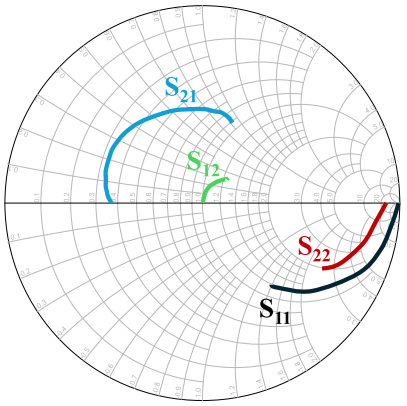

Fig. 6. Measured s-parameters from 45 MHz to 43.5 GHz for the device with gate length of 245 nm at peak f_t.

This equation can be rearranged to separate the associated delay terms as described by the following equation:

$$\begin{aligned}\tau_{\text{total}} &= \frac{1}{2\pi f_T} = \frac{c_{gs}+c_{gd}}{g_m} + \frac{c_{gs}+c_{gd}}{g_m}\frac{R_s+R_D}{R_{DS}} \\ &\quad + c_{gd}(R_s+R_D) \\ &= \tau_{\text{transit}} + \tau_r + \tau_{\text{miller}}. \end{aligned} \quad (2)$$

The total delay estimated from the measured f_t for 245-nm gate length was 8.04 ps. Small-signal parameters were used to calculate the individual delay terms, which together summed up to 8.73 ps. Ideally, the calculated delay should match the measured total delay of 8.04 ps for 245-nm gate length. This slight discrepancy can be attributed to the measurement and f_t estimation error. f_t calculated using small-signal parameters is 18.2 GHz, while the measured f_t is 19.8 GHz, indicating a reasonable agreement within the standard error bounds. The error between the calculated and measured f_t is around 8%. The electron velocity presented here is conservative, as it is estimated based on small-signal parameters derived from measured s-parameters. The total delay from small-signal parameters was 8.73 ps for 245-nm gate length and it encompasses intrinsic delay (τ_{int}), Miller effect (τ_{miller}), and resistor divider effect (τ_r) [6]. While delays due to resistor divider

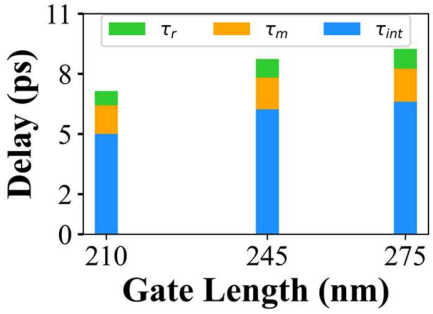

Fig. 7. Delay terms associated with the total measured delay τ_{tot} (ps) for different gate length devices.

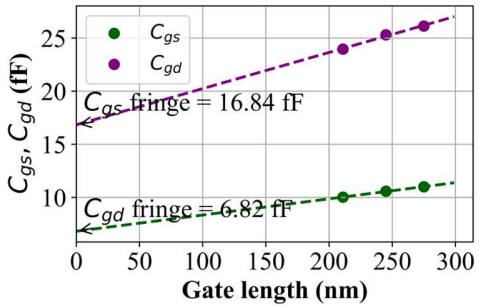

Fig. 8. Extraction of fringe capacitance.

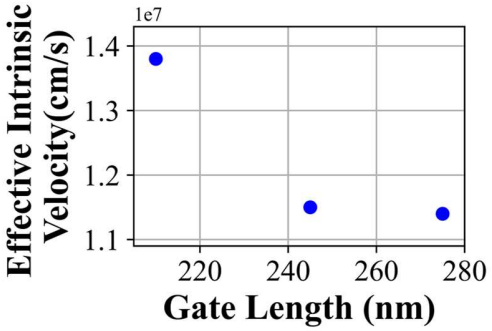

Fig. 9. Effective intrinsic velocity as a function of gate length at peak f_t.

effect (τ_r) and Miller effect (τ_{miller}) are caused by parasitics, they are decoupled from the total delay to yield the actual transit time from source to drain. τ_r and τ_{miller} were estimated as 0.93 and 1.58 ps, respectively, using small-signal parameters described in Table I. Fig. 7 shows the delay terms associated with the total measured delay for different gate length devices.

After decoupling τ_r and τ_{miller} from the total delay, the net intrinsic delay was found to be 6.22 ps. τ_{int} still accounts for the effect of fringing fields and therefore fringe capacitances and other parasitics. To decouple the effect of effect of fringing capacitance and other parasitics, C_{gs} and C_{gd} associated with τ_{int} are modeled as a linear combination of intrinsic and fringe capacitances given by the following equation:

$$\tau_{\text{transit}} = \tau_{\text{int}} + \tau_{\text{fringe}} = \frac{c_{\text{gs,int}} + c_{\text{gd,int}}}{g_m} + \frac{c_{\text{gs,fringe}} + c_{\text{gd,fringe}}}{g_m}. \tag{3}$$

$C_{\text{gs\_fringe}}$ and $C_{\text{gd\_fringe}}$ can be calculated using a linear fitting of C_{gs} and C_{gd} for different gate lengths and extrapolating the trendline at $L_{\text{g}} = 0$ nm, the y intercept shown in Fig. 8. Isolation of the fringe capacitances from the net transit time revealed the actual transit time under the gate as 2.12 ps. This enabled us to determine the effective peak intrinsic electron velocity given by (4) [34] as 1.15 $\times$ 10^7 cm/s for 245-nm gate length. Fig. 9 describes the effective intrinsic velocity as a function of gate length for three different gate lengths

$$v_{\text{eff}} = 2\pi f_t L_{\text{eff}} = \frac{L_{\text{eff}}}{\tau_{\text{transit}}}. \tag{4}$$

The 245-nm gate length was chosen to estimate the electron velocity, as the error between the delay terms was approximately 8%, while for other gate lengths, the error ranged from 10% to 11%. For the 245-nm gate length, using the actual measured delay, the estimated electron velocity is 1.71 $\times$ 10^7 cm/s. It is important to note that the electron velocity presented in this article is a conservative estimate. This approach was taken to account for potential measurement uncertainties, as the lower bound of f_t was used in all cases. Consequently, this may underestimate the maximum velocity.

Electric field saturation is crucial for optimizing the performance of AlGaN RF HEMTs for high-frequency applications. Monte Carlo simulations predict a critical field for velocity saturation around 0.2–0.4 MV/cm for AlGaN channels [28]. To accurately assess the electric field under the gate, TCAD simulations and analytical calculations in conjunction with the measurement data were performed. The simulated electric field profile, resulting from the TCAD simulation, shows an average electric field of approximately 0.67 MV/cm under the gate. To further validate the simulated data, an analytical calculation was performed. This procedure is based on subtracting the voltage drop due to contact resistances, source access, and drain access resistances from the applied drain bias. The resulting voltage under the gate was used to estimate the average electric field, which was found to be 0.65 MV/cm. The average electric field value with both TCAD simulation and calculations indicates that the device is operating near velocity saturation conditions [28].

The intrinsic effective electron velocity presented here seems to be in good agreement with the values predicted from Monte Carlo simulations [27], [28] as well as comparable to the highest experimental velocity achieved in GaN [4]. The estimated channel mobility, approximately 130 $\text{cm}^2/\text{V}\cdot\text{s}$, is discussed in detail in [5], providing insights into the measurement methods and procedures used. This unleashes the potential for AlGaN RF HEMTs with a higher JFOM. While improvements are still needed in growth and fabrication techniques, this benchmark will serve as a guideline for device design.

IV. Conclusion

This work demonstrated an effective intrinsic electron velocity exceeding 10^7 cm/s in $Al_{0.64}Ga_{0.36}N$ channel HEMTs optimized for RF power amplification in the K-band. A 245-nm gate length device achieved a peak f_t of 19.8 GHz with a total transit delay of 8.04 ps. After decoupling parasitic

delays, the actual transit time was 2.12 ps, yielding an electron velocity of 1.15×10^7 cm/s. These results align with theoretical predictions, setting new benchmarks for AlGaN RF HEMTs and highlighting their potential for high-frequency applications.

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