A DC to 25 MHz Current Sensing Interface for Hall-Effect Sensor

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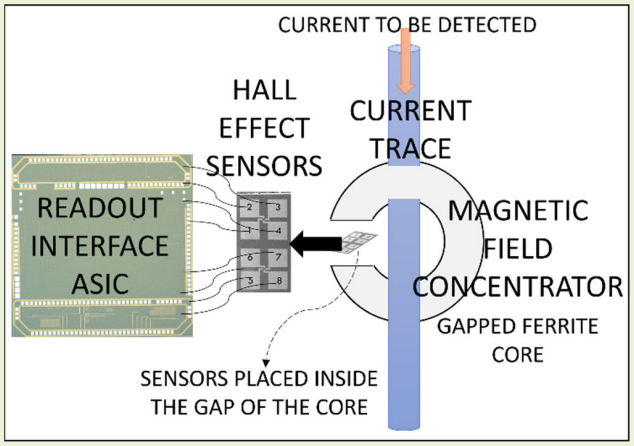
***Abstract*—A dc to 25 MHz readout interface (ROI) design for Hall-effect sensors is presented. The current sensing system is comprised of a high-bandwidth aluminum gallium nitride/gallium nitride (AlGaN/GaN) or aluminum gallium arsenide/gallium arsenide (AlGaAs/GaAs) Hall-effect sensor and an on-chip fast ROI. The interface makes use of multisignal paths, utilizing a two-way current spinning technique to minimize offset at dc while using high- pass filtering to eliminate offset at the high frequencies. The usage of two sensors and signal paths makes it possible to take advantage of the full bandwidth of the sensor. The summed output is the desired high- bandwidth signal proportional to the current or the magnetic field to be detected. The system achieves a rise time of 40 ns in response to a current pulse, resulting in a noninvasive fast current detection solution. The die area of the ROI is 2850 by 200 μm. When testing with a current trace at 1.5 mm from the sensor and using a ferrite-core magnetic field concentrator, the current sensitivity is observed to be 12.7 mV/A.**



***Index Terms*—Hall-effect devices, magnetic-field sensors, sensor readout circuits, sensor signal conditioning.**

I. Introduction

HALL-EFFECT sensors are magnetic field sensors. Corresponding to their biasing, they generate a voltage proportional to the magnetic field's strength [1]. Their applications range from the automotive industry to primary consumers. Hall-effect sensors are the most prevalent magnet sensors with ∼70% market share in 2017 [2].

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One of the most common uses of these sensors is current sensing [1]. When current flows through a conductor, it creates a magnetic field around it. The Hall-effect sensor has a current flowing inside it when biased. When the sensor is placed close to the current line, the external magnetic field coincides with the Hall-effect sensor's internal current and Lorentz force generates a potential across the opposite terminals of the sensor. This is called the Hall-effect signal (or Hall-effect voltage).

The Hall-effect sensors have an inherent offset, which is the sensor's output when no external magnetic field is present. This output should be ideally zero, but practically, the output voltage present in zero magnetic field when the sensor is biased is called Hall-effect offset [3]. Various studies have been conducted on multiple shapes and sizes of these devices to mitigate this offset [3], [4], [5]. However, the offset may be low for some devices and high for others, but it always exists. Hence, it needs to be compensated in the readout interface (ROI).

The type of Hall-effect sensor ROI initially depends upon the output, whether it is current or voltage. It is categorized as either current mode [6], [7], [8] or voltage mode [9], [10], [11], [12], [13]. Another categorization is based on whether the output is digital [14], [15], [16], [17], [18], detecting certain current levels, requiring high sensitivity and accuracy. While

in many applications, the analog output is preferred [6], [7], [8], [9], [10], [11], [12], [13]. For each of these categories, no matter what final output is desired from the Hall-effect sensor, the most critical design step in the ROI is to nullify the Hall-effect offset. For this purpose, initially, the Hall-effect offset voltage needs to be separated from the Hall-effect signal. A vastly used commercial technique for this purpose is the current spinning technique [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22]. This becomes the first stage of the ROI.

Following the current spinning stage, various dynamic offset cancellation techniques [23] can be employed, including chopper stabilization (CHS), autozeroing, track-and-hold, and other techniques. Using these cancellation techniques, a variety of ROI designs can be seen in the literature. One such ROI uses sample and hold circuitry for demodulation [11], [14], [16], which provides a highly sensitive signal but more complex circuitry than a chopper. Another design uses analog-to-digital converters (ADCs) with feedback loops to obtain low offset errors [15], forming a complex signal conditioning system. One ROI uses ADC, which takes input directly from current spinning [9], and requires internal offset compensation for the OpAmps and a very high-resolution ADC. Another simulated design offers a solution for reducing residual offset as discussed in [7], [8], and [12], where four phases are used and correlated double sampling for further subtraction of offset. Of all these ROIs, the most effective is the CHS in combination with current spinning [6], [10], [13], [17], [24], [25]. This can provide high sensitivity with sufficiently low flicker noise while effectively reducing inherent offsets of the OpAmps as well. However, the chopping adds switching noise in the signal, and one technique to reduce that is to eliminate demodulation choppers [19]. This improves the signal-to-noise ratio (SNR) but provides modulated ac Hall-effect signal as the output.

All the above ROIs use those dynamic offset cancellation schemes that limit the system's bandwidth. One high-frequency technique is a current spinning method followed by three ripple reduction loops instead of a low-pass filter [20]. This allows full system bandwidth, although it requires a complicated multiplex signal conditioning system, including data converters. Another method that provides high bandwidth is by combining CHS with track and hold comparators [21]. It uses sampling techniques to eliminate offset rather than filters. Another work [22] represents an X-Hall-effect sensor that is orthogonally shaped and uses a differential-difference current feedback amplifier. This sensor avoids using current spinning, allowing full practical bandwidth of the system. However, it can only be used for orthogonal-shaped sensors with eight terminals, which requires rearchitected sensor and the entire circuitry along with it. One technique recently developed allowed the separation of the Hall-effect signal from offset without using current spinning [26] but could only work for ac magnetic fields and cannot detect the dc signal. Other high-bandwidth sensing options then explore various other sensors, such as coils and magnetoresistance transducers [27], instead of Hall-effect sensors.

Most of the ROIs mentioned above utilize current spinning to differentiate between the Hall-effect offset and the Hall-effect signal. Following that step, some techniques focus on improving sensitivity or linearity, while others focus on decreasing the residual offset. There is limited work for bandwidth improvement of ROIs for Hall-effect sensors. The ROI architecture designed in this work focuses on increasing the bandwidth performance of the circuit by using two signal paths. This ROI, when combined with any high-bandwidth Hall-effect sensors, results in a fast current detection system. This system can be designed using any wide bandgap devices, such as aluminum gallium nitride/gallium nitride (AlGaN/GaN) [28] or aluminum gallium arsenide/gallium arsenide (AlGaAs/GaAs) [29] Hall-effect devices.

Another work [32] that focuses on bandwidth improvement has shown the performance of the system up to 400 kHz when using Hall-effect devices. The band limit of the high-frequency signal path in the referred paper is defined by the bandwidth of the amplifiers, which is 400 kHz. The amplifiers designed for the work presented in this article have a higher bandwidth, resulting in a system performance of 25 MHz with AlGaAs/GaAs Hall-effect sensors and a bandwidth of 40 MHz alone. Second, the implemented technique for offset removal is different in the referred paper. The impact of the spinning current modulator is removed from the frequency band of the system using the ripple reduction loop in the referred paper. This is simplified in the work presented in this article by using a modified CHS technique with a spinning frequency ten times the bandwidth of the low-frequency path of the system. This helped remove the ripple generated by the spinning frequency using a low-pass filter in the design, avoiding the complexity of the design while also reducing the chip area and potentially cost.

Section II covers the architecture of the designed ROI, followed by the circuit schematic and its details in Section III. The ROI simulation results are presented in Section VI. The measurement results of the designed and fabricated ROI Application Specific Integrated Circuit (ASIC) and sensor testing are discussed in Section V. This is followed by comparing the results with the state-of-the-art designs in Section VI.

II. Architecture of the Proposed ROI

Hall-effect sensors detect magnetic fields and generate a corresponding output voltage. Since a current-carrying conductor produces a magnetic field around it, these magnetic sensors can detect the current flowing through that conductor. Conventional Hall-effect sensors provide high magnetic field sensitivity but limited bandwidth. The state-of-the-art AlGaN/GaN Hall-effect sensors [28] have a bandwidth of greater than 10 MHz. Such sensors can thus be used to detect fast magnetic field variations. Due to their miniature size, they can be used in integrated power applications [30] to detect currents. Whenever there is an abrupt fluctuation in the current flowing through a conductor, these Hall-effect sensors can detect that rapid change and respond quickly because of their high bandwidth. Catastrophic failure in high-power devices caused by current fluctuations can thus be avoided. For such a scenario, the circuit reading the signal from the sensor must also have a high system bandwidth. Due to various design limitations, the commercially available ROI circuits do not

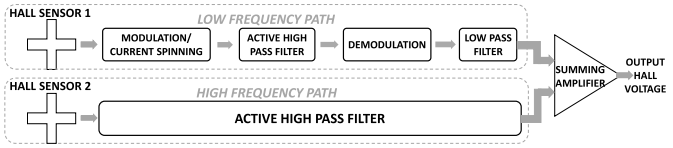

Fig. 1. Architecture of the designed readout interface circuit.

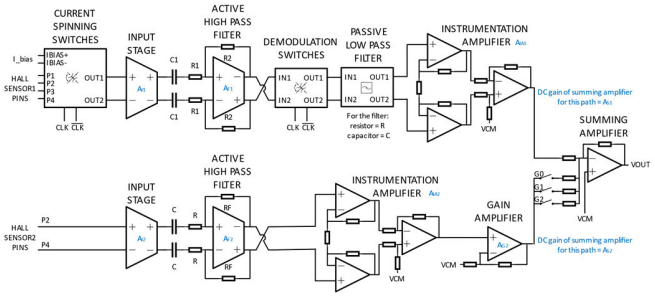

Fig. 2. Schematic of the designed readout interface.

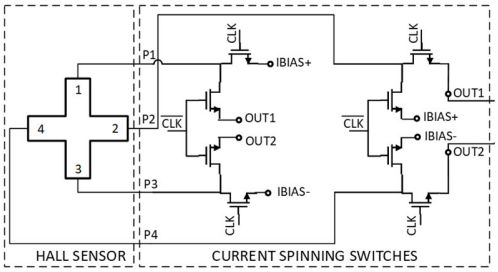

Fig. 3. Two-way current spinning switches.

provide high bandwidth. This gives rise to the need for an ROI circuit that can be used with such high-bandwidth Hall-effect sensors without limiting the system bandwidth.

Fig. 1 shows the block diagram of the architecture of the current sensing interface circuit designed in this work. The overall signal is divided into two signal paths. The low-frequency path comprises the current spinning technique to separate the Hall-effect offset from the Hall-effect voltage. This is followed by a modified version of the CHS technique to process the modulated Hall-effect voltage and remove the Hall-effect offset. The second path of this design is the high-frequency path. This uses a high-pass filter to remove the Hall-effect offset and the low-frequency components of the Hall-effect voltage. Hence, only the high-frequency components are processed and allowed to pass in this signal path. This way, both the signal paths are devoid of offset and contain a certain frequency portion of the Hall-effect voltage. In the end, a summing amplifier is used to add these two signals to obtain the final Hall-effect voltage.

The division of the signal into two paths is done to be able to amplify the signal and efficiently remove the offset. Hall-effect offset is present in the signal generated by the Hall-effect devices, due to unavoidable structural mismatches. It varies from one device to another as well as with temperature. Hence, signal conditioning methods must be applied to the output generated by the sensor to remove this offset. Two methods are required to remove this offset. The current spinning technique is the method used in the low-frequency path. Although this technique limits the usable bandwidth and hence cannot be applied to high-frequency signals. Similarly, filtering is applied in the high-frequency path to remove the offset, but it also rejects the low-frequency components and hence cannot be used in the low-frequency path. This necessitates the use of two signal paths with two different methods for offset cancellation, to be able to process a wider frequency range.

The low-frequency path is a combination of two techniques, namely, current spinning and CHS. CHS is a signal conditioning method that works in the frequency domain. It first modulates the desired signal on a high-frequency carrier. Then, during amplification, the OpAmp offset gets added to the signal as well as any flicker noise. Although the offset is a low-frequency signal and does not interfere with the desired modulated signal, the desired signal is then demodulated to its original form, whereas since the offset also passes through the demodulation switches, it gets modulated. Low-pass filtering then removes the modulated offset as well as any noise. This way, CHS gets rid of the offset and flicker noise. Since CHS technique is implemented using fully differential signal propagation, it facilitates the rejection of common-mode and environmental noise. The addition of current spinning to this technique is due to the Hall-effect sensor. The current spinning replaces the modulation block of CHS, as shown in Fig. 1. The current spinning partially works similar to the modulation block, such that it modulates the desired Hall-effect voltage. Although in addition to that, it also separates the Hall-effect offset by leaving it unmodulated.

III. Schematic of the Designed ROI

The circuit schematic of the ROI is shown in Fig. 2. The top branch is the low-frequency path, while the bottom branch is the high-frequency path. Hall-effect sensor#1 is connected to the top branch through the current spinning block, which is elaborated in Fig. 3. There are two phases controlled by clock signals (CLK and $\overline{\text{CLK}}$). When CLK is high, during phase#1, terminals 1 and 3 of the Hall-effect sensor are connected to the bias current, while terminals 2 and 4 are connected to the output of this block. Next, when $\overline{\text{CLK}}$ is high, during phase#2, the connections of the terminals switch up, such that the bias current is now provided to terminals 2 and 4, while the output is taken from terminals 1 and 3. Due to the switching from phase#1 to phase#2, the polarity of the measured Hall-effect voltage changes in the two phases. Whereas since the offset is due to structural mismatches and is being measured between two terminals in both phases, it remains unaffected by the switching. As a result, a modulated Hall-effect voltage is generated, whose frequency is the same as the clock frequency, and the Hall-effect offset remains a low-frequency discrete (dc) signal.

The rest of the circuit chain consists of operational transconductance amplifiers (OTAs) in fully differential (Fig. 4) or single-ended (Fig. 5) configurations. The first stage for both these OTA is designed using the folded-cascode configuration. This type of OTA uses cascode devices for high gain and high bandwidth. Compared to other cascode configurations, folded-cascode provides a large swing without compromising on gain or bandwidth. This results in high output common-mode range

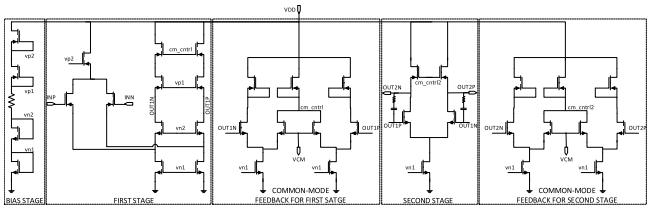

Fig. 4. Fully differential OTA.

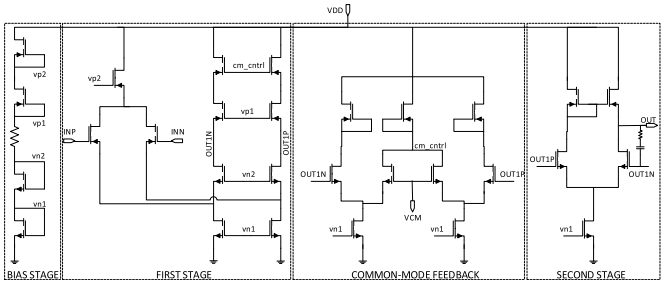

Fig. 5. Single-ended OTA.

(OCMR). The folded-cascode configuration also provides a high-power supply rejection ratio (PSSR).

When designing a fully differential OTA (Fig. 4), it requires a common-mode feedback stage to support each gain stage, since it has differential outputs. The purpose of the common-mode feedback circuit is to establish an appropriate current in each branch while maintaining the correct output common-mode voltage (VCM) of both output nodes. This stage deduces the output VCM by averaging the two output nodes and then compares it with the reference VCM. As a result, it generates the required control voltage for the p-channel metal oxide semiconductor (PMOS) device current source of the folded-cascode stage. Thus, by controlling that bias current, it keeps the output VCM close to VCM through this feedback loop.

The next stage of the fully differential OTA (Fig. 4) is the differential amplifier. This stage further increases the gain of the OTA. Since this stage also needs to have differential outputs, hence, a similar common-mode feedback stage is required for this gain stage as well.

The single-ended OTA (Fig. 5) also uses the folded-cascode as the first stage and a differential amplifier as the second stage. Since, in this OTA, the output is single-ended, there is no need for a common-mode stage for the second stage. However, as can be seen in (Fig. 5), the first stage is designed to be fully differential. This helps in keeping the output VCM more accurate since the common-mode feedback circuit maintains it.

Indirect Miller compensation scheme is used in both the amplifiers. Miller compensation uses a capacitor between the output and the input of the second stage, bypassing this stage for high frequencies. This causes pole splitting due to multiplication of capacitance and adds a dominant pole in the amplifier. For indirect Miller compensation scheme, a series resistor is added with the capacitor to add a zero, which increases the bandwidth of the amplifiers, as compared to using only Miller scheme. The stability of the amplifiers is ensured by designing them with a phase margin of greater than 50°.

From the schematic in Fig. 4, it can be seen that the input stage and the active high pass filter of both signal paths are fully differential. Hence, these stages use the fully differential OTA. Any other stage that has an amplifier uses the single-ended OTA.

Considering the low-frequency path, the first block is the current spinning, where the Hall-effect voltage gets modulated to the switching frequency (the frequency of the CLK signal), while the offset remains dc. This signal is then picked up by the fully differential input stage, which serves as a preamplifier stage, with high input resistance. Since the desired Hall-effect voltage is modulated to a high frequency, the next stage is an active high-pass filter, which then rejects the dc Hall-effect offset and amplifies the Hall-effect voltage. Since amplifiers are used in this chain, a dc offset of the OTA gets added to the signal. After filtering, the Hall-effect voltage is demodulated using the same switching frequency (CLK) back to its original form. However, the amplifier offset gets modulated when passed through the demodulation switches. Then, the signal is passed through a low-pass filter to reject the modulated offset as well as the high-frequency switching noise. A passive low-pass filter is used. The final signal at this stage is only the amplified Hall-effect voltage in its original unmodulated form. However, this is a fully differential signal, so it is passed through an instrumentation amplifier to convert it into a single-ended output. The offset of the amplifiers of this stage does not have any significant effect on the signal since the Hall-effect voltage is already amplified. Additionally, common-centroid techniques are implemented to minimize it.

The high-frequency signal path is simpler than the low-frequency path since no current spinning is required here. The reason is that no dc voltage needs to be processed in this signal path, and current spinning is needed to separate the dc Hall-effect voltage from the dc Hall-effect offset. The input stage is a fully differential amplifier with very high input resistance, so that it does not load the sensor. This is the preamplifier stage for this signal path providing a low gain but high input resistance and bandwidth. Then, the active high-pass filter provides gain and filters the offset. The use of a fully differential amplifier helps reduce noise. At this point, the output is the high-frequency components of the amplified Hall-effect voltage without any offset. Since it is a fully differential signal, an instrumentation amplifier converts it to single-ended output. The last stage in this path is the gain stage. Since this is a high-bandwidth signal path, the gain of the amplifiers is lower as compared to the low-frequency signal path. Hence, a gain stage is used to amplify the high-frequency signal further.

The final stage of the system is a summing amplifier. This stage takes input from both signal paths and adds them with appropriate gain. An inverting weighted summing amplifier configuration is used. In this configuration, a different gain can be set for the two inputs by adjusting the input resistor values. Another feature added to this stage is gain variability for the high-frequency signal using three gain bits, as shown in Fig. 2. The low-frequency signal path gain is fixed, while the high-frequency gain can be slightly adjusted to match it. This feature is added to cater to any mismatches between the two signal amplitudes.

To achieve the transfer function for the system shown in Fig. 2, assume the low-frequency path as path#1 and the high-frequency path as path#2. The dc gain of each block is mentioned in Fig. 2. Let $V_i(s)$ and $V_{\rm OS}$ represent the input signal and offset, respectively. The modulation block shifts the center frequency of the signal to a higher frequency called the carrier or switching frequency (w_S). This block only modulates the input signal, while offset remains a dc signal, which is given by

$$V_i\,(s + jw_S) + V_{\rm OS}.$$

After it passes through the input stage (whose gain is represented by A_{I1}) and an active high-pass filter, it becomes

$$-A_{I1}\frac{R_2}{R_1}\left[\frac{sR_1C_1}{1+sR_1C_1}\right]\left[V_i\,(s + jw_S) + V_{\rm OS}\right].$$

Since the input frequency is modulated at a higher frequency, the pole and zero of the high-pass filter do not affect this signal ($w_S \gg (1/R_1C_1)$). The zero exists at the zero frequency and it eliminates $V_{\rm OS}$, which is the dc signal. The output after high-pass filter is given by

$$-\frac{R_2}{R_1}V_i\,(s + jw_s) * A_{I1}.$$

The demodulator shifts the input signal frequency back to its origin and the output is given by

$$-\frac{R_2}{R_1}V_i\,(s) * A_{I1}.$$

Hence, the transfer function before the low-pass filter is given by

$$-A_{F1} * A_{I1}$$

where $A_{F1} = (R_2/R_1)$.

The complete transfer function for path#1 is given by

$$\text{TF}_1 = -A_{F1} * A_{I1}\frac{1}{1+sRC} * A_{IA1}.$$

Similarly, the transfer function for path#2 is given by

$$\text{TF}_2 = A_{I2} * \left[-\frac{R_F}{R}\right]\frac{1}{1+\frac{1}{sRC}} * A_{IA2} * A_{G2}.$$

The final transfer function of the summed output is

$$\text{TF} = -\left[A_{S1}\,(\text{TF}_1) + A_{S2}\,(\text{TF}_2)\right] * \frac{1}{1+\frac{s}{p_d}}.$$

The 3-dB bandwidth is represented by the dominant pole of the summing amplifier, which is given by

$$p_d = \frac{g_{m_1}}{A_L C_c}.$$

During this transfer function analysis, only the most dominant pole is shown for simplicity. The rest of the amplifiers have poles equal to or greater than this pole.

Solving for the final transfer function

$$A_x = -\left[A_{S1} * A_{IA1} * A_{F1} * A_{I1}\left(\frac{1}{1+sRC}\right) - A_{S2} * A_{G2} * A_{IA2} * A_{F2} * A_{I2}\left(\frac{sRC}{1+sRC}\right)\right]$$

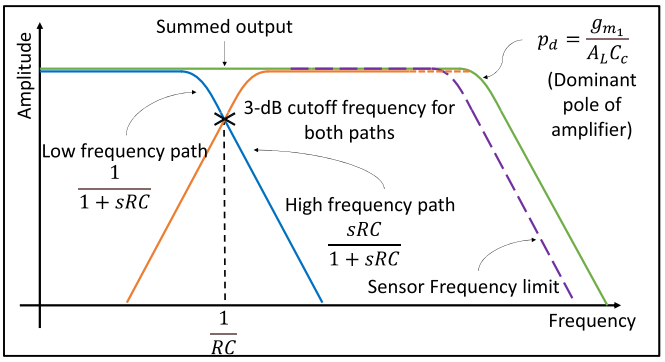

Fig. 6. Transfer function of the readout interface.

where $A_{F2} = (R_F/R)$.

The total gain of both the paths is kept equal

$$A_{S1} * A_{IA1} * A_{F1} * A_{I1} = A_{S2} * A_{G2} * A_{IA2} * A_{F2} * A_{I2} = A_v$$

$$A_x = -A_v\left[\frac{1}{1+sRC} + \frac{sRC}{1+sRC}\right]$$

$$A_x = -A_v\left[\frac{1+sRC}{1+sRC}\right] = -A_v.$$

The poles of the low- and high-frequency paths cancel out, reducing the final transfer function to

$$\text{TF} = \frac{A_v}{1+\frac{s}{p_d}}.$$

From the transfer function analysis, it can be determined that the bandwidth of the ROI circuit is dependent on the OpAmps and is not limited by the filters. By keeping the *RC* (resistor and capacitor) value and in turn, the filters' cutoff frequency of both paths the same, the effect of the poles and zeros of the filters cancels out in the final output. Then, also matching the gain of both the paths results in a smooth crossover. The simplified transfer function equation of the final output shows that the gain remains constant throughout the frequency range, having a smooth crossover, and the bandwidth is only limited by the dominant pole of the OpAmps. The transfer function is graphically depicted in Fig. 6.

IV. Simulation Results

The ROI is implemented on 180 nm XFAB XH018 (modular mixed-signal sensor CMOS) technology. The circuit was designed using 3.3 V ultralow-noise transistors supporting an extended temperature range of −40 °C to 175 °C.

The fully differential OTA is designed with 83.51 dB dc gain and exhibits a 329.4 MHz unity gain bandwidth (for a load of 100 fF). It has a current consumption of 527.6 μA, while the single-ended OTA has 80.82 dB dc gain and shows a unity gain bandwidth of 150.2 MHz (for a load of 100 fF) and 430.1 μA current consumption. Both the OTAs have an input and output VCM of 1.65 V and a phase margin of greater than 50°.

Using a supply voltage of 3.3 V, the VCM was kept at midrail (1.65 V). The circuit was designed and simulated after parasitic extraction (PEX). The switching frequency is

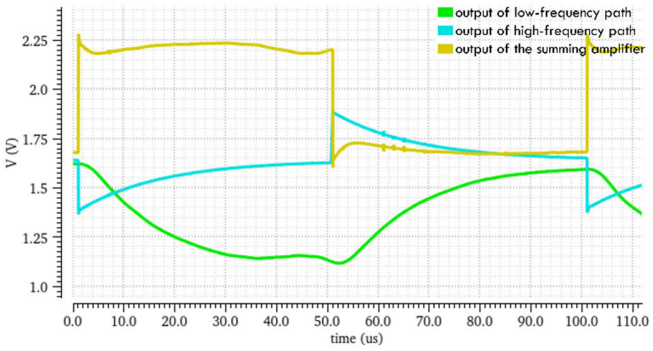

Fig. 7. Transient simulation of the readout interface.

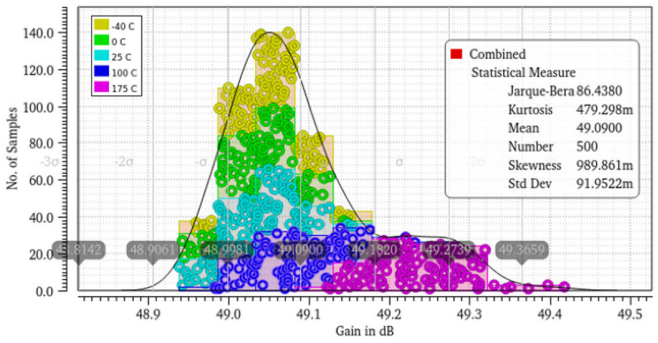

Fig. 8. AC Monte Carlo analysis of the readout interface.

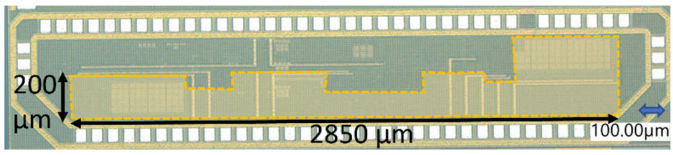

Fig. 9. Chip micrograph of the readout interface.

designed to be 250 kHz. For the simulation, the input pulses of 10 kHz and 2 mV were provided to both signal paths. An external dc offset of 100 mV was also added to the input for the purpose of testing. With no input, the output of the circuit is at the reference output VCM of 1.65 V. The transient simulation result for this test is shown in Fig. 7. The 3-dB frequency of the low-frequency path is decided by the low-pass filter in that chain, while the active high-pass filter decides the 3-dB frequency in the high-frequency signal path. During design, both these frequencies were kept the same to achieve a constant final output. This frequency is called the crossover frequency, which is observed to be 11.6 kHz. The crossover frequency is chosen to be approximately a decade less than the spinning frequency, so that the spinning frequency is efficiently rejected from the low-frequency path. Both filters are designed with the same resistor and capacitor values to match the frequencies and get a smooth crossover. To minimize the effect of filter components' tolerance on the crossover frequency, the same resistor and capacitor type with similar values and filter order is used. The layout of the devices is also optimized to minimize the process variation. As shown in Fig. 7, the rise time of both signal paths is ∼30 μs. The final output from the summing amplifier can be seen as a combination of both signals, giving a fast pulse response. Since an inverting configuration is used for the summing amplifier, it is inverse when compared to the signal from the two paths; however, it is in phase with the input.

Considering the gain, the high-frequency path has a gain of ∼126 V/V, while the low-frequency path has a gain of ∼280 V/V. Hence, a gain of 2.2 V/V is provided through the weighted summing amplifier to the high-frequency signal, while the low-frequency signal is added with a gain of 1 V/V. This is where the 3-bit gain variability comes in. The high-frequency gain can be selected using 3-bits G0, G1, and G2, as shown in Fig. 2. These bits provide a respective gain of 2.85, 2.22, and 1.82 V/V. The default setting is G1. In case of a significant gain mismatch between the two signal paths, the bits G0 or G2 can be used depending upon whether it is required to decrease or increase the gain of the high-frequency path.

The ac analysis was performed on the ROI to plot the output gain by providing a fixed input voltage. Monte Carlo simulation was performed to test the circuit performance across temperature and process corners. The achieved gain is ∼49 dB, as shown in Fig. 8. The standard deviation of the gain is 91.95 mdB. The resistors and the transistors all have an inherent temperature coefficient. The circuit design utilizes a proportional to absolute temperature (PTAT) and complimentary to absolute temperature (CTAT) combination of resistors in closed-loop amplifier configurations across the chain to maintain the gain constant. The consecutive positive and negative temperature coefficients cancel out each other's effect, keeping the gain variations minimum throughout the range. The ROI is designed with multiple Hall-effect sensors in mind. Hence, the gain is initially kept constant over temperature to demonstrate the frequency capability of the readout circuit, as shown in Fig. 8. Since each sensor material will have different temperature-dependent sensitivities, the PTAT and CTAT closed-loop resistors used for minimizing the change in gain over temperature would be modified to nullify the temperature effect of the particular sensor, once that dependence is measured or known.

V. Measurement Results

The chip micrograph of the ASIC is shown in Fig. 9. The highlighted portion of the chip represents the area of the ROI. The dimensions are approximately 2850 by 200 μm.

A. ROI Testing

The ROI is tested by providing a square wave input of 1 kHz. A supply voltage of 3.3 V and VCM of 1.65 V is used. CLK and $\overline{\text{CLK}}$ are provided a complimentary clock signal of 250 kHz. Three outputs are observed: the low-frequency signal (VLF), high-frequency signal (VHF), and final summed output (VOUT). The measured oscilloscope results are shown in Fig. 10. The results are normalized to the ground. The low-frequency path output is a square signal but with a slow rising edge, while the high-frequency path output spikes at the edge, giving a much shorter rise time. The final output is then a fast-rising square wave. It is the amplified version of the input

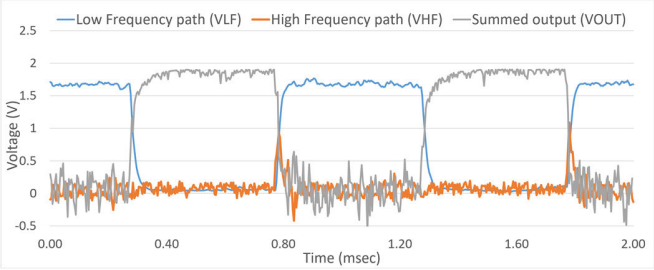

Fig. 10. Output waveforms of the readout interface standalone testing.

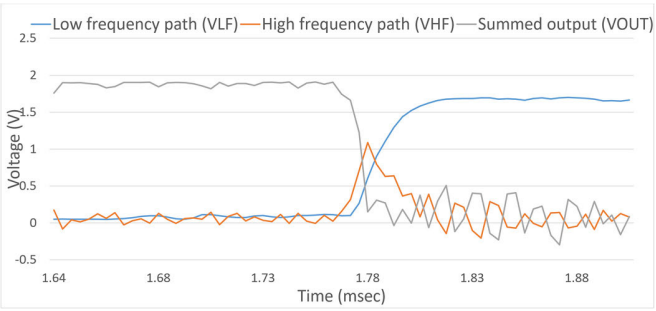

Fig. 11. Output waveforms of the ROI zoomed-in to show pulse edge.

with a fast response. The noise in the signal is random noise from the environment since the amplifiers are high bandwidth, and there is no low-pass filtering in the high-frequency path to limit bandwidth.

To see the performance of both the paths and final output, one of the edges is zoomed in Fig. 11. Here, it can be seen that VHF rises quickly with a sharp pulse and then decays slowly. VLF, on the other hand, has a longer rise time. The fall time of VHF and the rise time of VLF were set the same by keeping the 3-dB frequencies of both filters equal to the crossover frequency. This rise time of VLF and the fall time for VHF are $\sim$30 μs. The final summed output VOUT, in turn, shows the addition of the two signals, providing a fast response to the input pulse. The two signals, VLF and VHF, are inverted as compared to the input, which leads to the final output being in-phase with the input signal.

B. ROI Testing With Hall-Effect Sensor

ROI testing verified the performance of the circuit. This ROI is designed with multiple Hall-effect sensors in mind, and hence, it can be used for testing with any four terminal Hall-effect device. Preferably, a high bandwidth sensor should be chosen to highlight the high bandwidth capability of this ROI. The sensors used for these tests were AlGaAs/GaAs Hall-effect sensors [29]. The test setup is shown in Fig. 12.

Fig. 13 shows the printed circuit board (PCB) used for testing with the ASIC ROI and the sensor. The Hall-effect sensors are wire-bonded on the PCB with the ROI. These are two sensors fabricated on the same die next to each other. They are connected to the ROI, as shown in Figs. 2 and 3. One sensor is connected to the current spinning of the low-frequency path, while the second sensor is connected to the high-frequency path. The second sensor does not need any current spinning since it is going to the high-frequency

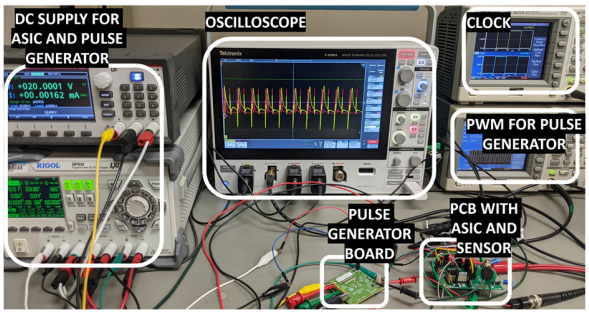

Fig. 12. Test setup for the current sensing system.

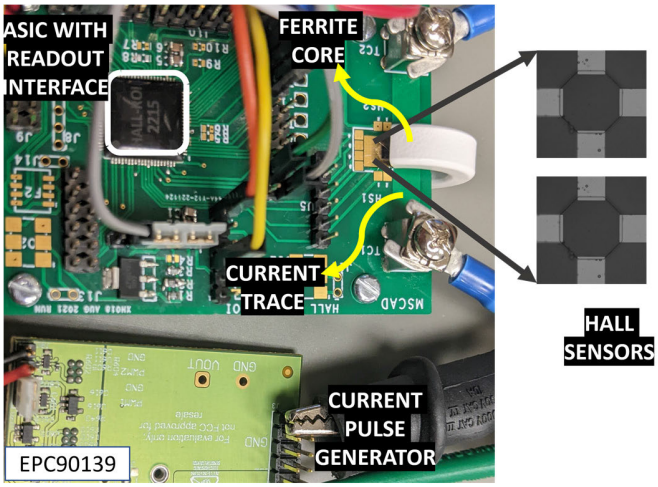

Fig. 13. PCB for the test setup with the ROI and the Hall-effect sensor.

path, and this path does not process any dc signal (current spinning is only required for low-frequency dc signals). Hence, its two alternating terminals (P1 and P3) are connected to the current bias, while the other two terminals (P2 and P4) are used for input to the ROI. A current trace is fabricated next to the sensors at a distance of 1.5 mm. A current pulse generator is used to drive the current trace on the PCB and provide high-current pulses for testing. A magnetic field concentrator is also used in this testing. It is a gapped ferrite core placed in such a way that the current trace passes from its middle, and the sensors sit inside the gap. It helps concentrate the magnetic field onto the sensors and improve sensitivity. The most common material used is ferrite, which has high permeability and low losses as needed for these magnetic field concentrators. Although the magnetic field concentrator is not a necessary part of the system and the system can be implemented without it, it helps increase sensitivity by focusing the field and reducing the noise captured by the sensor.

The Hall-effect sensors are biased with a current of 300 μA. The testing conditions of the ROI are set up in the same manner as explained in Section V-A. The current pulse generator produces short pulses of high current for the sensor to detect. This generates a step response of the combined setup of the sensor and the interface circuit. The normalized testing results are shown in Fig. 14. The current waveform peaks at $\sim$17 A and then decays slightly for the pulse duration. The low-frequency path signal slowly rises and then follows the current

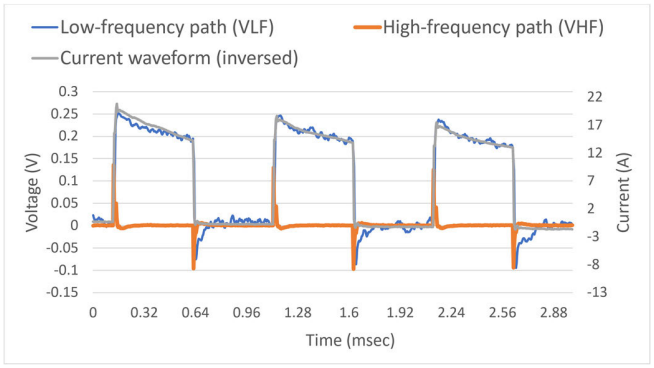

Fig. 14. Measurement waveforms from the Hall-effect sensor and the ROI.

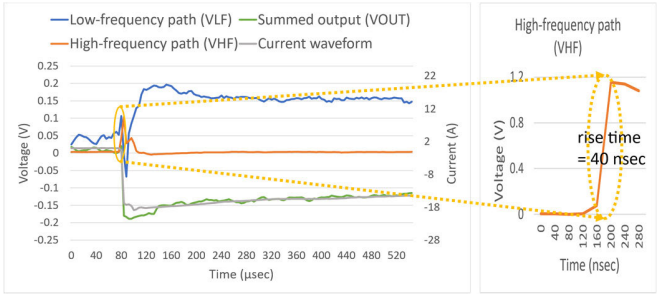

Fig. 15. Measurement from the sensing system to observe response times.

pulses. The high-frequency path signal gives a sharp peak during the rising edge of the current pulse, which speeds up the overall response of the system. As mentioned in Section IV, the high-frequency signal path is lower in amplitude and will be added with a higher gain using the weighted summing amplifier. From this figure, the sensitivity of the sensor can be calculated as 230 mV/18 A = 12.7 mV/A.

The output signals of the sensing system in Fig. 14 include slight noise peaks at each current pulse edge. This is due to electromagnetic coupling between the sensing system and the current pulse generator. These noise peaks can be eliminated by using isolation in the sensor packaging. To calculate the residual offset, the sensor is connected to the ROI, but no magnetic field is generated by not providing any current pulses on the current trace. The change in the dc value of the low-frequency output of the ROI is noted. The input-referred residual offset is 1.525 mV. This offset is from the sensor due to using a two-way current spinning technique. This can be minimized further by using a four-way or eight-way spinning technique. For this work, the ROI was tested with multiple sensor samples, and a 1.5 mV average offset was measured.

The normalized response of the sensor with the ROI to a single pulse is shown in Fig. 15. VLF and VHF are inverted with respect to the current pulse. The final summed output (VOUT) is the fast response to the current flowing through the current trace and is in phase with it. It is the combination of VLF, which follows the current pulse but with a longer rise time, and VHF, which has a sharp rising edge and hence makes the final output faster. From this figure, it can be seen that the low- and high-frequency paths, respectively, have a rise and fall time of ~30 μs. Having similar response times

TABLE I
COMPARISON WITH STATE OF THE ART

	[15] 2012	[8] 2018	[12] 2015	[20] 2014	[21] 2019	**This work**
Process	0.35 μm	0.8 μm	0.8 μm	0.18 μm	0.35 μm	0.18 μm
Bandwidth	**10 kHz**	**30 kHz**	**30 kHz**	**>100 kHz**	**1.7 MHz**	**25 MHz**
Sensitivity	-	16 mV/mT	-	-	-	12.7 mV/A 95.25 mV/mT*
Temperature range	–40 to 150°C	-	-	-	-40 to 150°C	–40 to 175°C
Residual Offset	>3 μV >30 mT	5 mV 0.3 mT	0.2 mT	25 μT	85 μT	1.5 mV 15.75 μT**

* To convert from mV/A to mV/mT, the formula for magnetic field created by current in a straight wire is used [$B = \frac{\mu_0 I}{2\pi R}$ where B = strength of magnetic field, μ_o = permeability of free space, I = current flowing in the wire, and R = distance from the wire].
** To convert from T to mV, the reported sensitivity is used.

is due to having the same filter frequencies in their design (as discussed previously). This ensures proper signal addition, resulting in VOUT. From Fig. 15, the rise time of the high-frequency signal can be noted as 40 ns. This rise time dictates the bandwidth of the current sensing system and how fast it can respond.

There are two methods for bandwidth calculation from rise time. One method utilized in filters is to use an approximation to calculate bandwidth, given as 0.35/rise time [31]. Another method is to invert the rise time of the step response to get the bandwidth [21], [32]. For accurate comparison with state of the art, the second method is used. The calculated bandwidth for this work is 25 MHz.

VI. COMPARISON WITH STATE OF THE ART

A comparison of the design with the state of the art is shown in Table I. The relevant work using only Hall-effect sensors is included in the table. The focus of this work was to improve the bandwidth of the ROI and hence the overall current sensing system. As seen from the table, this work achieves the highest frequency compared to other Hall-effect sensor-based designs.

VII. CONCLUSION

The proposed current sensing system makes use of Hall-effect sensors and an ROI ASIC. A high-bandwidth ROI is designed for Hall-effect sensors that removes the offset and amplifies the signal without limiting bandwidth. AlGaAs/GaAs Hall-effect sensors are used for this testing; however, this ASIC can be used for any four terminal Hall-effect sensors. This system utilizes only Hall-effect sensors, which makes miniaturization much easier as compared to other devices. This is a noninvasive magnetic field detection system. It has a high bandwidth, providing a fast response to a current pulse, and hence can be used in power electronics applications, including control and overshoot safety systems.

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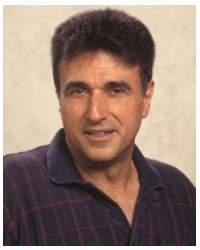

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