Use of E-Beam Lithography to Optimize Lithography Patterning on SiC Wafers

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***Abstract*-Silicon carbide (SiC) is a wide bandgap semiconductor material used to manufacture high-voltage and high-temperature operating devices. As SiC technology continues to advance, the density of devices across a wafer increases as transistors become smaller. On commonly used 6-inch SiC wafers, the wafers are subject to wafer bowing due to the physical hardness of'the material. Optical-based lithography faces several critical challenges when applied to the fabrication of SiC and other wide bandgap semiconductors, particularly in advanced device architectures like FinFETs and T-gate structures. A major limitation is the shallow depth of focus inherent in optical lithography systems. Because SiC devices often involve non-planar topographies-due to deep etching, thick epitaxial layers, or trench structill"es--the limited depth of focus can lead to pattern defocusing and critical dimension (CD) variation across uneven surfaces. This is especially problematic when trying to define narrow fins or ultra-short gate lengths, where nanometer-level precision is essential for device performance and yield. Further, implementing conventional photolithography can lead to resolution inconsistencies across the wafer and significantly reduce yield. Cross-wafer yield is a challenge that can be addressed with e-beam lithography (EBL). E-beam direct-write lithography demonstrates superior fidelity of nanoscale features due to its great depth of focus over challenging topography on 6-inch and greater diameter SiC wafers. All the while, the specific multicolumn e-beam lithography (MEBL) system implemented herein overcomes throughput challenges historically hampering EBL, making it a production-worthy lithography system for compound semiconductors.**

illdex **Terms-Compound semiconductors, depth of' focus, e-beam lithography, photolithography, silicon carbide.**

I. INTRODUCTION

SILICON carbide (SiC) is a semiconductor material commonly used to manufacture high-voltage and high-temperature devices. Compared to conventional silicon-based devices, SiC devices enable higher switching speeds, higher breakdown voltage, and higher temperature operation reliability, leading to smaller, faster, more efficient power devices. One major issue from SiC processing relates to transitioning from processing 4-inch wafers to 6-inch wafers. Due to the hardness of the material, SiC needs higher temperatures and more energy in crystal growth and processing. In addition, defects across the wafer are complex to inspect due to SiC's transparency and high refractive index. Due to the increased difficulty of producing 6-inch wafers, the wafers are subject to wafer bowing, leading to an uneven surface. An uneven surface directly affects the uniformity of films deposited on the wafer, leading to challenges for photolithography, which bas a limited Depth-of-Focus (DoF).

As the critical dimensions of electronics shrink, issues regarding accurate patterning become more prevalent. Technological improvements to lithographic patterning technology are essential to continued scaling in the semiconductor industry [l]. With wafers not completely flat, the photoresist on top of the wafer conforms with the warping and bowing of the wafer. This can lead to surface variations exceeding the DoF of optical lithography, leading to varied resolutions throughout the wafer. With varied resolutions across the wafer, the minimwn device dimensions are limited, affecting the scalability of the devices.

Handling topography has proven very challenging, especially for optical lithography. Methods such as Optical Proximity Correction (OPC) struggle to handle complex wafer landscapes, usually leading to erosion and dishing.

Other common processes utilized to remedy the DoF constraints of optical-based lithography such as implementing Stress Compensation Layers (SLC's), or Laser Annealing can impact material integrity and device performance. The most common solution is Chemical Mechanical Polishing (CMP) as it has been proven to solve some of the issues found in wafer topography. However, CMP isn't a flawless solution and results in a more expensive and time-consuming manufacturing process.

Another potential issue stems from alignment control of photolitbography, which is exacerbated by wafer warpage. Misalignment issues are magnified with smaller pitch distances. Improper alignment can lead to significantly increased gate-source and gate-drain overlap capacitances in MOSFET devices or cause electric field crowding, leading to device degradation. One example of such misalignment is seen in Fig. 1. If the misalignment is large enough, tunneling can occur depending on the regions aligned, and the device could degrade further. It is important to observe the effects of resolution, depth of focus, and film uniformity to ensure

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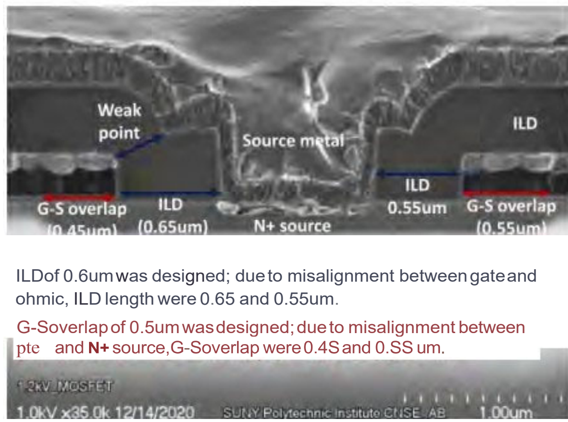

Fig. I. Misalignment error seen in Source contact alignment, leading to increased weak point faults [2].

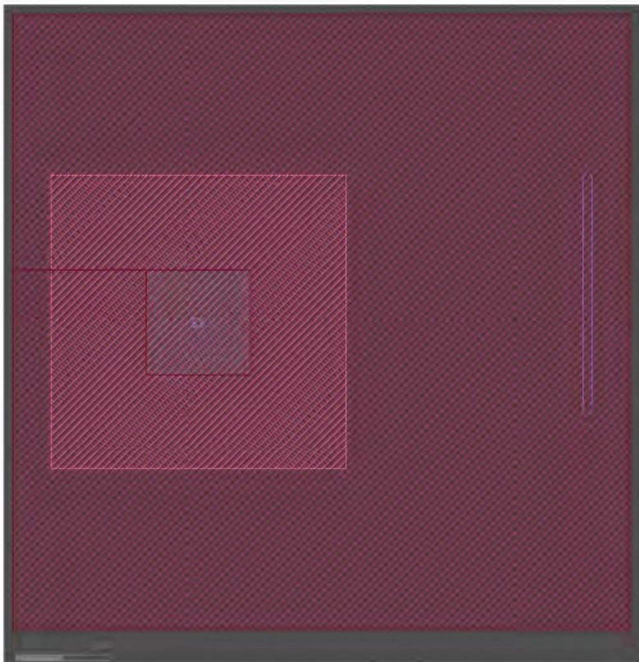

Fig. 2. Example module layout designed for stepper testing.

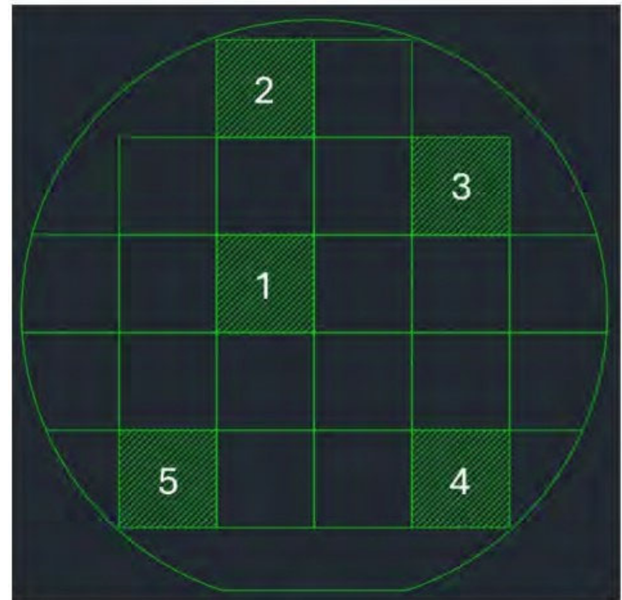

Fig. 3. Example module layout designed for stepper testing.

minimal processing defects that affect device performance. Direct e-beam writing can improve pattern alignment on warped wafers, and can improve the resolution and precision of critical features, including source contact alignment and gate contact opening, leading to improved device performance and reliability.

II. Stepper Experimental Setup

For testing involving the stepper, the Nikon 2005i8A -a precision machine designed for the photolithography process - was used to pattern 150mm Si wafers. It uses a focused cooled argon-ion laser source and a high-definition digital imaging system to accurately reproduce patterns on the wafer. A reticle with features varying from 0.2µ,m to 20µ,m was designed and tested. The reticle has double pellicles on both sides to prevent debris from affecting feature resolution. Limitations on optical photolithography can be noticed through the stepper and resolutions across the whole wafer [3]. The varying CD and pitches on the reticle enable easy observance of differences in resolution across the wafer.

With the stepper, the positive photoresist GIR 2700 was exposed and developed. The photoresist is deposited on the substrate with an approximate thickness of 1.3µ,m. The photoresist is then soft baked at 90°C for 60 seconds. Exposure is then completed with the i-line wavelength Nikon stepper. A post exposure bake was completed at 115°C for 60 seconds. Development is then completed using a 0.262N TMAH compatible developer with surfactant. The wafers are submerged in the developer for 60 seconds and puddle developed.

Once development is completed, the sample processed through the stepper is analyzed with IVS series equipment. The IVS provides an optical view of the developed features and critical dimension (CD) metrology. The sample is examined across the full wafer to observe variations in the CD resolution.

III. Stepper Results

The IVS was used to determine CD of features developed by the stepper. Areas were tested across the wafer to evaluate the correlation between wafer pattern location and CD values. Figure 3 below showcases various sections of the wafer used for testing.

Within each area, a standard feature of 4um was developed and tested using the recipe previously mentioned. Each feature was developed and measured with the IVS system. The Table below showcases the CV values of the top and bottom of developed features. The sidewall angle is extracted using the CD values of the developed feature's top and bottom and the photoresist's estimated thickness. Modules in each area, as depicted in Figure 3, were measured and plotted for comparison.

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TABLE I
EXTRACTED CD AND SIDEWALL ANGLES

	Field 1	Field 2	Field 3	Field4	Field 5
CD Top	3.91	4.17	4.24	4.31	4.46
CD Bottom	1.93	2.07	1.93	2.15	2.08
Extracted Angle	52.6	51.1	50.7	50.2	47.7

From Table I, it can be seen that the feature resolution and sidewall angle vary across the whole wafer. The wafer bowing and potential inconsistent exposure leads to varying feature resolution across the wafer. For larger-scale production, the nonuniformity of the resolution will greatly affect the overall yield. In addition, with smaller features, the resolution will continue to worsen. With gradually smaller and smaller features, stepper alternatives may need to be considered for resolution improvement.

IV. E-BEAM DEMONSTRATION AND RESULTS

Optical steppers have been optimized over many years to be highly productive; however, they are fundamentally limited by the diffraction of light. To achieve the highest in-plane patterning resolution an optical system must operate at a high numerical aperture, leading to very narrow depth-of-focus. This is typically generalized by the following two equations in terms of the wavelength ()..) and numerical aperture **(NA)** of the optical system as described by

$$\text{resolution} = k1 \frac{\lambda}{NA}$$

$$DoF = \pm k2 \frac{\lambda}{(NA)^2}$$

where kl and k2 are related to the mask pattern and illumination.

As technology bas progressed, wavelengths have become smaller and numerical apertures larger to support resolution requirements for semiconductor industry scaling. However, these advancements in resolution have come with the tradeoff of reduced depth-of focus. In response to this, the industry bas adopted tight controls for silicon wafer flatness in response. For advanced nodes, improvements in silicon wafer planarization have decreased the exposure requirements such that a depth-of-focus of 100 nm is considered sufficiently high. However, this narrow depth-of-focus is insufficient for SiC wafers.

Nikon steppers are optimized for planar silicon wafers and struggle with the reflectivity, surface roughness, and topographic complexity of wide bandgap materials like SiC. The stepper's limited focus window can result in poor pattern fidelity, reducing the viability of optical lithography for next-generation wide bandgap device structures. These limitations highlight the need for alternative patterning techniques, such as electron beam lithography, which offer greater flexibility and precision for complex SiC device fabrication.

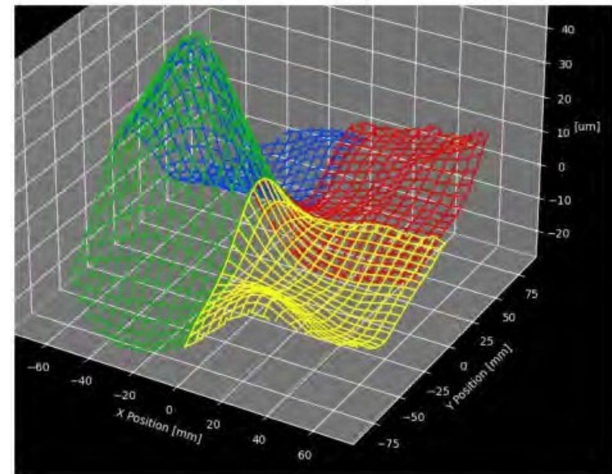

Fig. 4. Multibeam e-beam direct-write lithography wafer height map revealing $45\mu m$ in variation across a wafer.

To address the challenge of resolution variation caused by warpage and bowing of SiC wafers, the Multibeam direct-write multicolumn e-beam lithography technology (MEBL) was used to fabricate sub-micron lines on warped wafers. Since Multibeam MEBL uses electrons, it possesses several performance advantages over photolithography. In particular, the resolution can be maintained given its large depth-of-focus, on the order of 10 microns or more with a <lOOnm resolution.

First, the Multibeam system employed wafer height mapping to measure topology variation across the wafer. Fig. 4 shows peak-to-valley wafer warpage of 45JLID (45,000 nm) across 150mm wafer surface.

Next, the Multibeam system was leveraged to pattern 200nm lines across a warped wafer to assess impact to resolution. The system adjusts the focus of each e-beam based on the wafer height map (e.g., Fig. 4) to track the wafer surface, maintaining consistent resolution and CD control during wafer patterning. This enables the system to pattern fine features at very high resolutions over highly non-planar surfaces.

Figures 5 and 6 demonstrate Multibeam's capability to pattern consistent lines across the wafer, regardless of wafer warpage. In this example, Multibeam patterned a wafer coated with 100nm of **PMMA.** Thee-beam exposure energy was 6.5 keV. After patterning, the wafer was developed and imaged under a Scanning Electron Microscope (SEM) to measure critical dimension uniformity (CDU) and line-edge roughness (LER). The patterning results met requirements for both CDU (< 10% 3cr) and LER (< 10% 3cr).

The Multibeam system has an intrinsic DoF of ±lOJLm. This enables the system to pattern across steps, or height discontinuities, in addition to warped wafers, without loss of dimensional fidelity. In Fig. 6, the Multibeam system was used to pattern a wafer with 5µ,m steps. The wafer was spin-coated with PMMA, which resulted in inconsistent PMMA thickness across the highly topographic wafer. The e-beam exposure energy was 6.5 keV. After patterning, the wafer was developed and imaged under an SEM. Note that the PMMA was thicker at the bottom of the step, thinner at the top of the step, and non-existing at the upper corner of the

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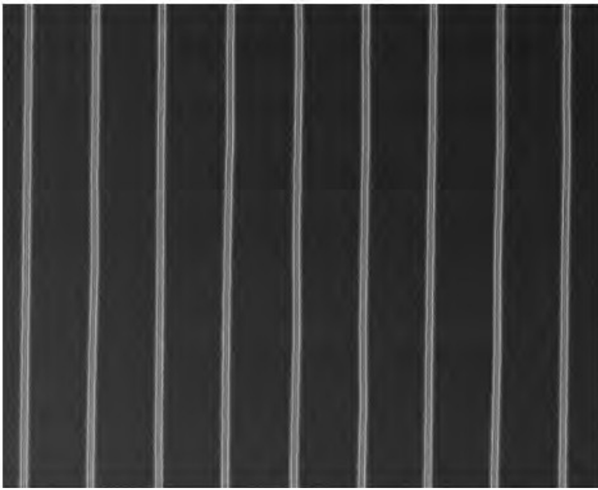

Fig. 5. Multibeam e-beam direct-write results demonstrating consistent high-resolution 200 nm lines. Line width ranges from 195 to 201 nm; LER is 6.7nm.

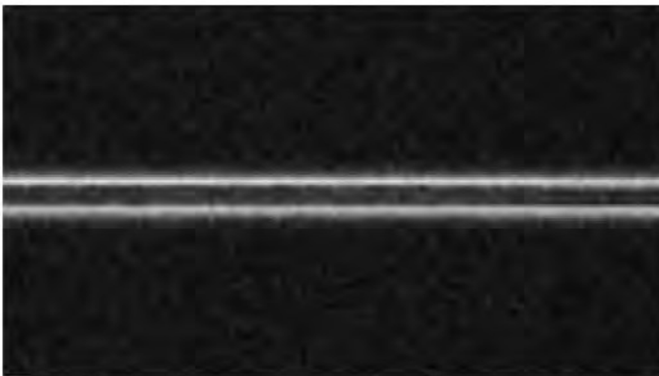

Fig. 6. Multibeam e-beam direct-write result: Line width is 200nm, LER is 4.4nm.

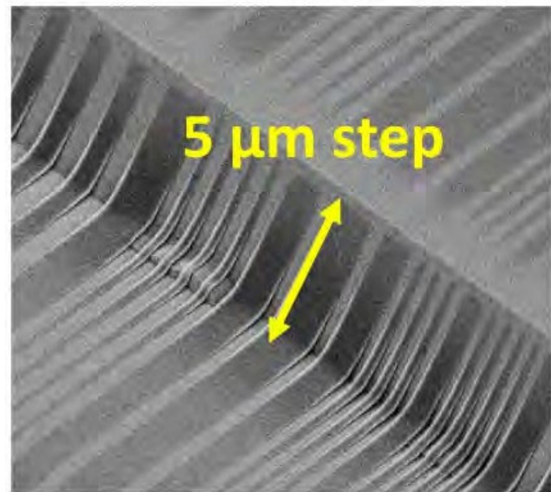

Fig. 7. Multibeam writing results: submicron lines over topography larger than I micron. Where photolithography suffers from the diffraction-limited tradeoff between resolution and depth-of-focus, e-beam lithography exhibits high resolution with little sensitivity to topographic features.

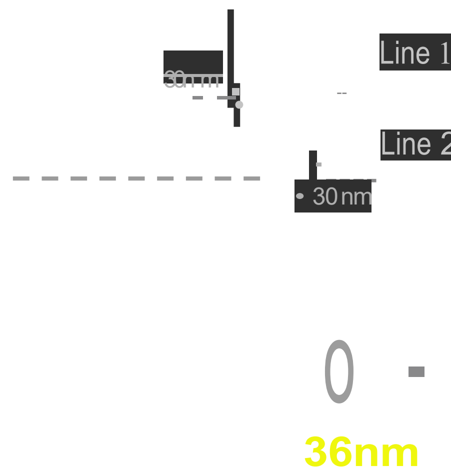

Fig. 8. Example process results: Despite their compact size, miniature e-beam columns can achieve exceptional resolution, as demonstrated above. (left) 30nm lines with rms LER <10% and (right) vias down to 36nm.

step. This inconsistent **PMMA** thickness is due to the spin-coat process used before patterning. Despite the variation in PMMA thickness, Multibeam successfully patterned the wafer and demonstrated excellent CD control across the step. The line-widths at the top of the *5μ,m* step are the same as the line-widths at the bottom of the step. This demonstrates that the entire step range is within the system's depth-of-focus.

V. CONCLUSION

Today's challenges in fabricating SiC devices include limitations in optical lithography resolution for 150mm & 200mm wafers as well as wafer warpage which results in poor alignment and lack of fidelity of resolution and linewidths over high topography. These challenges have resulted in an overall complex and costly manufacturing process for today's power devices that are fueling high-growth applications like powertrain converters, wireless communications, satellites and RADARs, and defense. Wide bandgap semiconductors - particularly SiC and GaN - offer several advantages over silicon-based devices given their ability to operate at higher voltages, temperatures, and frequencies. However, these advantages cannot be fully realized without addressing the complexities that also come into play in the fabrication process. Implementing multicolumn e-beam direct-write lithography overcomes the aforementionedchallenges, as shown in Figures 4-7. It can accurately pattern over complex surface topographies, which is particularly valuable for wide bandgap materials that often require etching and deposition steps resulting in non-planar surfaces. Further, Multibeam's resolution capabilities can be extended even further down on the nanometer scale, as shown in Figure 8, and is capable of extending even further beyond this.

Beyond its ability to remedy the topographic challenges, **MEBL** has innate advantages in enabling rapid exploration of advanced device architectures. For advanced power device structures like vertical SiC power MOSFETs, which are increasingly exploring FinFET-like geometries to

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improve channel control and performance, e-beam lithography's precision and topographic adaptability make it a strong candidate for defining narrow fins with high dimensional control. Similarly, the ability of e-beam to produce extremely fine features with high resolution is advantageous in fabricating shorter T-gates in high-electron-mobility transistors (HEMTs) or MESFETs. These shorter gates can improve switching speed and reduce parasitic capacitances-critical factors in high-frequency and high-power applications where wide bandgap materials excel.

Vertical SiC power MOSFETs exploring FinFET-like designs require patterning over vertical or semi-vertical sidewalls. Optical lithography struggles to maintain resolution and alignment in these conditions, leading to rounding or distortion of features. Similarly, forming short T-gates in lateral high-frequency devices becomes difficult due to diffraction limits and limited resolution, making it bard to reliably fabricate sub-100 nm gates on rough or high-aspect-ratio surfaces.

Direct write e-beam lithography enables precision fabrication of new, high-resolution, small-line SiC devices, including 3D devices, opening up greater design flexibility for wide bandgap devices. It enables patterning capabilities that go beyond the limits of traditional optical lithography, making it a powerful tool for pushing the boundaries of SiC and other wide bandgap semiconductor device performance. Multibeam has taken these advantages to the next level by coupling the unique patterning capabilities of e-beam with an overall significantly improved full-system architecture that delivers an order of magnitude more productivity than that of a traditional single e-beam system. Wbat does this mean for the industry? Rapid development, prototyping, and production of next-generation device designs.

ACRONYMS

CD: Critical Dimension
CDU: Critical Dimension Uniformity
DoF: Depth of Focus
LER: Line-Edge Roughness
MOSFET: Metal Oxide Semiconductor Field Effect Transistor
NA: Numerical Aperture
SEM: Scanning Electron Microscope
Si: Silicon
SiC: Silicon Carbide
TMAH: Tetramethylarnrnonium Hydroxide
EBL: Electron Beam Lithography

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