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Characterization of Silicon Carbide Low-Voltage n/p-Channel MOSFETs at High Temperatures

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ABSTRACT SiC-based n-channel and p-channel MOSFETs fabricated by Fraunhofer IISB SiC CMOS technology are characterized from room temperature up to 300°C. The behaviors of these low voltage devices including the short-channel effect (SCE), p-type ohmic contact with high resistivity, and the low channel mobility due to the SiC/SiO_2 interface are presented. A thorough analysis is performed to understand the cause of low channel mobility, with TCAD simulations specifically on p-channel MOSFET, providing an insight into the impact of channel length, interface traps, and contact resistivity on device performance. The analysis in this paper is important in the comprehension of the low-voltage SiC MOSFETs so as to achieve balanced n-channel and p-channel MOSFETs and lead to the monolithic integration of SiC ICs with SiC power devices.

INDEX TERMS Silicon carbide, CMOS, high temperature, TCAD, channel mobility, SiC/SiO_2 interface.

I. INTRODUCTION

Silicon carbide (SiC) is a candidate material of great interests due to its wide bandgap and ability to grow the native oxide as silicon (Si) [1], [2]. SiC offers several advantages over Si, including high breakdown electric field, high saturation velocity, etc., which are particularly beneficial for applications of high-voltage, fast-switching, low-loss, etc. [3]. Its extremely low intrinsic carrier concentration of SiC as shown in Fig. 1 enables high-temperature operation of SiC devices [4], [5]. Since 1995, SiC-based electronics for high-temperature applications have received extensive attention [6]. As the market of SiC power electronics grow rapidly, the end system using Si-based devices or chips are often constrained by parasitic effects [7]. Si ICs are also inadequate for applications in sectors like aircraft, automotive and aerospace systems where operating temperatures exceed 200°C [8], [9], [10]. Consequently, there is a strong desire to develop a SiC CMOS technology to fully integrate essential functions - such as gate driving, sensing, amplifying, and controlling - with SiC-based power electronics to minimize losses, reduce size and cost, and enable operation in harsher environments [11]. Despite these needs, the monolithic integration of the control circuity in SiC or other wide bandgap materials has proven challenging. Among wide bandgap materials, although both SiC and gallium nitride (GaN) have long been proposed for high-temperature applications, SiC is the only material where complementary MOSFET process is not merely a tantalizing possibility, but already an established process platform with some digital circuit demonstrations and extreme-condition reliability studies [12]. Technological advances in SiC, including interconnect metallization and device packaging [13], have enabled SiC ICs to operate at temperatures beyond 450°C. While the development of SiC ICs traces to early 90s led by Cree [14] and Purdue [15], we still lack matured SiC CMOS processes, and the accessible in-house SiC CMOS fabrication processes are scarce.

Among the reported SiC CMOS processes, Raytheon U.K. has set the benchmark for SiC CMOS technology with its 1.2-μm HiTSiC process, achieving a high manufacturing readiness level and enabling the monolithic integration of n-channel and p-channel MOSFETs (nMOS/pMOS) with the capability to operate at 300°C and above [11], [13]. However, it lacks the evaluation of the SiC/SiO_2 interface traps which has always been a major reliability concern for SiC MOSFETs. Ekström from KTH demonstrates a

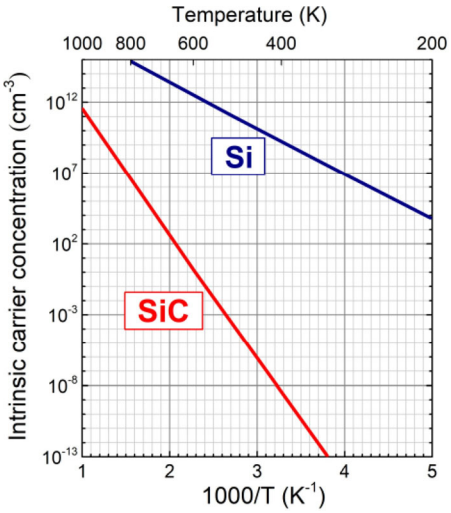

FIGURE 1. Temperature dependence of the intrinsic carrier concentration for SiC and Si [4].

TABLE 1. Properties of 4H-SiC as compared to Si.

Parameters	Si	4H-SiC
E_G(eV)@300K	1.12	3.26
E_C (MV/cm)	0.3	2.5-3
μ_n ($cm^2/V{\cdot}s$) *1	1350	1020
μ_n ($cm^2/V{\cdot}s$) *2		1150
μ_p($cm^2/V{\cdot}s$)	450	120
$\mu_{fe,n}$ ($cm^2/V{\cdot}s$)	500	*3 15-35
$\mu_{fe,p}$ ($cm^2/V{\cdot}s$)	100	*3 7-10
σ_{therm} (W/m·K)	150	490

*1 perpendicular to c-axis, *2 parallel to c-axis.
*3 values represent the results of conventional oxidation followed by nitrogen annealing.

preliminary SiC CMOS process with devices such as MOSFETs, capacitors as well as ICs, inverters and ring oscillators that operate at 200°C [16]. Recessed channel MOSFETs without using ion implantation are designed for the demonstration. The main benefit of recessed channel design is the immunity to short-channel effect (SCE). Nevertheless, the benefit is not manifested since the designed devices have long channel length. Since 2017, Hitachi has focused on developing radiation-hardened SiC technology for nuclear plant applications, particularly after the Fukushima disaster, and has demonstrated some SiC devices and ICs [17], [18]. The n-channel and p-channel MOSFETs have unsatisfactory mobilities with unbalanced threshold voltages. MOSFETs are fundamental to modern microelectronics due to advantages such as high input impedance, simple gate-driven operation, low static power consumption due to the complementary pair structure, and high device density [19], [20]. They hold substantial promise for the next generation of high-temperature, high-frequency and high-voltage applications [19]. Yet, the performance of SiC MOSFETs is hampered by the low channel mobility largely due to the high interface traps [20], [21], [22]. TABLE 1 gives a comparison of the material with the parameters which

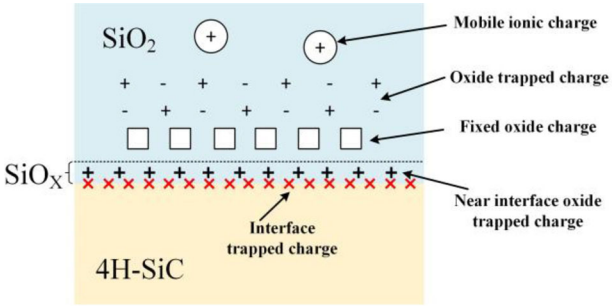

FIGURE 2. Allocation of five types of charges associated with SiC-SiO_2 interface system [24].

are important in MOSFET device design and evaluation. Currently, typical 4H-SiC n-channel MOSFET inversion channel mobility is 15 – 35 $cm^2/V.s$, while p-channel is 7 – 10 $cm^2/V.s$ with nitridation-treated oxides [20], [23], which is far from the channel mobility of Si counterparts. It is noted however that the mobility of pMOS is lower than nMOS by a factor of 2 – 3, which presents a unique balance level compared to Si. The low channel mobility of SiC device is primarily caused by the structural imperfection of the dielectric and the interface defects. The exact causes of trap formation have not been fully understood, but the presence of electrically active traps in the oxide and at the interface have impacts on the device's electrical properties. As shown in Fig. 2, there are mainly five types of charges associated with the SiC-SiO_2 system in general: mobile ionic charges, oxide trapped charges, fixed oxide charges, near interface oxide trapped charges (NIOT) and interface trapped charges [24]. The interface trapped charges are mainly responsible for limiting the channel mobility, while the fixed oxide charges and oxide trapped charges, NIOTs are responsible for the instability of the threshold voltage [25].

Recently, Fraunhofer IISB in Erlangen, Germany, developed a promising SiC CMOS technology, reporting an inverter using the pMOS [26] operating with a 5 V power supply over the temperature range of 25°C to 400°C and op-amp with both nMOS and pMOS [27] measured up to 300°C. Although SiC low-voltage CMOS devices have been developed, their performance across varying temperatures remains under-explored, especially the pMOS. Furthermore, the threshold voltage shift, contact resistance, especially the channel mobility at high temperature needs to be analyzed to serve a purpose to optimize the process.

In this paper, we present the characterizations of 4H-SiC MOSFETs fabricated with the optimized Fraunhofer SiC CMOS process. Both n-channel and p-channel MOSFETs with various channel lengths are evaluated regarding the short-channel effect (SCE), while the scattering effects on channel mobility at high temperature are analyzed. Technology computer-aided design (TCAD) simulations with consideration of effects of numerous physical mechanisms have been conducted with the p-channel MOSFET structure, which gives insights into the device operation.

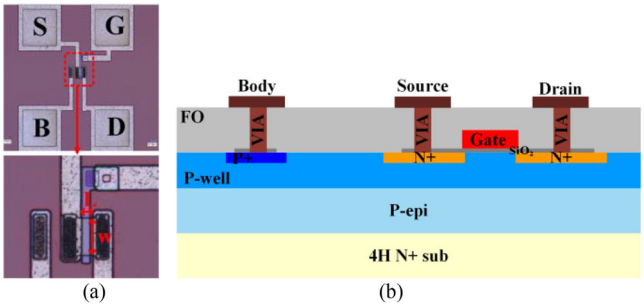

FIGURE 3. (a) Top view of a SiC nMOS layout. (b) Technology cross section of SiC CMOS process for nMOS structure.

II. EXPERIMENT RESULTS

The structures were fabricated using an optimized SiC CMOS process in collaboration with Fraunhofer IISB. This process has a minimum linewidth of 1 μm with twin wells, a single poly, and a single metal layer (1P1M). The devices are formed in a lightly doped P-epi layer (i.e., 1e15 cm^{-3}) on top of a 4H-SiC N_+ substrate. A series of aluminum (Al) implants are used for the P-well and P_+ regions while nitrogen (N) implants are applied for N-well and N_+ regions. No channel counter doping was employed in this process. A 50 nm gate oxide was grown by dry oxidation at 1300°C and followed by annealing in NO atmosphere at the same temperature. The dielectric layer and doping profiles are designed to allow 20 V operation at temperature beyond 300°C. P-type gate polysilicon is used for both nMOS and pMOS to help balance the threshold voltage [28]. TABLE 2 lists the parameters of the fabricated devices including the gate oxide thickness, the doping concentrations and junction depth which were extracted from the secondary ion mass spectrometry (SIMS) analysis. It is noteworthy that the ionization energy of Al is significantly higher than that of N; consequently, the electrical activation of Al could be substantially lower than its doping concentration unlike N [29]. This incomplete ionization of dopants is an essential factor to consider in device simulation to ensure accuracy in predicting electrical behavior.

A. N/P-CHANNEL MOSFETS AT ROOM TEMPERATURE

Fig. 3 shows the nMOS structure used for the characterization with varying channel width *(W)* and channel length *(L)*. I_D–V_G, I_D–V_D, and transconductance g_m of both nMOS and pMOS were obtained at room temperature.

I_D–V_G of n-channel MOSFETs were measured by sweeping V_G from 0 to 20 V at drain bias V_D = 0.5 V, while V_G from 0 to –20 V at drain bias V_D = –0.5 V was applied for p-channel MOSFETs. The curves with varying L are given in Fig. 4(a) and (c), respectively. The threshold voltage V_{TH} is extracted by the constant current method (CCM) [30] at predefined $I_D = W/L \times 10^{-1}$ A. V_{TH} extraction results in Fig. 4(b) and (d) indicate the(SCE occurs with L less than 2 μm for both nMOS and pMOS. It can be seen in Fig. 4(b) that V_{TH} for the long-channel nMOS is about 5.0V while

TABLE 2. Device parameters.

Parameters	Value
t_{ox}	50 (nm)
x_j	0.3 (μm)
N+ doping concentration	5e19 (cm^{-3})
P+ doping concentration	3e19 (cm^{-3})
N-well doping concentration	2e16 (cm^{-3})
P-well doping concentration	1e17 (cm^{-3})

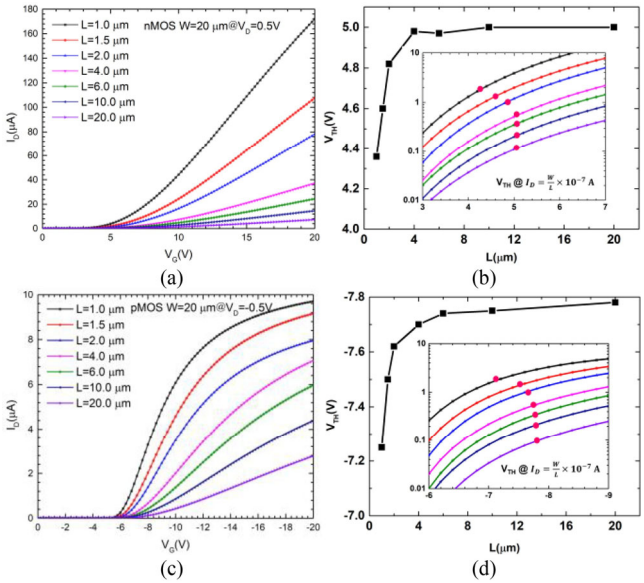

FIGURE 4. (a) I_D–V_G of n-channel MOSFETs with varying L (W = 20 μm). (b) V_{TH} extraction of n-channel MOSFETs. (c) I_D–$V_G$of p-channel MOSFETs with varying L (W = 20 μm). (d) V_{TH} extraction of p-channel MOSFETs. * *Sign of* I_D of pMOS is transferred to be positive for the convenience of data process especially for the log-scale plot.

for short-channel device with L = 1 μm, V_{TH} = 4.35 V. Fig. 4(d) shows $V_{TH} \approx$–7.7 V and –7.25 V for the long-channel and 1 um short-channel pMOS, respectively.

The density of interface trap D_{it} extraction from the subthreshold characteristics [31] are presented in Fig. 5. The D_{it} increases exponentially near the conduction band edge for nMOS and valance band for pMOS, which exceeds 10^{13} $cm^{-2}eV^{-1}$. It drops to 10^{12} $cm^{-2}eV^{-1}$ or below towards the mid-gap. The level of D_{it} is comparable to that reported in [32] with similar post-oxidation annealing condition.

Fig. 6 shows the I_D–V_D curves with L = 1 μm and L = 6 μm for both nMOS and pMOS. Devices were characterized by sweeping V_D from 0 to 20 V with a biased V_G from 3 V to 19 V with a 2 V step for nMOS, and V_D from 0 to –20 V with a biased V_G from –3 V to –19 V with a –2 V step for pMOS. The SCE can be further confirmed by the soft-saturation characteristics at the large drain bias region. It can be explained by the drain-induced barrier lowering (DIBL) with short channel length, which causes a reduction of V_{TH}.

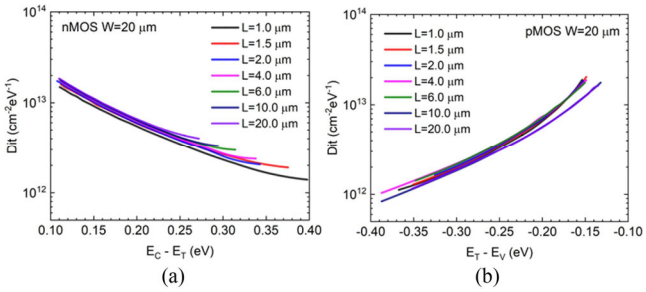

FIGURE 5. D_{it} extraction of (a) N-channel MOSFET; (b) P-channel MOSFETs.

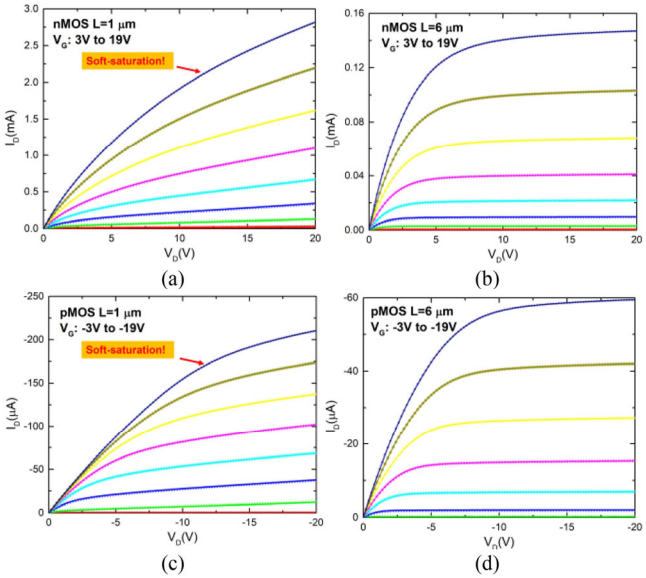

FIGURE 6. I_D–V_D of 20 μm width: n-channel MOSFETs with (a) L = 1 μm and (b) L = 6 μm; p-channel MOSFETs with (c) L = 1 μm and (d) L = 6 μm.

There are several criteria to determine the boundary between "short-channel" and "long-channel" [33], [34], which is referred in the device scaling study to avoid potential instability. An empirical relation can be applied to estimate the minimum channel length L_{min} of SiC MOSFET to avoid the short-channel behavior [2], [35]. The L_{min} is described as

$$L_{min} = A\gamma^B \tag{1}$$

where A is a proportionality factor and 0.4 is typically adopted, B is 1/4 in for SiC [2]. γ is expressed as

$$\gamma = x_j t_{ox}(w_D + w_S)^2 \times 10^4 \tag{2}$$

where x_j is the junction depth in the drain and source regions, t_{ox} is the oxide thickness, and w_D and w_S are the depletion layer widths at the drain and source ends, respectively. The depletion widths w_D and w_S is given by the one-dimensional abrupt junction formulation

$$w_{D,S} = \sqrt{\frac{2\varepsilon_{SiC} V_{bi} + V_{D,S}}{qN_{A(D)}}} \tag{3}$$

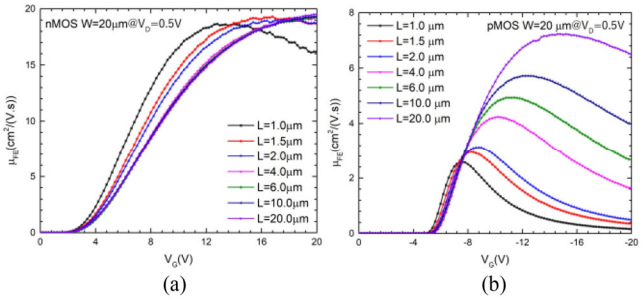

FIGURE 7. μ_{FE} curves extracted from g_m data: with (a) n-channel MOSFETs, (b) p-channel MOSFETs.

where ε_{SiC} is the permittivity of SiC, V_{bi} is the build-in potential in SiC, V_D and V_S in the drain and source voltages, q is the elementary charge, and N_A and N_D are the acceptor and donor concentrations, respectively. Referring to the parameters listed in TABLE 2, the L_{min} estimation of the fabricated devices is 0.9 μm for nMOS and 1.3 μm for pMOS.

Field-effect mobility μ_{FE} is extracted from the transconductance g_m by the following equation

$$\mu_{FE} = \frac{L}{WC_{ox}V_D} g_m \tag{4}$$

where C_{ox} is the oxide capacitance. The mobility curves are presented in Fig. 7. The peak value of nMOS μ_{FE} is around 19 cm^2/(V$\cdot$s), while the peak value of pMOS μ_{FE} ranges from 2.5 to 7.5 cm^2/(V$\cdot$s). As the channel length L decreases, the peak μ_{FE} is getting smaller as it is more obvious in p-channel MOSFETs. This is because p-type (P_+) ohmic contact has much higher resistance than n-type (N_+) leading to the increasing series contact resistance (R_C) effect [36], that the increasing R_C/R_{total} ratio leads to a decrease in effective V_D and V_G. More details of contact resistance results with the characterization of the transfer length method (TLM) are presented in the next section.

B. N/P-CHANNEL MOSFET AT HIGH TEMPERATURE

An nMOS (W = 60 μm, L = 2 μm) and a pMOS (W = 100 μm, L = 4 μm) were characterized from room-temperature up to 300°C. Fig. 8 shows I_D–V_G curves with varying temperatures. It is observed from Fig. 8(a) and (c) that the drain driving current I_D of both nMOS and pMOS increases with higher temperature. Meanwhile, zoom-in regions near the turn-on point in Fig. 8(b) and (d) show a monolithic reduction in V_{TH} with elevated temperatures. The dashed green lines are determined by the CCM to extract the V_{TH}. The increasing I_D at elevated temperature is primarily due to the decrease of contact resistance along with the reduction of V_{TH} causing gate overdrive voltage, while the V_{TH} reduction is due to the increase of intrinsic carrier concentration and lower interface trapped charges at higher temperature, and the channel mobility at low V_G increases.

Further DC I-V characterization has been performed on TLM structures to extract the contact resistance. Especially

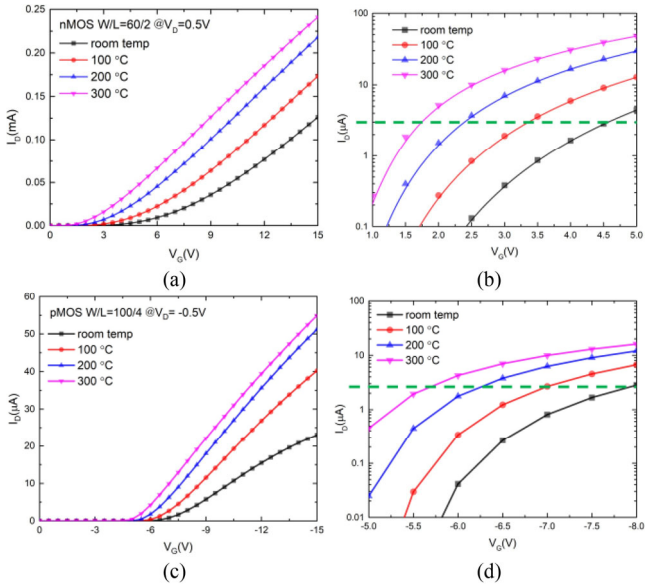

FIGURE 8. (a) I_D–V_G of n-channel MOSFET with W/L = 60 μm/2 μm. (b) $log(I_D)$–V_G of (a) to compare the V_{TH} within the V_G range of 0.5 ~ 3.5 V. (c) I_D–V_G of p-channel MOSFET with W/L =100 μm/4 μm. (d) $log(I_D)$–V_G of (c) to compare the V_{TH} within the V_G range of –4 ~ –6.5 V.
* Sign of I_D of pMOS is transferred to be positive for the convenience of data process especially for the log-scale plot.

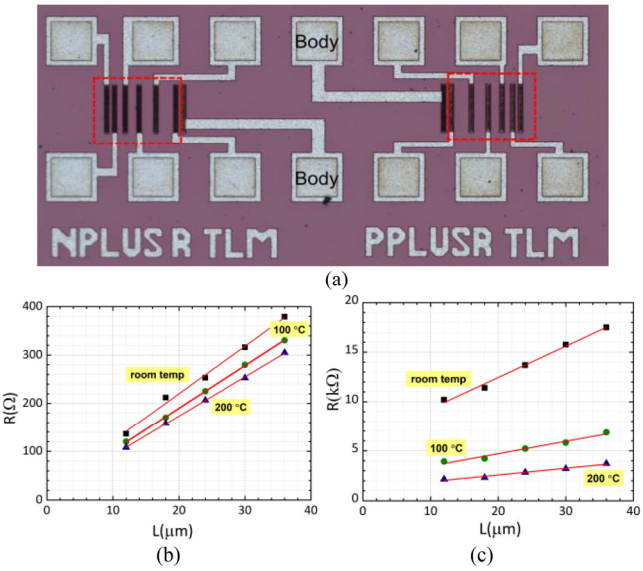

FIGURE 9. (a) Top view of N+ and P+ TLM structures. (b) Resistance versus resistor length of N+ TLM at different temperatures. (c) Resistance versus resistor length of P+ TLM at different temperatures.

TABLE 3. Extraction results.

Parameters	Room temperature	100°C	200°C
R_S of N+ [Ω/□]	983	884	815
R_S of P+ [kΩ/□]	31.6	12.4	6.7
ρ_C of N+ [$\Omega \cdot cm^2$]	1.37×10^{-5}	4.83×10^{-6}	3.43×10^{-6}
ρ_C of P+ [$\Omega \cdot cm^2$]	0.0297	0.01	5.69×10^{-3}

for p-channel MOSFET, the huge difference among the mobilities in Fig. 7(b) implies P + ohmic contact has much higher resistance than N+. Fig. 9(a) gives the top view of the N+/P + TLM with 100 μm width. The total resistance R versus the resistor length L is extracted and the linear curving fitting results are shown in Fig. 9(b) and (c). TABLE 3 gives the extraction summary of N 4P + source/drain sheet resistance and N+/P+ contact resistivity. As expected, the resistances of P+ and N+ regions decrease with temperature increasing which is related with the ionization at high temperature. It is more obvious when it comes to Al since the activation rate of Al is not high enough as compared to N. As temperature increases, the sheet resistance of P+ region decreases more significantly as it is shown in the table that the sheet resistance drops from 31.6 kΩ/□ at room temperature to 6.7 kΩ/□ at 200°C. Moreover, the extracted contact resistivity of P+ shows at least three orders higher than N+ contact, and it contributes a considerable portion to the on-resistance of the MOSFETs. The higher Schottky barrier height of Al than N along with incomplete ionization of Al significantly hinders the formation of ohmic contacts due to a lower free carrier concentration, which leads to a higher Schottky barrier height at the metal-semiconductor interface. For example, the extracted specific on-resistance ($R_{ON,sp}$) of nMOS at $|V_G|$ = 19 V, $|V_D|$ = 1 V in Fig. 6(b) and pMOS in Fig. 6(d) are 0.024 Ω.cm^2 and 0.15 Ω.cm^2, respectively. The P+ source and drain contact resistivities are approximately 40% of the total $R_{ON,sp}$. Though both P+ and N+ contacts are ohmic which are formed on heavily doped regions, the higher resistivity of P+ contacts over N+ adversely affect the pMOS performance such as driving current capability and field-effect mobility. The existing methods for creating ohmic contacts to n-type SiC are generally deemed adequate for commercial manufacturing. However, the process of forming p-type contacts still remains a significant challenge, posing limitations to the advancement of highly reliable IC technology [37].

The μ_{FE} extraction results of the nMOS and pMOS at high temperature are given in Fig. 10. The peak is shifted to the lower gate electric field as temperature increases, which is consistent with the trend of V_{TH}, while the peak value increases due ionization and reduction of contact resistance. More analysis of the mobility regarding the scattering mechanisms will be presented in the simulation section.

III. SIMULATIONS AND DISCUSSION

Sentaurus TCAD software from Synopsys was used to perform MOSFET simulation. Structures were created based on the device layout given in Fig. 3. Monte-Carlo ion implantations were adopted to form the N-well, P-well, N+ and P+ regions. The mesh was made fine near the junctions and surface in order to capture the rapid change in potential and charge concentration and avoid the convergence problem. In the inversion layer, the mesh spacing is kept as low as 1 Å close to the surface while spacing is sufficiently large in

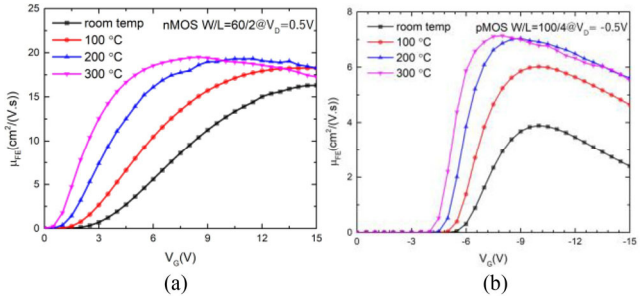

FIGURE 10. μ_{FE} curves with varying temperature extracted from g_m data: with (a) n-channel MOSFET with W = 60 μm, L = 2 μm, (b) p-channel MOSFET with W = 100 μm, L = 4 μm.

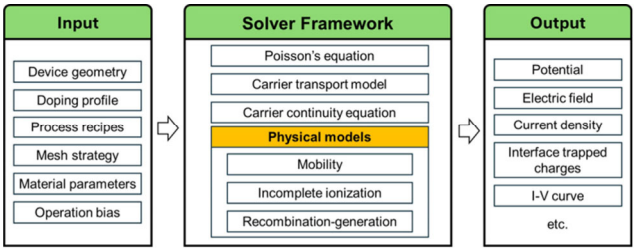

FIGURE 11. Framework of TCAD simulator.

regions where there are no abrupt changes in the distribution of charges, electric field and electrostatic potential etc., to improve the simulation speed. Simulations are conducted at room temperature with varying channel dimensions as well as at high temperature up to 300°C. The framework of simulation including the input, solver, and output is shown in Fig. 11. The key physical models are mobility-related models (scattering mechanism models, fixed charges at the SiC-SiO_2 interface, and interface trap distribution), incomplete ionization, and recombination-generation models (Schockley-Read-Hall (SRH) recombination and Auger recombination model). Among all the models, scattering mechanisms, fixed oxide charge, interface trap distribution are the main models in which the parameters are modified and calibrated according to the characterization results. Simulation on P-channel MOSFET has been conducted. The P-type contact also needs to be calibrated due to the high contact resistance as reported in Fig. 9 compared to N-type that it cannot be neglected. The V_{TH} estimation of p-channel MOSFET can be obtained by the equations [1]:

$$V_{FB} = \varphi_{Poly} - \varphi_S - \frac{Q_{OX}}{C_{OX}} - \frac{Q_{IT}(\psi_S = 0)}{C_{OX}} \tag{5}$$

$$V_{TH} = \left(\varphi_{Poly} - \varphi_S - \frac{Q_{OX}}{C_{OX}} - \frac{Q_{IT}(\psi_S = 2\psi_F)}{C_{OX}}\right) - 2|\psi_F| - \frac{\sqrt{4\varepsilon_{SiC} q N_D |\psi_F|}}{C_{OX}} \tag{6}$$

where φ_{Poly} and φ_S are the work functions of the polysilicon and substrate, respectively. ψ_F represents the surface potential for inversion. Q_{OX} is the fixed charges. C_{OX} is the capacitance of the oxide between the substrate and gate per unit area. $Q_{IT}(\psi_S = 0)$ is the interface charges at the flat band. $Q_{IT}(\psi_S = 2\psi_F)$ is the interface charges at the starting point of strong inversion. N_D is the donor doping concentration of the substrate for the pMOS. q is the elementary charge, and ε_{SiC} is the permittivity of silicon carbide. From (5) and (6), the V_{TH} deviates from the ideal value due to the presence of Q_{IT} and Q_{OX}, and the incomplete ionization of donors N_D. Without considering incomplete ionization, there is an overestimation of V_{TH} (absolute value). However, the effect is relatively little due to a higher activation rate of nitrogen (>98%). For most SiC processes, Q_{OX} has a level of 10^{12} cm^{-2} [31], which will have more impacts on the switching performance along with interface traps.

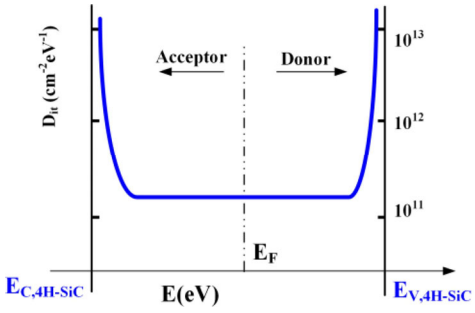

FIGURE 12. Interface traps density distribution of 4H-SiC.

The distribution model of the interface trap density for 4H-SiC refers to [39], which has a constant distribution in the midband region and an exponential increase near the edge of the band as shown in Fig. 12. The energy dependent density of trap states is expressed as

$$D_{it}(E) = D_{it,mid} + D_{it,edge} exp\left(\frac{E - E_C}{\sigma_{it}}\right) \tag{7}$$

$$D_{it}(E) = D_{it,mid} + D_{it,edge} exp\left(\frac{E_V - E}{\sigma_{it}}\right) \tag{8}$$

where, E_C and E_V are the energy at the conduction band edge and valance band edge respectively, $D_{it,\mathrm{mid}}$ and $D_{it,\mathrm{edge}}$, represent the densities at the middle and the edge of the bandgap, and σ_{it} defines the curvature of the density of states curve. It is noted that the traps close to the intrinsic Fermi level are the most effective generation-recombination centers. Equation (7) and (8) represent the acceptor-like traps above the midgap and the donor-like traps below the midgap, respectively. They present the different polarities as shown in Fig. 13. The extracted D_{it} in Fig. 5 is only available over a limited energy range from 0.1eV to 0.4eV. We extrapolate the full bandgap distribution by fitting the extracted D_{it} to the model as shown in Fig. 12, and we have: $D_{it\_\mathrm{mid}} = 2 \times 10^{11} cm^{-2} eV^{-1}$, $D_{it\_\mathrm{edge}} = 1 \times 10^{14} cm^{-2} eV^{-1}$, and $\sigma_{it} = 0.067 eV$. The accuracy of the extrapolated D_{it} distribution is verified and assured by comparing the simulation and characterization results. The results can be improved with further calibration.

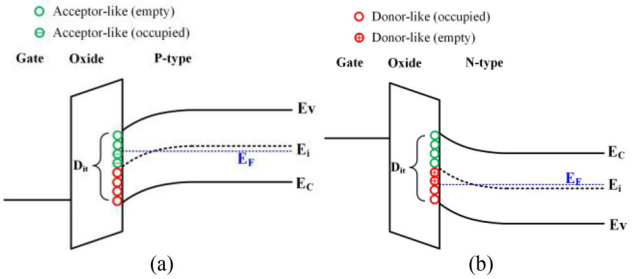

FIGURE 13. Energy band diagram illustrating interface traps in MOSFETs at inversion for (a) n-channel MOSFET; (b) p-channel MOSFET.

The transfer and output characteristics of p-channel MOSFETs with varying channel geometry were conducted at room temperature. Fig. 14(a) is the cross-section of a p-channel MOSFET created based on the device structure given in Fig. 3. The simulation of pMOS I_D–V_G was performed by sweeping V_G from 0 to –20 V at V_D = –0.5 V. Fig. 14(b) shows the simulated curves with varying L and the V_{TH} extraction using the same CCM as mentioned above. The V_{TH} is stabilized at –7.8 V for long-channel device while the short-channel effect is prominent with channel length less than 2 μm. With the adopted interface traps distribution model and calibrated contact resistance value from the measurement, both the transfer curves and the extraction results match very well with the characterization results. Fig. 14(c) and (d) show the pMOS I_D–V_D curves with L = 1 μm and L = 6 μm, respectively. Simulations were conducted by sweeping V_D from 0 to –20 V with a biased V_G from –3 V to –19 V with a –4 V step size. The soft-saturation characteristic of the pMOS with L= 1 μm at large drain bias confirms the SCE as illustrated in Fig. 6.

The channel mobility of a pMOS is affected by four scattering mechanisms, which is modelled using Matthiessen's rule as [40]

$$\frac{1}{\mu_{\text{Total}}} = \frac{1}{\mu_B} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_{SP}} + \frac{1}{\mu_C} \tag{9}$$

where μ_B represents the bulk mobility [41], [42], [43] that is the ionized impurities scattering in the body, μ_{SR} is surface roughness scattering [44], μ_{SP} is the surface phonon scattering [45], and μ_C is the Coulomb scattering [46], [47] due to the interface traps,. All the four terms in this work are modelled as:

$$\mu_B = \frac{\mu_{max}\left(\frac{300}{T}\right)^{\alpha} - \mu_{min}}{1 + \left(\frac{N_D}{N_{REF}}\right)^{\beta}} + \mu_{min} \tag{10}$$

$$\mu_{SR} = \frac{\delta_{SR}}{E_\perp^2} \tag{11}$$

$$\mu_{SP} = \frac{A}{E_\perp} + \frac{B}{TE_\perp^{1/3}} \tag{12}$$

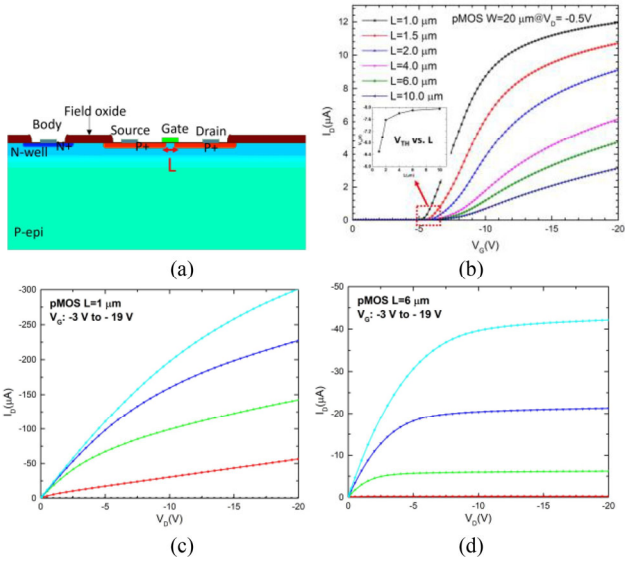

FIGURE 14. (a) cross-section of the p-channel MOSFET. (b) I_D–V_G simulation results with varying L and the inset of V_{TH} extraction. I_D–V_D simulation results of 20 μm width p-channel MOSFETs with (c) L = 1 μm and (d) L = 6 μm.

$$\mu_C = \frac{\mu_0 \left(\frac{T}{300}\right)^{\kappa} \left(1 + c\left(\frac{N_{it}}{N_0}\right)^{\alpha_1}\right)^{\sigma}}{\left(\frac{N_{it}}{N_0}\right)^{\alpha_2} D(x) f(E_\perp)} \tag{13}$$

where μ_{max} represents the mobility of an undoped sample, while μ_{min} is the mobility in the highly doped material, N_{REF} is the doping concentration at which the mobility is halfway between μ_{max} and μ_{min}, N_D is the donor impurity concentration, $E_\perp$ is the perpendicular electric field, c is the concentration of the holes near the interface, N_{it} is the density of the interface traps by integrating the function $D_{it}(E)$, $f(E_\perp)$ is the probability function for finding charged traps at $E_\perp$, $D(x)$ is a factor of distance from the surface where x is the distance from the surface, α, β, A, B, μ_0, α_1, α_2, κ, N_0, and σ are the fitting parameters. The functions $D(x)$ and $f(E_\perp)$ are given by

$$D(x) = e^{-\frac{x}{l_{crit}}} \tag{14}$$

$$f(E_\perp) = 1 - e^{-\left(\frac{E_\perp}{E_0}\right)^{\tau}} \tag{15}$$

where, τ l_{crit} and E_0 are the fitting parameters.

μ_{SR} is a proportionality constant that accounts for the combined effects of various parameters including the roughness correlation length, oxide permittivity and the wave vector at the Fermi surface. Therefore, surface roughness scattering is highly dependent on the quality of the interface, which varies from process to process. From the equation (11) that surface roughness becomes dominant to affect the channel mobility at the high-field region because of an index of 2, while surface phonon and Coulomb scatterings are dominant in low electric field. The values of the parameters involved in our simulation of scatterings are listed in TABLE 4.

TABLE 4. Parameters for 4H-SiC mobility model.

Eq.	Parameters	Unit	Value
(10)	μ_{max}	$cm^2/(V{\cdot}s)$	125
	μ_{min}	$cm^2/(V{\cdot}s)$	40
	N_{REF}	cm^{-3}	2.23×10^{17}
	α		-2.4
	β		0.76
(11)	δ_{SR}	V·s	1×10^{13}
(12)	A	cm/s	8.1×10^{5}
	B	$(V/cm)^{-2/3}{\cdot}K{\cdot}cm/s$	8.36×10^{3}
(13)	μ_0	$cm^2/(V{\cdot}s)$	40
	α_1		1.0
	α_2		0.5
	σ		1.5
	κ		1.0
(14)	l_{crit}	cm	1×10^{-6}
(15)	E_0	V/cm	2×10^{5}
	τ		2.0

With the completed models, we probe inside the device to gain further details which usually cannot be acquired by direct measurements. The channel mobility close to the surface (surface mobility) as a function of position in the channel of a pMOS with 4 μm channel length is presented in Fig. 15. The simulation was performed at $V_D =$ –0.5 V with varying V_G at 0V, –5 V, –10 V, –15 V, and –20 V. A cutline below the surface along the channel region shown in Fig. 15(a) was placed to extract the hole's surface mobility. The total cutline length is 5 μm. The 4 μm channel position along the cutline is from 0.5 μm to 4.5 μm. It is noticed in Fig. 15(b) that the mobility for a given gate voltage across the effective channel length (which is less than the defined channel length due to the diffusion of the drain/source ion implantation regions) is fairly constant in the linear operation region. It shows that at V_G at –5 V, which is just below threshold, the surface mobility is approximately 30 $cm^2/(V{\cdot}s)$. As the gate voltage decreases to –20 V, the surface mobility decreases dramatically from 30 $cm^2/(V{\cdot}s)$ at $V_G =$ –5 V to 6 $cm^2/(V{\cdot}s)$ at $V_G =$ –20 V. It is also observed that the surface mobility increases close to the source and drain region when the pMOS is operating at inversion. This is due to the existence of the depletion regions where the vertical field is lower than the channel. This gives rise to less surface scattering given in equations (11) and (12).

Fig. 16 shows the interface trap density and occupation probability of these traps as a function of energy with different gate bias. When the trap is occupied (the occupation possibility =1), the trap shows the polarity as illustrated in Fig. 12. It is observed that the 100% possibility curve of trap occupation moves toward the valence band edge rapidly as the gate bias decreases. Total occupied interface trap density in the SiC/SiO_2 interface along the cutline range shown in Fig. 15(a) as a function of the gate bias is presented in

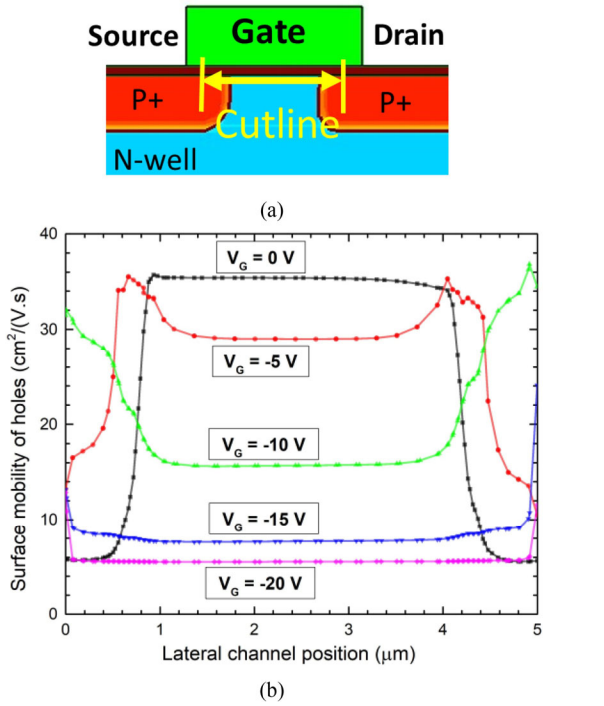

FIGURE 15. (a) Cross-section of the channel region, (b) surface hole mobility as a function of position in the channel simulated at $V_D =$ –0.5 V, and $V_G =$ 0V, –5 V, –10 V, –15 V, and –20 V.

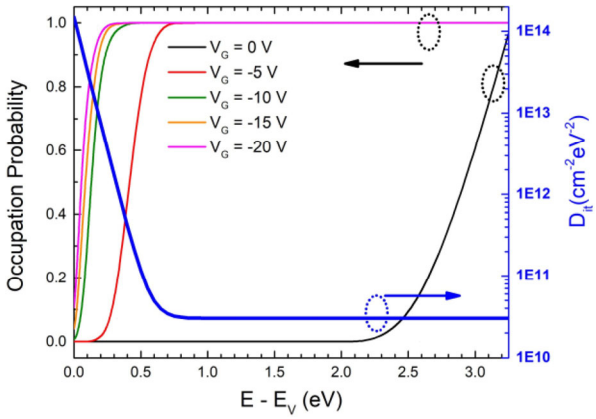

FIGURE 16. Interface trap density (right) and occupation probability (left) as a function of energy for pMOS.

Fig. 17. As expected from Fig. 15, the occupation of the traps increases for lower gate voltage since with the decrease in gate voltage, holes are pulled closer to the interface that increases the hole concentration in the channel. These occupied traps act as a major role in the Coulomb scattering. Regarding the scattering mechanisms in equation (9), at low-field region, surface phonon and Coulomb scattering limit the mobility, while at high-field, surface roughness becomes the dominant scattering mechanism. The simulation results with models calibrated against our experimental results confirm that enhancing oxide quality significantly improves mobility, and this remains a primary area of future work.

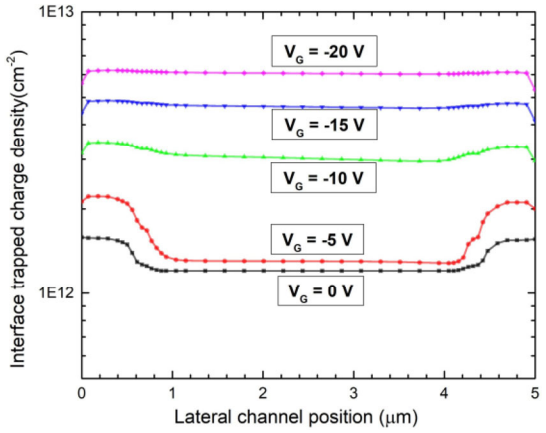

FIGURE 17. Interface trapped charge density (occupied interface traps) as a function of energy with different gate bias.

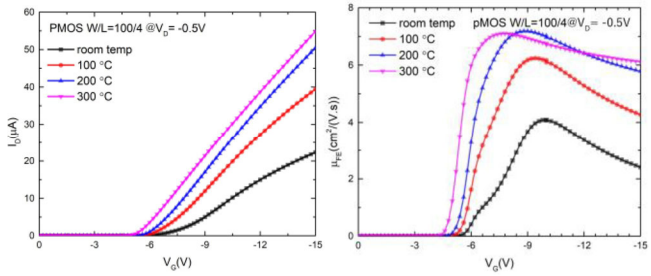

FIGURE 18. (a) I_D–V_G of p-channel MOSFET with W = 100 μm, L= 4 μm, (b) μ_{FE} curves with varying temperature.

Besides the room temperature, the simulation deck also yields good results at high temperature. The I_D–V_G and μ_{FE} of n-channel MOSFET with W= 100 μm and L=4 μm are presented in Fig. 18, which match very well with the experimental results in Fig. 7(c) and 9(b). The calibrated mobility and interface traps models agree with the experiment as moving to the high temperature application since the models have been defined as temperature dependent. The developed simulation deck for SiC pMOS, which specifically accounts for the individual effects of numerous physical mechanisms, is very useful to predict how device performance could be improved.

IV. CONCLUSION

Both n-channel and p-channel MOSFETs fabricated with the optimized Fraunhofer IISB SiC CMOS process are characterized from room temperature to 300°C. The SCE arises when the channel length reduces to a certain point which can be estimated by the presented empirical relationship. The low mobility extraction results (the peak μ_{FE} for nMOS is less than 20 cm^2/(V·s) while the pMOS is below 8 cm^2/(V·s).) lead to thorough SiC/SiO$_2$ interface studies. The interface trap distribution and scattering models adopted in the TCAD simulation for the p-channel MOSFET yield good simulation results matching well with the characterizations. Meanwhile, the high p-type ohmic contact resistivity is observed compared to the n-type ohmic contact and this is further verified by the characterization of TLM structures. It still remains a challenge to get a low ohmic p-type contact resistivity for commercial manufacturing. Overall, this research shows a promising potential of SiC low voltage MOSFETs to be monolithically integrated with SiC power devices and operate under harsh environments which Si counterparts cannot achieve.

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