2D Amorphous Homojunction Transistors Exfoliated from Liquid Metals

*Minh Nhut Le, Md Saifur Rahman, Simon A. Agnew, Samuel W. Ong, and William J. Scheideler**

Thayer School of Engineering

Dartmouth College, Hanover, NH 03755, United States

E-mail: william.j.scheideler@dartmouth.edu

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Abstract

Ultrathin 2D metal oxides are a high-performance class of transparent conducting materials capable of overcoming the traditional limitations of inorganic flexible electronics. The low temperature, thermodynamically favorable synthesis of 2D oxides at liquid metal interfaces offers the potential for printing these materials over large areas at unprecedented speeds with sub-nanometer scale precision. However, these native oxides are sub-stoichiometric and highly conductive, so new strategies are needed that can precisely engineer the electrostatics and enhance stability. In this work, we engineer the crystalline vs. amorphous phase of 2D oxides via alloying of ternary $In_{1-y}Sn_yO_x$ and utilize ultralow deposition temperatures (120 – 160 °C) afforded by In-Sn eutectics. We extend this approach to rapid assembly of nanoscale (3-5 nm per layer) vertical 2D homojunctions with electrostatically favorable grading from high density of states front channels to lower density of states back-channels. Detailed materials characterization reveals how this platform enhances electron mobility while improving resilience under bias-stress in metal oxide transistors. Devices based on amorphous 2D oxide homojunctions with high-k sol-gel ZrO_x dielectrics achieve excellent electron mobility (30 $cm^2/V{\cdot}s$), steep switching (SS of 100 mV/dec), $I_{on/off}$ of 10^7 and 10X reduced bias-stress shifts, presenting an ideal strategy for high-performance flexible oxide electronics.

1. Introduction

In the era of the Internet of Things (IoT), the rapidly growing demand for flexible, wearable, and portable electronics has introduced challenges that conventional silicon-based materials struggle to meet due to their inherent rigidity, brittleness, and limited mechanical flexibility. Recently, two-dimensional (2D) metal oxide materials just 1 – 5 nm thick have attracted significant attention as a promising alternative for high-performance flexible electronics,[1] offering exceptional mechanical flexibility[2] combined with superior electronic mobility[3,4] and conductivity[5] as well as superlative interfaces to other 2D materials such as transition metal dichalcogenides.[6] These unique characteristics make 2D oxides particularly suitable for expanding the application of printed electronics into diverse domains such as personalized healthcare devices, wearable sensors,[7] and information display.[8–10]

Recently, ALD and sputtered oxides have demonstrated that ultrathin (1-6 nm) InO_x and ITO[11,12] can be utilized as semiconducting channels with a high density of states (DOS) that perform surprisingly well (I_{on} > 2 mA/ μm) in scaled (L_g < 20 nm) channel-length devices,[11,13] highlighting the state of the art performance achievable and the potential for high-speed circuits based on amorphous oxides[14]. These advancements validate the intrinsic suitability of 2D oxides for next-generation electronics and motivate further exploration of alternative, scalable, and low-temperature fabrication methods for high-quality 2D oxide films. However, in many cases, 2D native oxides are highly sub-stoichiometric and their relatively high oxygen vacancy concentrations result in high carrier concentrations that must be controlled for thin film transistor applications[1,15] via composition or precise engineering of the channel layer thickness at the sub-nm scale.[16]

Engineering ternary or quaternary oxides via doping and alloying is known to control the high intrinsic carrier concentration of these semiconductors. Although aliovalent dopants such as Sn can produce degenerate ITO for transparent electrodes,[2,7] they can also enhance semiconducting qualities of 2D InO_x as shown by recent work by Tang, et al.[17] Oxygen getters such as Ga are also well established to mitigate the oxygen vacancies and reduce the free carrier concentration(e.g. Ga-doping[18,19]). Recent literature has shown that doping Sb,[16] Sn,[17] or Zn[20] into the InO_x system can improve both channel conductance and carrier mobility but generally comes with a tradeoff of increased off-current and weaker subthreshold slope. Amorphous oxide semiconductors combining Ga, Sn, and Zn (e.g. IGZO) are traditionally known to demonstrate steeper switching and improved bias-stress stability, but previous attempts to implement such

quaternary 2D oxides using liquid metal printing have been confounded by mixed polycrystalline-amorphous phases[21,22] and have utilized higher printing temperatures (300 °C).

2D oxides can advance closer to circuit level applications only if we can control channel conductance, enhance uniformity, and improve bias-stress stability. Stabilizing the amorphous phase of 2D oxides while keeping high performance has not been achieved, though amorphous films are known to solve these issues based on decades of experience in the display industry.[23] However, this also requires strategies to mitigate the well-established tradeoff between mobility and stability.[24] The unique challenge in the case of 2D oxides for flexible electronics is the resulting need to engineer the properties of inorganic semiconductors at temperatures compatible with flexible substrates. Here, we present two innovations to overcome these challenges for printed oxide electronics. First, we grow an amorphous phase of 2D ITO over large areas using ultra low

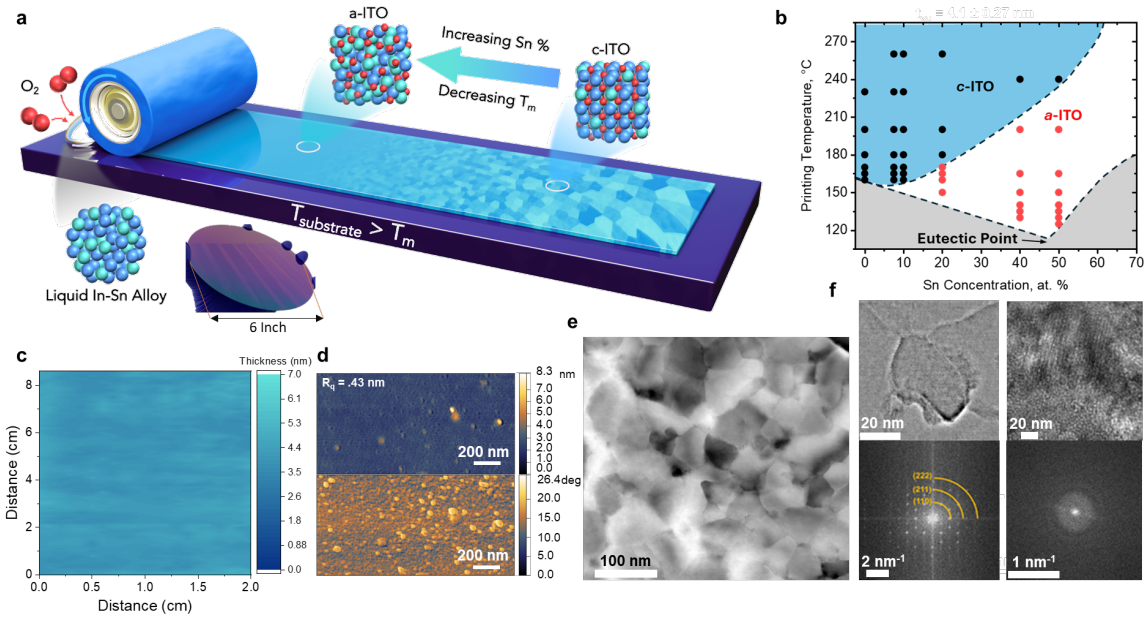

Figure 1*: a) Schematic of roller-based continuous liquid metal printing from In-Sn alloys showing variable amorphous vs crystalline phase vs. Sn concentration and image of multiple printed strips of 2D ITO on a 6-inch SiO_2/Si wafer. T_m is the melting temperature of the metal precursor alloy. b) Empirically determined phase diagram of ITO films showing the XRD-determined amorphous (a-ITO) vs. polycrystalline (c-ITO) phase as a function of printing temperature and Sn concentration. Measurements are of the as-deposited films. Grey shading indicates conditions below the melting temperature, T_m. c) Thickness heatmap of a film of 20% Sn 2D ITO printed at 160°C. d) AFM height image (top) and phase image (bottom) of crystalline 2D ITO (7.5 wt% Sn) printed at 170 °C. R_q reports the RMS roughness. Rq = 0.43 nm based on entire height image (R_q = 0.35 nm excluding the two rightmost asperities). e) High-resolution transmission electron microscopy (HRTEM) image. f) HRTEM image of a crystalline domain (left) of 10% Sn 2D ITO after 250 °C annealing and an amorphous region (right) of 20% Sn 2D ITO after 250 °C annealing, with the corresponding fast fourier transform on the bottom.*

temperature hypoeutectic liquid metal printing (120 – 160 °C). Second, we engineer layered homojunctions of 2D oxides to integrate high-mobility front channels and high-stability back channels using variable Sn doping. The result is that we can achieve superlative on-state performance while yielding steep turn on (SS of 100 mV/dec) and enhanced stability (10X improvement in bias-stress compared with uniformly doped channels) simultaneously with high on-state performance.

2. Results & Discussion

This study applies a version of kinetically controlled roller-based continuous liquid metal printing (CLMP) established in our earlier work,[15] to achieve the deposition of large-area amorphous ITO films from hypoeutectic In–Sn alloys at ultra-low temperatures (120–160 °C). In contrast to the majority of previous 2D oxide thin-film transistor (TFT) studies, which rely heavily on crystalline oxide materials known for high mobility yet limited mechanical resilience, the present approach exploits amorphous-phase 2D oxide layers that have the potential to offer enhanced mechanical flexibility and improved uniformity for large scale circuit applications. The process utilized here involves the Cabrera Mott oxidation of the surface of a liquid metal meniscus. Thanks to the liquid nature of the parent metal alloy, the absence of strong macroscopic forces between the liquid metal and the thin 2D oxide layer facilitates clean exfoliation and transfer onto another substrate at temperatures above the melting point of the metal alloy.

As illustrated in **Figure 1a**, the deposition process involves heating the target substrate, followed by rolling the droplet across the substrate to translate the liquid metal meniscus and transfer the solid surface oxide continuously. This CLMP technique is scalable, performed under ambient conditions, and supports high-throughput, roll-to-roll compatible processing without the need for lengthy post-annealing due to the inherently conductive phase of the sub-stoichiometric 2D oxide. As a clear demonstration of the scalability and high-throughput potential of this method, an image is shown featuring a series of uniformly printed strips of 2D ITO on a 6-inch SiO_2/Si wafer. Furthermore, by leveraging variable Sn doping (up to 40%) and variable temperature we can control the deposition of crystalline (For 160 °C prints with 10% Sn as confirmed in **Figure S1**) vs. amorphous films (≤160 °C prints w/ 20% or 40% Sn, which remain amorphous after post annealing, as shown in **Figure S1**). To systematically understand how the processing conditions

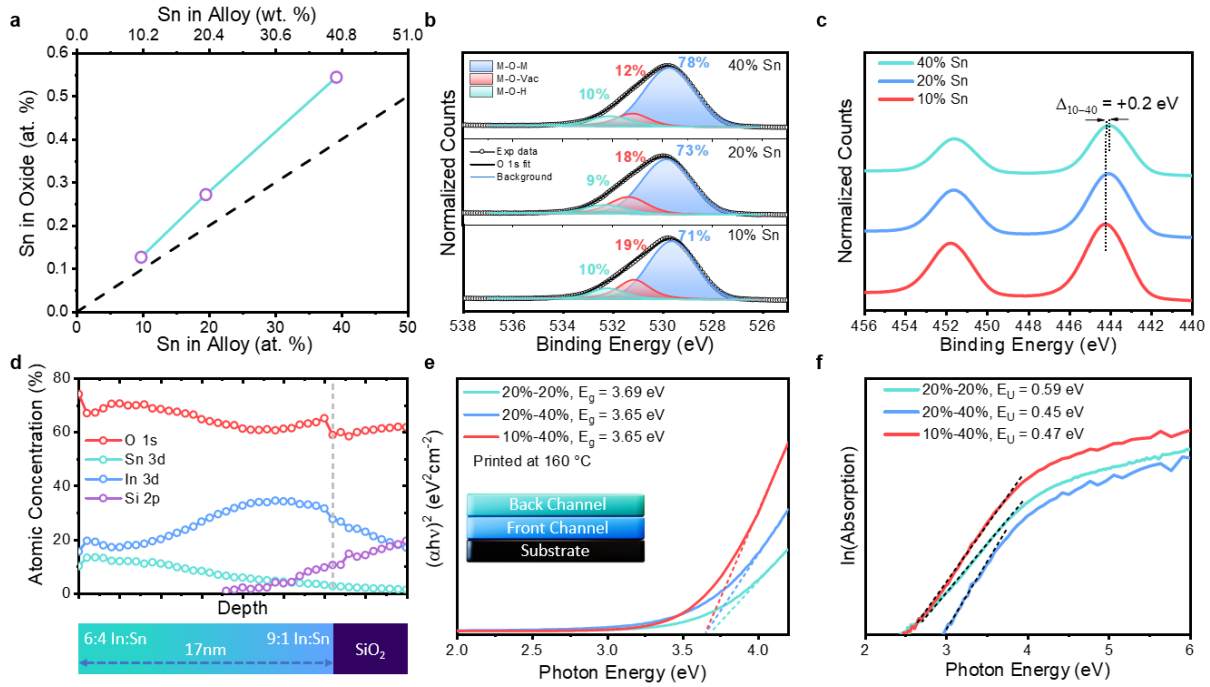

***Figure 2**: a) Sn atomic percentage in the oxide as determined by XPS analysis, as a function of Sn wt% (top axis) and at% (bottom axis) in the alloy. The dashed line represents a 1:1 ratio between the Sn concentration in the alloy and the resulting Sn concentration in the oxide film. X-ray photoelectron spectroscopy (XPS) analysis of (b) O 1s and (c) In 3d peaks for 10%, 20%, and 40 wt%-Sn 2D ITO films after 200°C post-annealing. d) XPS analysis of homojunction 2D ITO 10%/40% as a function of etching step. 4-layers sample is used for XPS measurement to avoid the substrate signal. e) Tauc plot of homolayer 20%/20% film and homojunction 10%/40%, 20%/40% film. f) Urbach energy (E_u) analysis of 2D ITO films including the homolayer 20%/20% film and homojunction 10%/40%, 20%/40% films.*

lead to these different phases, we constructed a phase diagram based on experimental XRD analysis, as shown in **Figure 1b** for the as deposited films. Each data point in the diagram corresponds to a unique deposition condition and a film characterized via XRD. The shaded regions denote empirically determined phase regimes, revealing distinct windows in which either the amorphous or crystalline 2D oxide phases are observed. This diagram shows two interesting features. First, the heavier Sn doping closer to the eutectic point (~ 1:1 wt%) enables lower temperature printing down as low as 120 °C, which is significantly lower than past liquid metal printing works utilizing InO_x.[2,7] The second result of heavier Sn doping is that the amorphous phase can be maintained, even at higher deposition temperatures that otherwise result in crystalline films. This enables control over the electronic properties and oxygen stoichiometry without inducing crystallization, even during post-annealing (**Figure S1**). **Figure 1c** presents a thickness heatmap of a single printed 2 × 8 cm ITO film, measured by spectroscopic reflectometry using the robotic gantry system shown in **Figure S2**. The printed film by CLMP shows a uniform thickness

around 4.1 ± 0.3 nm over the 16 cm^2 area. A study on the effect of varying Sn wt% on film thickness was also conducted under identical printing speed and temperature conditions, as shown in **Figure S3**. Notably, the resulting film thickness (~ 3.5 nm) varies little as a function of the Sn concentration.

For the low Sn% printed crystalline films, the morphology and grain size were studied by AFM height and phase imaging. AFM analysis (**Figure 1d)** show that the c-ITO has a smooth surface with rms roughness of 0.43 nm and an average lateral grain size of 45 ± 13 nm (**Figure S4**), showing the plate-like, 2D shape of the grains in these films. High-resolution TEM (HRTEM) as well as energy-dispersive x-ray spectroscopy (EDS) elemental mapping obtained by printing the films directly onto TEM grids (**Figure 1e** and **Figure S5**) show the high crystallinity of the 2D ITO with lower Sn concentrations and display uniform distribution of In, Sn and O, consistent with observations reported in our previous study.[7] The presence of distinct Moiré fringes further supports the formation of overlapping crystallites in a single printed layer, indicating substrate-aligned but non-epitaxial growth of the top and bottom surface oxides from the liquid metal meniscus. **Figure 1f** shows a HRTEM image of the printed film prepared under the amorphous printing conditions, as defined within the amorphous regime of the phase diagram. The image reveals a uniform, featureless texture across the field of view, indicative of a smooth and amorphous film morphology.

As shown in **Figure 2a**, the stoichiometry of the 2D ITO film scales linearly with the Sn composition of the precursor alloy. A 1:1 mapping between the precursor alloy and oxide film is shown for reference in **Figure 2a** as a dotted line. XPS analysis shows that Sn is slightly overrepresented in 2D ITO (~54.4 at% in the oxide film vs. 39.2 at% in the alloy), at a ratio roughly in line with those reported by Datta et al. for 2D ITO printed at 200 °C.[2] We note that compared with alternative dopants such as Ga, Sn doping is more controllable. For example, we have found previously that Ga doping at just 0.001 wt% Ga in the IGO precursor alloy led to 8 at% Ga in the oxide film.[18] For clarity and simplicity, all Sn% values mentioned for the devices refer to weight percent used in the precursor alloy (**Figure 2a** shows both wt% and at%).

Sn doping significantly modifies the oxygen stoichiometry of the 2D ITO films. **Figure 2b** and **Table S1** show the XPS O1s spectrum of a film printed from alloys with 10, 20, and 40% wt Sn. These peaks can be deconvolved into three separate peaks centered at 529.7 ± 0.1, 531.2 ± 0.1, 532.2 ± 0.1 eV metal-oxygen-metal bonds (M-O-M), metal-oxygen bonds near oxygen vacancies (M-O_{Vac}) and metal-oxygen bonds in hydroxide or surface groups (M-OH), respectively. We

observe that with increasing Sn concentration, the portion of M-O-M bonding increases from 71% (10% Sn) to 78% (40% Sn) and the portion of M-O_{Vac} decreases from 19% (10% Sn) to 12% (40% Sn), indicating that the film is more stoichiometric with greater Sn incorporation. This would suggest that heavy Sn doping should subsequently reduce the free carrier concentration and lower the Fermi level (E_f). **Figure 2c** shows the In *3d* spectrum of the ITO films with 10, 20 and 40 wt% Sn. The In $3d_{5/2}$ is centered at 444.3 eV and In $3d_{3/2}$ is centered at 451.8 eV for 10% Sn doping, showing that no metallic indium remains in the film. The 0.2 eV shift in the In $3d_{5/2}$ and In $3d_{3/2}$ to lower peak binding energy when doping additional Sn also supports that greater Sn incorporation will lower the E_f.[25]

As we have shown in previous work, the unique ability that rapid liquid metal printing affords is to stack 2D oxides with varying electronic properties. In this case, we assemble 2D oxides with variable Sn doping into homojunctions comprised of 3 – 5 nm thick layers. To fabricate the homojunction, we first print low Sn concentration layers on the bottom and then print higher Sn concentration layers on top of the stack. The XPS depth profile study in **Figure 2d** illustrates the formation of the homojunction of 10% Sn on bottom and 40% Sn on top (10%/40%). This result confirms that starting from the top layer to bottom layer, the In content gradually increases and Sn content decreases as expected. Unlike sol-gel processing or other high temperature methods, interdiffusion between layers is presumed to be limited due to the dense layers and low temperatures utilized here. Additionally, the oxygen content of the top layer is higher than that of the bottom layer, which supports the role of heavier Sn doping in oxygen vacancy suppression. Tauc plots in **Figure 2e** based on optical absorption show the optical bandgap values of homolayer (20%/20%) and homojunctions (10%/40% or 20%/40%). The optical bandgap values of these films are similar, showing that the interface, unlike heterojunctions of InO_x / GaO_x,[15] does not produce significant Burstein Moss shifts. **Figure 2f** shows the Urbach energy comparison of the homojunctions and homolayers. Compared to E_u ~ 0.59 eV of 20%/20%, the 20%/40% and 10%/40% show lower Urbach tail energies of 0.45 eV and 0.47 eV, respectively. This indicates that the homojunctions have fewer optically active subgap defects than the homolayer, specifically that the oxygen rich layers on the top of the film may be helping to reduce the surface defects.

To study the effect of the vertical homojunction structures, we characterized the electrical performance of thin-film transistors fabricated with homolayers and homojunctions as shown in **Figure 3a**. First, we investigated the effect of printing temperature on the electrical performance of 2D ITO films by fixing the Sn concentration at 20 wt% and varying the printing temperature

between 140 °C, 150 °C, and 160 °C. The transfer characteristics and a summary of the electrical performance are presented in **Figure 3a** and **Table S2**. As the printing temperature increases from 140 °C to 160 °C, the mobility improves from 12 cm²/ V·s to 25 cm²/ V·s Meanwhile, the turn-on voltage and threshold voltage shift negatively from –65 V and 17 V to –100 V and –11 V, respectively, indicating a higher carrier concentration in films printed at 160 °C compared to those at 140 °C. The measured channel thicknesses of 12.4 ± 0.4 nm (140 °C), 12.8 ± 0.1 nm (150 °C), and 11.2 ± 0.3 nm (160 °C), as shown in **Table S3,** are similar, suggesting that the elevated print temperatures nearest the threshold for crystallization form more conductive channels with higher electron mobility.

Next, we examined the effect of varying Sn concentrations on the performance of 2D ITO TFTs. By maintaining printing temperature at 160 °C and varying Sn concentration from 10% to

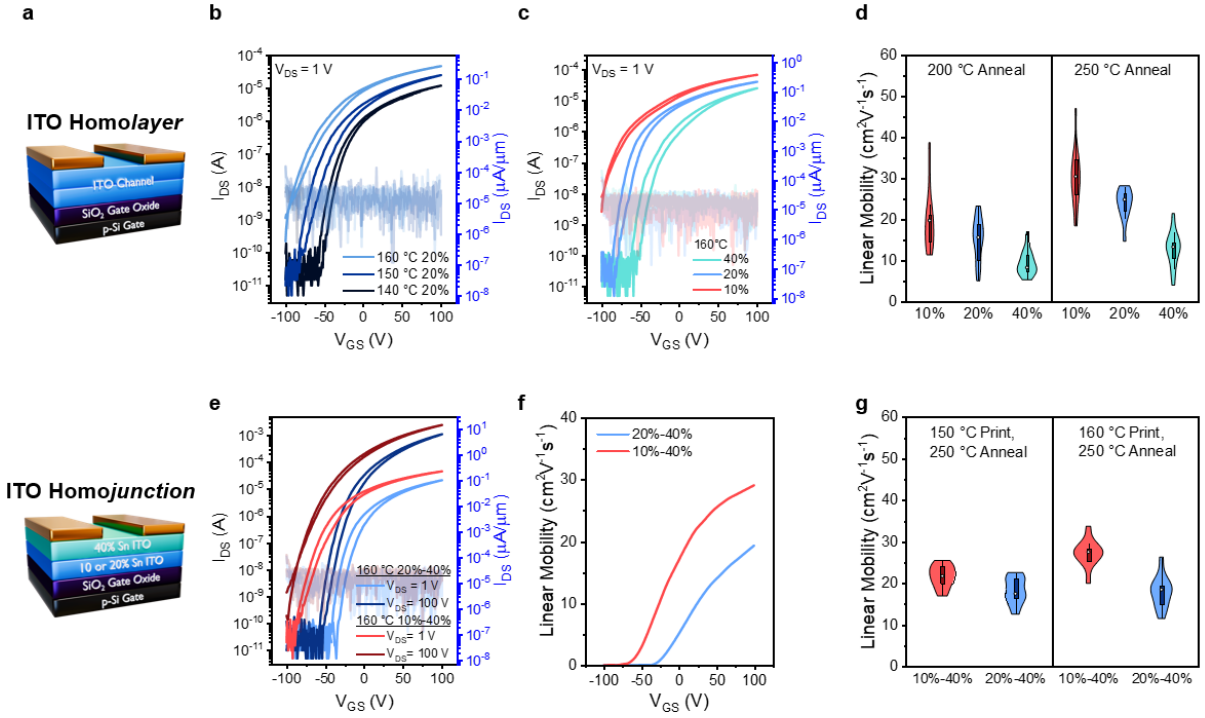

Figure 3: a) TFT bottom-gate structure using a homolayer as the channel and TFT bottom-gate structure using a homojunction as the channel. b) Transfer characteristics of homolayer 2D ITO (20% Sn) films at different printing temperatures after post-annealing at 250 °C. c) Transfer characteristics of homolayer 2D ITO films at 160 °C with different Sn% after post-annealing at 250 °C. d) Violin plot of mobility for 2D ITO films with different Sn concentrations after post-annealing at 200 °C and 250 °C. Violin shape using Kernel density estimation, central white dot is median, thick bar showing interquartile range, whiskers show 1.5×IQR, N =16 devices. e) Transfer characteristics of homojunction 2D ITO films after post-annealing at 250 °C. f) Incremental linear field effect mobility vs. gate voltage of homojunction 2D ITO after post-annealing at 250 °C, g) Violin plot of mobility for homojunction 2D ITO films printed at 150/160 °C. The channel length of all devices was 150 µm and the channel width of all devices was 200 µm.

40%, we observed positive shifts in the turn on voltage with increasing Sn (**Figure 3c** and **Table S2**). The 10 wt% Sn-doped ITO film, with a crystalline nature confirmed by **Figure S1**, exhibits a negative V_{on} and a high mobility of 30 ± 7 cm²/V·s (with a maximum of 47 cm²/V·s), matching well to our previous reports of crystalline InO_x and InO_x:Sb with mobility of 30 – 67 $cm^2/V{\cdot}s$.[3,16] With increased Sn incorporation up to 40%, the mobility decreases to 13 ± 4 cm²/V·s, while V_{on} and V_{th} shift closer to 0 V, indicating a lower carrier concentration. These trends are consistent with the XPS results discussed above, since 40% Sn films were determined to be the most oxygen rich. In addition, the violin plots shown in **Figure 3d** and the series of transfer characteristics for different Sn% 2D ITO TFTs post-annealed at 200/250 °C (**Figure S6, S7** and **S8**) display a narrower distribution for high Sn% conditions (20%, 40%), supporting the improved uniformity of the amorphous channel devices compared to the crystalline channels of 10% Sn-doped condition.

Post-annealing activation of amorphous 2D ITO generally results in more uniform characteristics and helps to achieve a turn-on voltage near 0 V for enhancement mode operation. We observe an interesting distinction in the transition from as deposited to post-annealed behavior of heavier Sn-doped (40 wt%) ITO vs. 20 wt% Sn ITO (**Figure S9**). Lower Sn concentrations are degenerate as deposited and after post-annealing can be gated effectively, while 40 wt% Sn conditions are typically inactive or have low currents as deposited but then exhibit significant increases in their mobility after post-annealing. This improvement can be attributed to changes in chemical bonding and structural relaxation induced by the thermal treatment.[26–28] Specifically, the O 1s XPS analysis shown in **Figure 2b**, **Figure S10** and **Table S1** reveals that, for the low Sn% film, excess charge carriers from oxygen vacancies dominate the as-deposited state, with a high M–O–Vac component of 24%. Post-annealing reduces the oxygen vacancy content to 18%. For the high Sn% film, the as-deposited films are highly sub-stoichiometric, as indicated by a low M–O–M component of 39%, which improves significantly to 78% after annealing. These chemical and structural modifications not only enhance electrical performance but may also improve the film's radiation hardness, as the high plasticity associated with the amorphous structure helps absorb radiation-induced defects, suggesting potential advantages for radiation-tolerant flexible electronic applications. [29,30] Remarkably, **Figures S6–S8** show that the widely dispersed series of transfer characteristics observed after post-annealing at 200°C become tightly distributed following annealing at 250°C, indicating that higher-temperature post-annealing significantly improves device uniformity.

Homojunction devices offer an opportunity to combine the relative advantages of both low Sn and high Sn 2D ITO layers. We investigated two types of homojunctions, 10%/40% and 20%/40%, as shown in **Figures 3e**, **3f**, and **Table 1**. For the 10%/40% 2D ITO, due to the crystalline front channel with 10% Sn, the average mobility is 27 ± 3 cm²/V·s (maximum 34 cm²/V·s), slightly lower than the 10%/10% homolayer, while V_{on} and V_{th} shift more positively to –86 V and –2 V. In the case of the 20%/40% 2D ITO, the mobility is 18 ± 4 cm²/V·s (maximum 26 cm²/V·s), with V_{on}

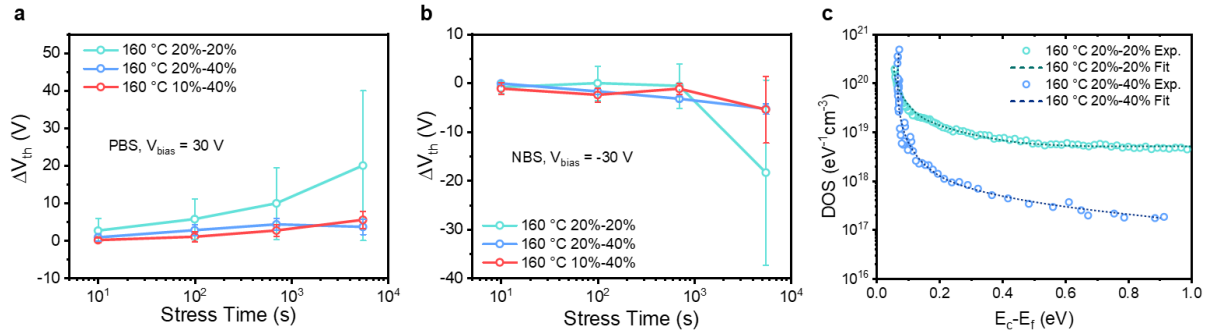

***Figure 4**: Threshold voltage shifts for a) positive bias stress (PBS, V_{ds} = 1 V, V_{gs} = 30 V, 5500s) and b) negative bias stress (NBS, V_{ds} = 1 V, V_{gs} = -30 V, 5500s). Extracted electronic density of state for homolayer 20%/20% and homojunction 20%/40% channel layers.*

and V_{th} shifting further positively to –45 V and 22 V. These shifts in each case highlight a potentially stabilizing effect of the 40% Sn back channel. With the stabilization provided by the 40% Sn back channel, the violin plots for both types of homojunctions also exhibit tighter distributions, perhaps also due to the role of the high Sn-layer in passivating surface defects. Multiple independent device batches yield similar results in terms of mobility, on/off ratio, and threshold / turn on voltage for homojunction devices. **Table S4** shows this comparison, for example, of one batch with linear mobility of 19.4 ± 3.7 $cm^2/V{\cdot}s$ vs. another batch having linear mobility of 21.1 ± 5.0 $cm^2/V{\cdot}s$, illustrating the repeatability of the liquid metal synthesis process as well as the consistent device yield.

Positive and negative bias stress tests comparing the homolayer and homojunction structures were conducted (**Figures 5a**, **b** and **Table S5**) to understand the influence of this channel architecture on operational stability and to consider the influence of a crystalline front channel on stability. Under positive bias stress (PBS, V_{gs} = 30 V, V_{ds} = 1 V) and negative bias stress (NBS, V_{gs} = –30 V, V_{ds} = 1 V) up to 5500 s, the ΔV_{th} for the 20%/20% homolayer device is a more severe 26 V (PBS) and –18 V (NBS) as shown in **Figure 4a, b** and **Table S5**. In contrast, the ΔV_{th} shifts for the 20%/40% and 10%/40% homojunctions are significantly lower: 3 V and –5 V for the 20%/40%, and 6 V and –5 V for the 10%/40%, showing that the amorphous/amorphous homojunctions had slightly better stability than the crystalline/amorphous condition. Given the

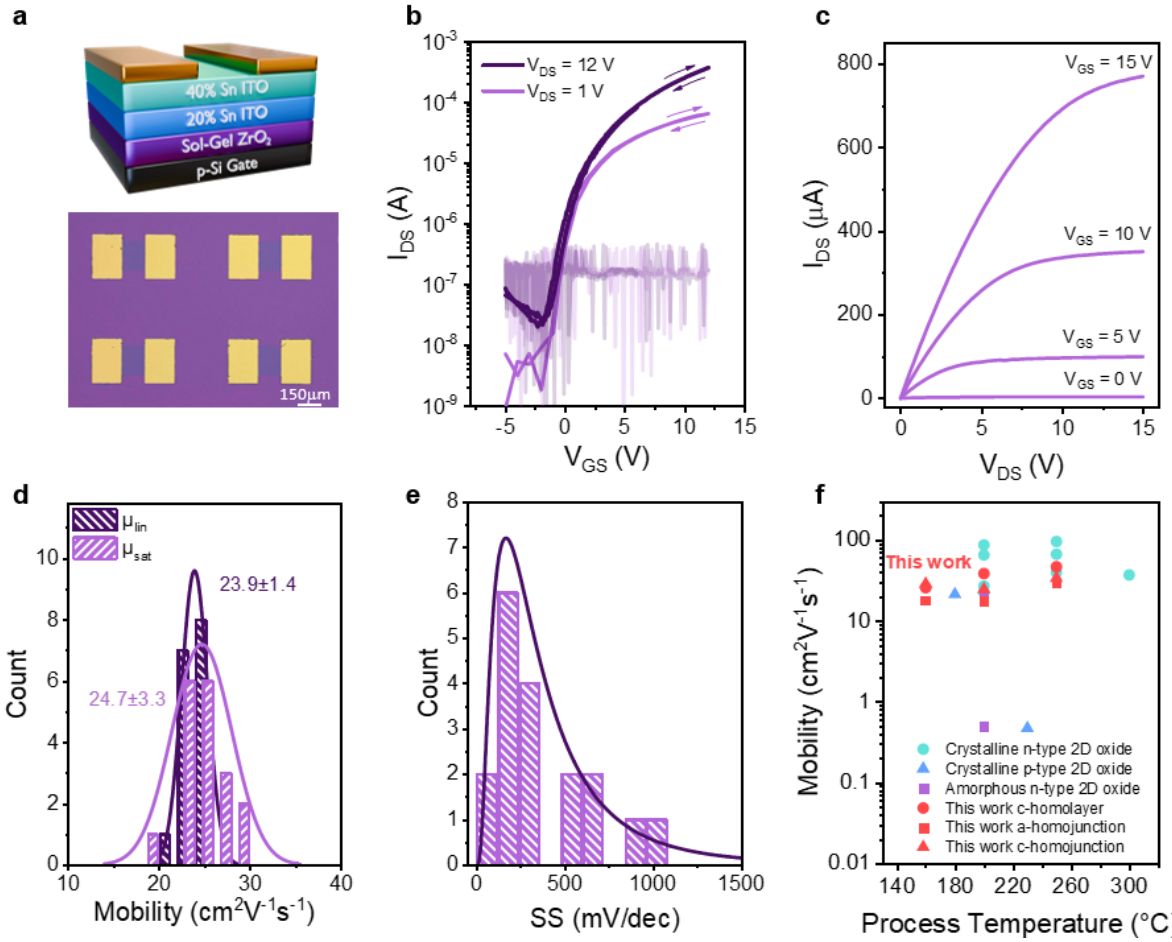

Figure 5*: a) Bottom-gate TFT structure and optical image of devices using solution-processed ZrO_x. b) Transfer, c) output characteristics, d) mobility histogram, and e) subthreshold swing histogram for homojunction 2D ITO (20%/40% Sn) devices. f) A comparison of the linear mobility of printed transistors in this study against other liquid metal printed 2D oxide tranistors reported in literature. Cyan and blue conditions show the crystalline 2D oxide performance reported while purple conditions show amorphous 2D oxide device performance. The values for this study at 250 °C, 200 °C, and 160 °C are presented in **Table S2**, **Table S6**, and **Table S7**, respectively. Literature values are provided in **Table S8** for comparison.* The channel length of all devices was 150 μm and the channel width of all devices was 200 μm.

ultrathin nature (3–5 nm) of the front channel, its electrical properties are especially sensitive to defects and ambient conditions such as adsorbates and surface contamination, this homojunction demonstrate an excellent enhancement in bias stress stability. This behavior is attributed to the use of a high-mobility, bias-unstable oxide at the front channel, and a bias-stable, low-mobility oxide at the back channel that passivates and shields against ambient influences.[24] Interestingly, one origin of bias stress instability is attributed to CO-related impurities, which can only be desorbed at temperatures above 350 °C.[24] Despite our homojunction platform being processed at a maximum temperature of 250 °C—insufficient to remove these impurities—bias stress stability is still significantly improved, suggesting that the junction interface itself acts as a natural barrier.

To further clarify the enhancement in bias stress stability, the sub-gap electronic density of states (DOS) was extracted for the homolayer (20%/20%) and homojunction (20%/40%) devices using temperature-dependent transfer measurements (**Figure S11**). The DOS extraction shown in **Figure 5c** captures the combined contributions from the bulk channel and the front- and back-channel surfaces. The extracted density of states of both conditions can be modeled approximately as a bi-exponential distribution of localized states, as typically done for disordered semiconductors. These distributions can be deconvolved into a linear superposition of exponential "tail states" near the band edges and exponential "deep states" further into the bandgap (**Figure S12**). The comparable tail state densities and band tail slopes explain the high mobility of both the 20%/20% and 20%/40% devices printed at 150°C (**Figure 3d**, **3g**, and **Table 1**). Additionally, the roughly 20X reduction in deep state density for the homojunction device can explain the steeper switching and a lower subthreshold swing (SS) (**Table 1)**.

Finally, the 20%/40% homojunction was selected for integration with solution-processed high-k ZrO_x, achieving a balance of high mobility, V_{on} and V_{th} near 0 V, and outstanding bias stress stability (**Figure 5a**). This result, we note, is to our knowledge the first report of the integration of liquid metal printed 2D oxide semiconductors with solution-processed high-k gate dielectrics, a key step towards achieving low-power flexible electronics. **Figures 5b** and **5c** show the champion transfer and output characteristics of the 20%/40% homojunction TFTs, exhibiting a mobility of 29.9 $cm^2/V{\cdot}s$, V_{on} of –4.9 V, and a V_{th} of 1.9 V. The outstanding SS as low as 100 mV/dec and a remarkably small hysteresis both indicate the compatibility between liquid metal printed semiconductors and sol-gel high-k dielectrics such as ZrO_x (**Figure S13**). We observe that using the high-k ZrO_x dielectric, the mobility is improved from 18 ± 4 $cm^2/V{\cdot}s$ (maximum 26 $cm^2/V{\cdot}s$) to 24.7 ± 3.3 $cm^2/V{\cdot}s$ (maximum 29.9 $cm^2/V{\cdot}s$). This difference could likely be due to the larger

effective transverse field in the channel for devices on ZrO_x since the devices on 300 nm SiO_2 dielectrics could not be biased to reach their peak transconductance.

Figures 5d, **5e**, and **Figures S14** further illustrate a tightly distributed histogram of linear and saturation mobility and SS values, as well as highly uniform transfer characteristics across 20 devices. It should be noted that most studies relying on crystalline high-mobility phases often suffer from brittleness, poor bias stress stability, and low device uniformity. **Figure 5f** presents the mobility achieved in this study in the context of maximum processing temperature and structural state reported for 2D printed oxide in the literature (**Table S8**)[35-41]. While crystalline 2D oxides can demonstrate higher mobility (e.g., crystalline In_2O_3 achieving 96 $cm^2/V{\cdot}s$ at 250°C but with a low on/off ratio of 10^4), our work achieves a high mobility of 33.7 $cm^2/V{\cdot}s$ for crystalline homojunctions and 29.9 $cm^2/V{\cdot}s$ for amorphous homojunctions at 250°C with much higher on/off ratio of 10^7, negligible hysteresis when combine with sol-gel ZrO_x and high uniformity. At just 200°C (shown in **Table S6**), we achieved mobilities of 24.5 $cm^2/V{\cdot}s$ (crystalline) and 17.4 $cm^2/V{\cdot}s$ (amorphous); at 160°C (**Table S6**), 28.64 $cm^2/V{\cdot}s$ (crystalline) and 17.9 $cm^2/V{\cdot}s$ (amorphous). Although the peak mobility values achieved in this study are lower than those reported for some crystalline 2D oxides, our homojunction devices exhibit superior bias stress stability, low hysteresis, a high on/off ratio, and excellent potential for mechanical flexibility due to their ultrathin and amorphous nature—offering significant advantages for circuit integration.

Furthermore, the compatibility with large-area, low-cost continuous liquid metal printing highlights additional benefits compared to vacuum-processed oxides, which typically require expensive equipment and suffer from low throughput. Additionally, our 2D ITO printing method is solvent-free, enabling the achievement of high electron mobility (> 30 $cm^2/V{\cdot}s$) at a relatively low processing temperature of 250°C. In comparison, sol-gel-derived ITO typically exhibits lower mobility values ranging from 10 to 20 $cm^2/V{\cdot}s$ at this range of annealing temperatures[31] while higher performance in the range of 40 $cm^2/V{\cdot}s$ requires significantly higher, non-plastic-compatible annealing temperatures up to 400°C[32]. Similarly, we can benchmark liquid metal printed 2D amorphous oxides against ALD and sputtered ultrathin oxide semiconductors based on InO_x[33], which achieve outstanding on-state performance ($I_{D,max}$ ~ 1 – 10 mA/μm) and SS of 100 mV or lower but generally require 300 - 400 °C annealing. The comparable linear mobility in this work suggests the potential liquid metal printing to bring high-performance to flexible electronic devices on plastic substrates or to applications in back-end-of-line (BEOL) vertical integration with CMOS

integrated circuits. The self-limiting Cabrera Mott growth mechanism could enable sub-nm control[16] for growing larger, uniform wafer-scale arrays suitable for applications such as oxide-transistor based monolithic 3D-integrated memory[34]. Finally, to demonstrate the compatibility of our approach with flexible devices, we have integrated the 2D homojunction ITO channels on an ultrathin polyimide substrate with a top-gate architecture (**Figure S15a**). A set of typical TFT transfer and output characteristics (**Figure S15b, c**) of the 20%/40% homojunction ITO fabricated at 160°C show its strong potential for flexible applications.

3. Conclusion

In summary, we have demonstrated a strategy for controlling the amorphous vs. crystalline phase of liquid metal printed 2D oxide semiconductors, revealing the potential for printing high performance oxide materials at ultralow temperatures near the eutectic point of indium-tin alloys (~118°C). Sn-rich alloys control the free-carrier concentration and allow nanoscale vertical homojunctions with graded composition spanning crystalline and amorphous phases in the same film. Sn-rich amorphous homojunctions of ITO optimize the balance between mobility and switching behavior while improving subthreshold swing and hysteresis, leveraging the high DOS front-channel and a low DOS back-channel. Printed TFT devices incorporating solution-processed ZrO_x dielectrics are demonstrated for amorphous 20%/40% 2D ITO homojunctions, producing ultra-steep subthreshold slope and negligible hysteresis. These impressive device performances, combined with the facile, high-throughput, large-area CLMP method, demonstrate that this approach could be a promising strategy for scalable fabrication of next-generation flexible electronics.

4. Experimental Section

Precursor Alloy Preparation

Hypoeutectic In–Sn alloys were synthesized by melting indium (In, 99.995%, Luciteria) and tin (Sn, 99.99%, Luciteria) in a glass vial at 200°C for 10 minutes under an inert nitrogen atmosphere inside a glovebox to minimize surface oxidation. Alloys with 10, 20, and 40 wt% Sn were prepared by direct weighing then mixed by stirring with a glass tube when melt with above condition.

Continuous Liquid Metal 2D Oxide Printing (CLMP)

The 2D metal oxide films were prepared by rolling a droplet of liquid metal alloy across 3 × 7 cm substrates using a silicone roller at a speed of approximately 5 cm/s on a hot plate set to 140, 150,

or 160 °C. Before deposition, the substrates underwent surface activation using atmospheric plasma treatment for 30 seconds (Plasma Etch system, 1000 W, 30 LPM compressed dry air) to enhance film adhesion. For multilayer printing, each intermediate layer received a brief 2 s plasma exposure to improve interlayer bonding. The transient effects of the plasma treatment are reported in Figure S16, showing that thermal post-annealing heals defects induced by plasma surface treatment. To ensure continuous and uniform film coverage, the target substrate was positioned between two sacrificial substrates of the same dimensions, which served as buffer zones at the start and end of the rolling path. The silicone roller was preconditioned by rolling it over a clean 300 nm SiO_2/Si substrate for 1 minute prior to printing. After deposition, residual liquid metal on the oxide film surface was cleaned using isopropyl alcohol (IPA), first while the sample remained heated, and again after cooling to room temperature.

Device Fabrication

Thin-film transistors were fabricated using CLMP layered metal oxide films on 300 nm SiO_2/Si substrates, following standard photolithography and wet etching techniques. The channel length of all devices was 150 μm and the width of all devices was 200 μm. The active regions of ITO were patterned to dimensions of 400 μm x 200 μm. For 2D ITO channels, wet etching was performed using 18% HCl for 30 seconds. Source and drain electrodes were formed by sputtering approximately 30 nm of Au and were patterned via a lift-off process. Then the final devices were post-annealed at 200/250˚C (either 1, 2, or 24 hr) to enhance performance.

For low-voltage operation, ~60 nm-thick ZrO_2 gate dielectrics were deposited onto heavily doped p-type silicon substrates. This was achieved by spin-coating a 0.2 M solution of $ZrOCl_2$ (reagent grade, 98%, Sigma-Aldrich) in 2-methoxyethanol at 3000 rpm for 40 s, followed by a soft bake at 150 °C for 5 min. This coating and baking cycle were repeated four times. The films were then post-annealed at 300 °C in ambient air for 2 hr. To further enhance dielectric performance, the samples were soaked in hot deionized water at approximately 85 ˚C for 30 min. Then, the next step for channel layer to finish the TFT device is the same as described above. Metal–insulator–metal (MIM) structures for gate capacitance measurements were prepared on the same substrate configuration using circular gold pads (area ≈ 0.2 mm^2) deposited via sputtering. Frequency-dependent capacitance was measured using a Hiroki IM3570 LCR meter over the range of 100 Hz to 1 MHz.

For flexible devices, top gate architectures were employed as described in Figure S15a. First, polyimide (PI2545, HD MicroSystems™) was spin-coated on an SiO_2 /Si wafer at 5000 rpm

for 80 s. The film was soft-baked at 140 °C for 5 min, followed by a gradual temperature ramp to 200 °C at a rate of 4 °C/min, and held at 200 °C for 30 min. Subsequently, the sample was annealed in an inert atmosphere at 200 °C for 5 min, then the temperature was gradually increased to 350 °C at a rate of 4 °C/min and maintained for 1 hr. Next, the 2D metal oxide was printed under the previously described conditions, but with the homojunction order reversed to align with the top-gate structure. Then, the channel was patterned via photolithography and wet etching as mentioned above and Cr/Au (5 nm/ 30 nm) S/D was deposited and patterned by lift-off. Another PI2545 layer was used for the dielectric but was spin coated at 8000 rpm, resulting in a dielectric of thickness approximately 800 nm (confirmed by stylus profilometer). The gate dielectric annealing process was similar to that of the bottom substate layer but the temperature in the inert atmosphere step was only 250°C. Finally, the Au top-gate electrode was deposited by sputtering and patterned using a lift-off process to complete the top-gate TFT structure. The entire device was then released from the SiO_2 / Si substrate by mechanically detaching it from the rigid bottom substrate. The whole device structure consisting of the flexible PI substrate is shown in Figure S5a.

Materials Characterization

X-ray diffraction (XRD) analysis was conducted on three-layer films deposited on silicon wafers coated with a 300 nm thermally grown SiO_2 layer. The measurements were carried out using a Rigaku Miniflex diffractometer equipped with Cu Kα radiation, operated at a scanning rate of 10˚ per minute. Transmission electron microscopy (TEM) was employed to characterize the 2D ITO films using a FEI Tecnai F20 microscope, operated at an accelerating voltage of 200 kV. For TEM observation, the 2D ITO films were directly printed onto carbon type-B 2000-mesh copper grids (Ted Pella) via the CLMP printing technique.

X-ray photoelectron spectroscopy (XPS) measurements were carried out using a Kratos Axis Supra instrument under ultra-high vacuum conditions (~10^{-9} Torr) on metal oxide films comprising four printed layers deposited on silicon substrates with a 300 nm SiO_2 layer. Optical absorbance spectra of the 2D ITO films were obtained using a Cary 60 UV-Vis spectrophotometer, scanning in the range of 200–800 nm with samples printed on borosilicate glass substrates. Surface morphology of the printed films was analyzed using an AIST-NT atomic force microscope (AFM). Optical images were captured using a Keyence VHX-7100 digital microscope. Film thicknesses were determined using Filmetrics (F3-sX) spectral reflectometers to measure oxide layers printed over 300 nm SiO_2/Si substrates. Automated thickness measurement of printed ITO films for thickness measurements was characterized using spectroscopic reflectometry in the 380–1050 nm range,

integrated with an automated gantry system (Genmitsu). The gantry was controlled via GrblControl and Microsoft Power Automate to scan the reflectometry probe across the sample with a 1 mm spatial resolution (**Figure S2**). Before film measurements, the SiO_2 layer thickness was determined to enable accurate modeling of the reflectance spectra and extraction of the 2D ITO film thickness. Alpha-Step® D-500 Stylus Profiler from KLA is used to measure thickness of PI2545 dielectric layer with scan speed of 0.15 mm/sec, scan range up to 10 μm and stylus force of 0.1 mg

Electrical Measurements

Thin-film transistor measurements, including both transfer and output characteristics, were performed in ambient conditions at room temperature using an Agilent E5260A semiconductor parameter analyzer. The electronic density of states (DOS) was determined from temperature-dependent transfer measurements taken in the linear regime under 1 V drain voltage, across a temperature range from room temperature up to approximately 100 °C. Extraction of the DOS was based on fitting an activation energy as a function of gate voltage, following the approach described by Zeumault et al. [A. Zeumault, W. Scheideler, V. Subramanian, Adv. Funct. Mater. 2017, 27, 1701021.], using the multiple trap-and-release (MTR) model as a theoretical framework. Bias stress stability was also evaluated using the same analyzer after encapsulating the devices with a layer of polymethyl methacrylate (PMMA 950A4, *Microchem*).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supporting Information

2D Amorphous Homojunction Transistors Exfoliated from Liquid Metals

*Minh Nhut Le, Md Saifur Rahman, Simon A. Agnew, Samuel W. Ong, and William J. Scheideler**

Thayer School of Engineering
Dartmouth College, Hanover, NH 03755, United States
E-mail: william.j.scheideler@dartmouth.edu

Table S1: *Summary of XPS O1s peak fitting results of 2D ITO with different wt % Sn.*

Condition	Sample	M-O-M peak at 529.7 ± 0.1 eV (%)	M-O-Vac peak at 531.2 ± 0.1 eV (%)	M-O-H peak at 532.2 ± 0.1 eV (%)
As-fabricated	40 wt% Sn	39	35	26
	20 wt% Sn	52	24	24
	10 wt% Sn	67	20	13
200°C post-anneal	40 wt% Sn	78	12	10
	20 wt% Sn	73	18	9
	10 wt% Sn	71	19	10

Table S2: *Summary of 2D printed ITO TFT performance after 250 °C annealing. Champion values are indicated with parentheses. A total of 12 devices were characterized on SiO_2 for each condition, except where noted: *16 devices on SiO_2; **20 devices on solution-processed ZrO_x. The values presented in this table are average values ± standard deviation, except for I_{on}/I_{off}, for which only the average value is shown.*

Sample	Printing temperature (°C)	Number of Printed Layers	Linear Mobility ($cm^2/V \cdot s$)	V_{on} (V)	V_{th} (V)	Subthreshold Slope (V/dec)	I_{On}/I_{Off}
20%	140	3 layers	12±3.3 (15)	-65±6.0	17±7.0	4.4±0.9 (3.3)	$3.1 \cdot 10^6$
20%	150		18±2.2 (22)	-93±3.0	9.0±3.0	4.9±0.6 (4.0)	$4.3 \cdot 10^6$
20%	160		25±3.1 (30)	-100	-11±5.0	6.1±3.3 (3.5)	$1.0 \cdot 10^6$
20%-20%	150	2 layers	19±3.8 (23)	-70±8.0	7.0±10	4.6±0.6 (4.1)	$5.4 \cdot 10^6$
20%-40%			18±3.1 (23)	-59±6.0	18±4.0	4.1±0.9 (3.0)	$4.7 \cdot 10^6$
10%-40%			22±2.7 (26)	-79±7.0	10±8.0	4.7±0.7 (3.7)	$6.1 \cdot 10^6$
* 10%-10%	160	2 layers	30±7.0 (47)	-100	-27±25	14±21 (4.4)	$1.6 \cdot 10^5$
20%-20%			24±3.8 (28)	-84±5.0	-5.0±14	4.4±0.6 (3.5)	$6.8 \cdot 10^6$
*40%-40%			13±4.4 (21)	-71±15	-6.0±7.6	4.0±0.6 (3.0)	$4.8 \cdot 10^6$
10%-40%			27±3.3 (34)	-86±6.0	-2.0±3.0	4.3±0.7 (3.3)	$7.8 \cdot 10^6$
20%-40%			18±3.8(26)	-45±7.0	22±6.0	3.3±0.7 (2.4)	$4.5 \cdot 10^6$
**20%-40%(w/ ZrO_x)			24.7±3.30 (29.9)	-4.90±1.00	1.90±1.90	0.40±0.30 (0.10)	$6.5 \cdot 10^6$ ($2.68 \cdot 10^7$)

Table S3: *Summary of 2D ITO film thickness under various printing conditions. The films were post-annealed at 250°C for 30 minutes to avoid influence from metal residue.*

Sample	Printing temperature (°C)	Number of Printed Layers	Thickness (nm)
20%	140	3 layers	12.4±0.4
20%	150		12.8±0.1
20%	160		11.2±0.3
10%-10%	160	2 layers	6.4±0.2
20%-20%			7.6±0.3
40%-40%			6.6±0.2
10%-40%			6.9±0.6
20%-40%			7.1±0.2

Table S4: *Comparison of device statistics for 250 ℃ post-annealed 20/40% Sn homojunction devices fabricated in two independent device batches. All 50/50 devices measured from Batch 2 met a yield criteria of a mobility > 10 cm^2/Vs and an I_{on}/I_{off} ratio > 10^3.*

	μ_{lin}	V_{on}	V_{th}	SS	I_{On}/I_{Off}
Batch 1 *(18 devices)*	*19.4±3.7*	*-61.3±6.2*	*12.6±6.2*	*4.8±1.1*	*$5.2 \cdot 10^6$*
Batch 2 *(50 devices)*	*21.1±5.0*	*-56.4 ± 18.0*	*20.2 ± 15.9*	*4.3±0.8*	*$6.7 \cdot 10^6$*

Table S5: *Summarized parameter of bias stress measurement for homolayer and homojunction device after 250°C post-annealing. A total of 3 devices were characterized on SiO_2 for each condition. The values presented in this table are average values ± standard deviation.*

Printing temperature (°C)	Sample	PBS (30 V 5500s after PMMA) ΔV_{th}	NBS (-30 V 5500s after PMMA) ΔV_{th}
160	20%-20%	26±31	-18±19
	20%-40%	2.8±2.6	-5.3±1.0
	10%-40%	5.6±2.8	-5.4±6.8

Table S6: *Summary of 2D printed ITO TFT performance after 200°C anneal. Champion values are indicated with parentheses. A total of 16 devices were characterized on SiO_2 for each condition. The values presented in this table are average values ± standard deviation, except for I_{on}/I_{off}, for which only the average value is shown.*

Sample	Printing Temperature (°C)	Number of Printed Layers	Linear Mobility ($cm^2/V \cdot s$)	V_{on} (V)	V_{th} (V)	Subthreshold Slope (V/dec)	I_{On}/I_{Off}
20%	140	3 layers	8.8±1.1 (11)	-58±11	28±8.8	5.2±0.9 (4.1)	$2.2 \cdot 10^6$
20%	150		11±1.9 (15)	-80±9.2	18±8.7	5.3±0.9 (4.0)	$2.3 \cdot 10^6$
20%	160		12±1.8 (14)	-59±37	23±4.8	6.0±1.1 (4.4)	$2.6 \cdot 10^6$
20%-20%	150	2 layers	5.4±1.5 (7.7)	-38±14	63±8.8	5.7±0.9 (4.3)	$4.5 \cdot 10^6$
20%-40%			9.0±2.3 (12)	-43±10	44±8.2	5.1±0.9 (4.1)	$1.7 \cdot 10^6$
10%-40%			11±3.0 (15)	-58±14	39±11	5.1±0.8 (4.0)	$1.8 \cdot 10^6$
10%-10%	160	2 layers	20±7.3 (39)	-70±12	31±11	7.6±6.9 (4.4)	$3.9 \cdot 10^6$
20%-20%			15±5.2 (23)	-66±19	32±13	6.0±2.3 (3.4)	$5.9 \cdot 10^6$
40%-40%			9.4±3.0 (17)	-36±8.3	46±14	5.6±2.2 (4.4)	$2.2 \cdot 10^6$
10%-40%			19±3.7 (25)	-40±8.6	47±5.7	4.7±1.3 (3.2)	$1.9 \cdot 10^6$
20%-40%			13±2.1 (17)	-33±15	44±11	4.5±0.9 (3.6)	$3.3 \cdot 10^6$

Table S7: *Summary of as-fabricated ITO TFT performance. Champion values are indicated with parentheses. A total of 3 devices were characterized for each condition. Devices were substrate-gated with a 300 nm thermally-grown SiO_2 gate dielectric. The values presented in this table are average values ± standard deviation, except for I_{on}/I_{off}, for which only the average values are shown.*

Sample	Printing temperature (°C)	Number of Printed Layers	Linear Mobility ($cm^2/V \cdot s$)	I_{On}/I_{Off}
20%	140	3 layers	2.5±0.5 (3.0)	7.5
20%	150		6.9±1.4 (8.3)	4.6
20%	160		5.1±0.2 (5.3)	1.5
20%-20%	150	2 layers	3.5±0.1 (3.6)	20
20%-40%			6.3±2.3 (8.6)	$1.6 \cdot 10^3$
10%-40%			13±0.6 (14)	$1.3 \cdot 10^2$
20%-20%	160	2 layers	23±1.9 (26)	5.2
20%-40%			16±1.2 (17)	29
10%-40%			25±4.4 (30)	4.0
40%-40%			0.14±0.03 (0.18)	$2.0 \cdot 10^4$
10%-10%			13±4.9 (18)	1.5

Table S8: *Summary of other 2D oxide printed TFT for benchmark comparison.*

Reference	DOI	Material	Carrier type	Structural nature	Printing temperature (°C)	Post-annealing Temperature (°C)	Mobility ($cm^2/V·s$)
[4]	10.1002/admi.202202036	In_2O_3	n	c	250°C	250°C 2h	96
[3]	10.1038/s41699-022-00294-9	In_2O_3	n	c	165°C	250°C 1h	67
[17]	10.1021/acsnano.1c11205	ITO	n	c	200°C	200°C	27
[35]	10.1002/admi.201900007	SnO (bottom)/In_2O_3 (top)	n	c	300°C for Sn, 200°C for In	/	37
[36]	10.1002/adom.202200925	IAO	n	c	250°C	/	40
[20]	10.1021/acsnano.0c06791	IZO	n	c	200°C	/	87
[37]	10.1021/acs.nanolett.2c04555	InO_x/GaO_x	n	c	200°C	/	22.6
[38]	10.1021/acsaelm.3c00127	GaInSnO	n	c	200°C	/	65.4
[39]	10.1021/acsami.1c15990	SnO	p	c	230°C	/	0.47
[40]	10.1002/pssr.201900271	Beta-Ga_2O_3	p	c	180°C	/	21.3
[41]	10.1039/d2nr04535d	IZTO	n	a	200°C	/	0.5
[42]	10.1039/d4tc02312a	IZO/Ga_2O_3	n	a	200°C	/	20.79

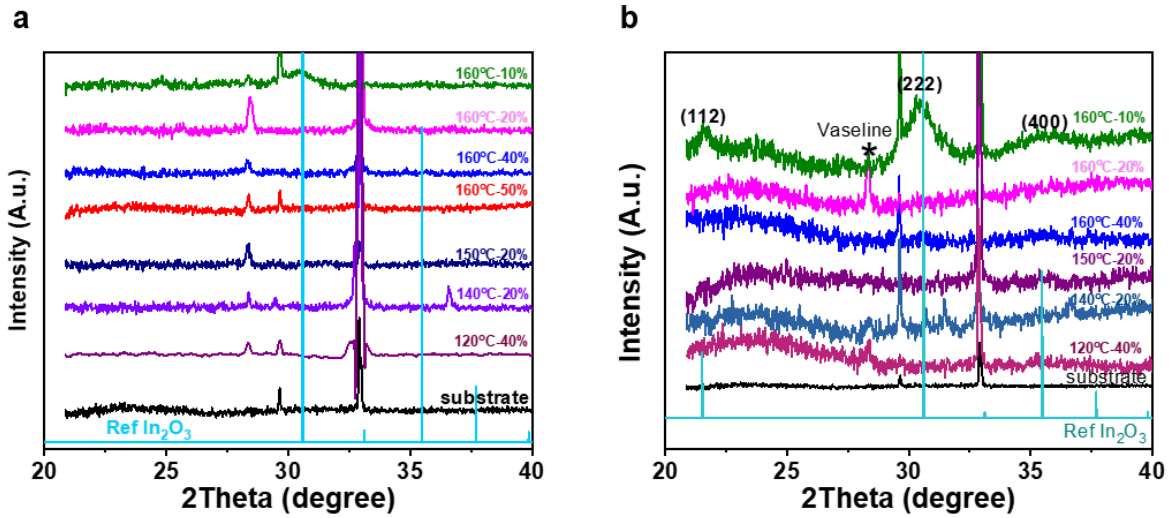


Figure S1. XRD pattern of series of 2D ITO with variation of temperature and Sn% a) as-fabricated and b) after 250 °C post-annealing.

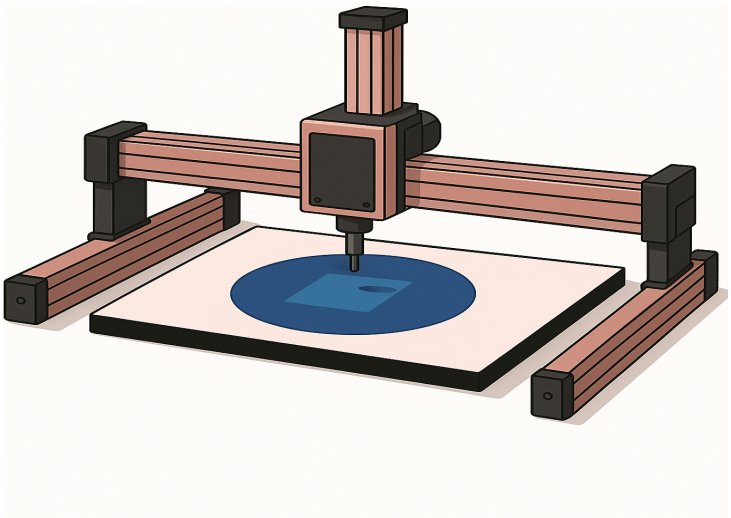


Figure S2. Schematic of the robotic reflectometry setup used for film thickness mapping. The reflectometer probe is mounted on a Genmitsu system and controlled via GrblControl and Microsoft Power Automate, enabling automatically measurements at 1 mm intervals.

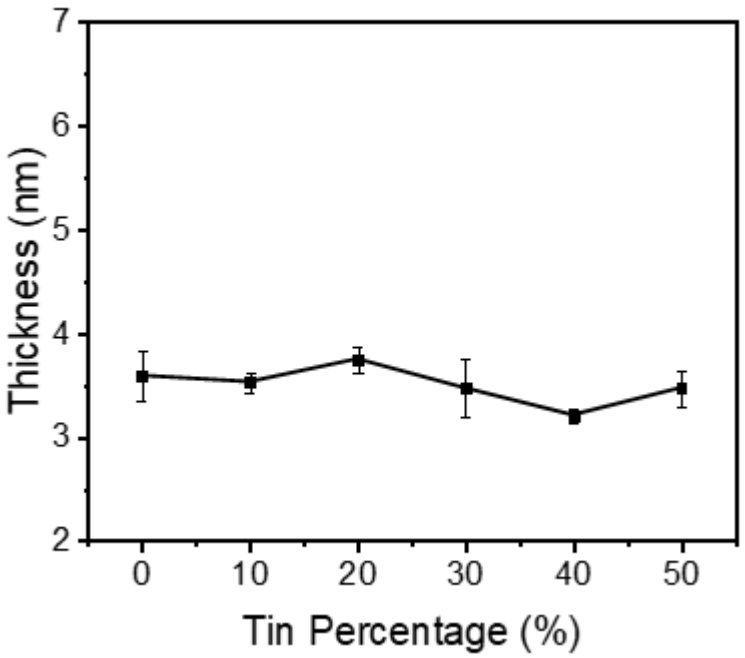


Figure S3. Measured thickness of 2D ITO films as a function of Sn content (wt% in the precursor metal alloy) printed under identical conditions. All films were post-annealed at 250 °C for 30 min to eliminate potential influence from residual metal. Before 2D oxide thickness measurements, the SiO_2 thickness was also measured to allow the utilization of a two layer spectral reflectance model. Thickness values represent the average of six measurement points, with error bars indicating the standard deviation. At each point, normal-incidence reflectivity was measured and fitted to an optical model based on the Fresnel equations, using known refractive indices of the film and substrate. The local film thickness was extracted by matching the experimental data to the simulated reflectivity profile. To ensure high accuracy, only data points with a goodness of fit (GoF) greater than 0.995 were included in the final analysis. Error bars shown in this plot are equal to one standard deviation.

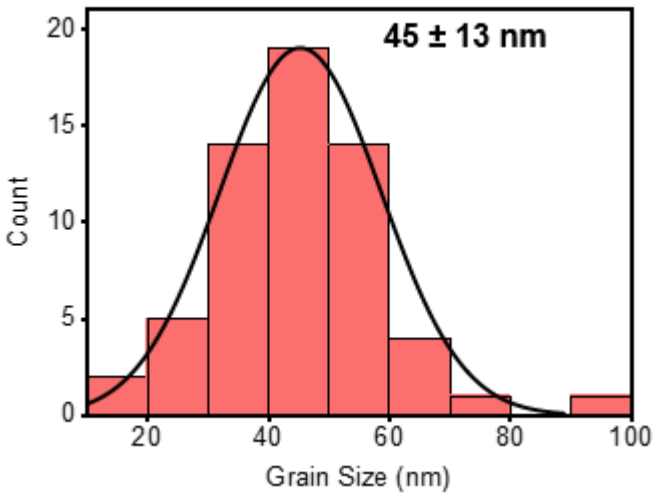
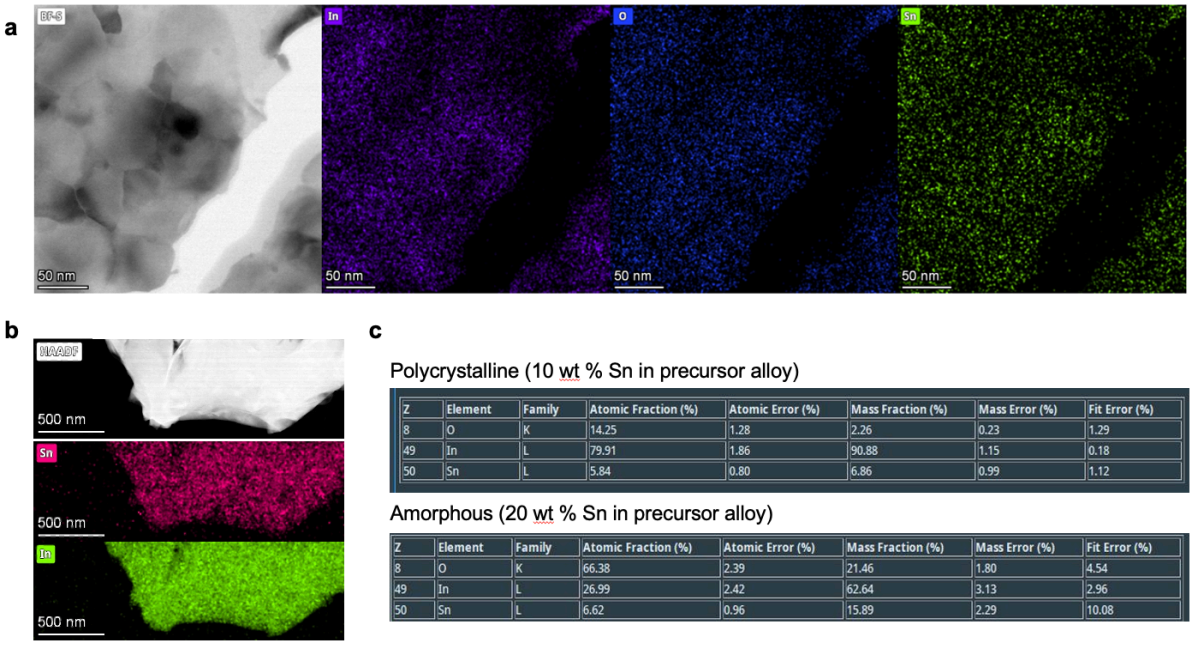


Figure S4. Grain size histogram of 2D ITO (7.5% Sn) printed 170 °C with 0.5 cm/s speed as extracted from the AFM scan shown in Figure 1. Annotation shows the average grain size plus / minus a single standard deviation.



Polycrystalline (10 wt % Sn in precursor alloy)

Z	Element	Family	Atomic Fraction (%)	Atomic Error (%)	Mass Fraction (%)	Mass Error (%)	Fit Error (%)
8	O	K	14.25	1.28	2.26	0.23	1.29
49	In	L	79.91	1.86	90.88	1.15	0.18
50	Sn	L	5.84	0.80	6.86	0.99	1.12

Amorphous (20 wt % Sn in precursor alloy)

Z	Element	Family	Atomic Fraction (%)	Atomic Error (%)	Mass Fraction (%)	Mass Error (%)	Fit Error (%)
8	O	K	66.38	2.39	21.46	1.80	4.54
49	In	L	26.99	2.42	62.64	3.13	2.96
50	Sn	L	6.62	0.96	15.89	2.29	10.08

Figure S5. (a) Bright-field STEM image (left) and corresponding EDS elemental maps of In (purple), O (blue), and Sn (green) for the 2D crystalline 10% Sn ITO sample printed at 160°C after 250 °C post-annealing for 1 hour. (b) HAADF TEM showing In (green) and Sn (pink) for amorphous ITO (20 wt% Sn precursor alloy) post-annealed at 250 °C for 1 hr. (c) Table summarizing stoichiometry for polycrystalline (10 wt% Sn) and amorphous (20 wt% Sn) samples measured via EDS.

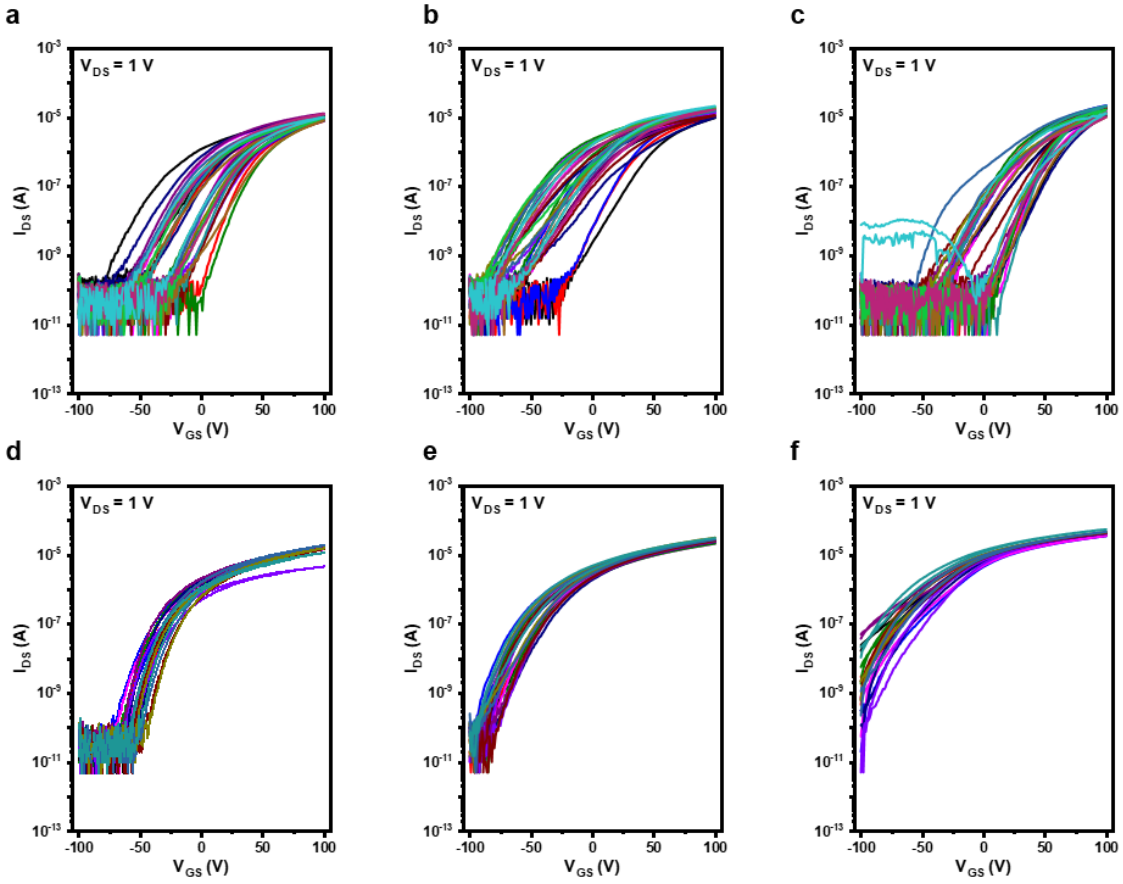


Figure S6. Series of transfer characteristic of 2D ITO film post-annealed at 200˚C for a) 140˚C printed 3 layer 20% Sn channels, b) 150˚C printed 3 layer 20% Sn channels, c) 160˚C printed 3 layer 20% Sn channels, Series of transfer characteristic of 2D ITO devices post-annealed at 250˚C and PMMA encapsulated for d) 140˚C printed 3 layer 20% Sn channels, e) 150˚C printed 3 layer 20% Sn channels, and f) 160˚C printed 3 layer 20% Sn channels.

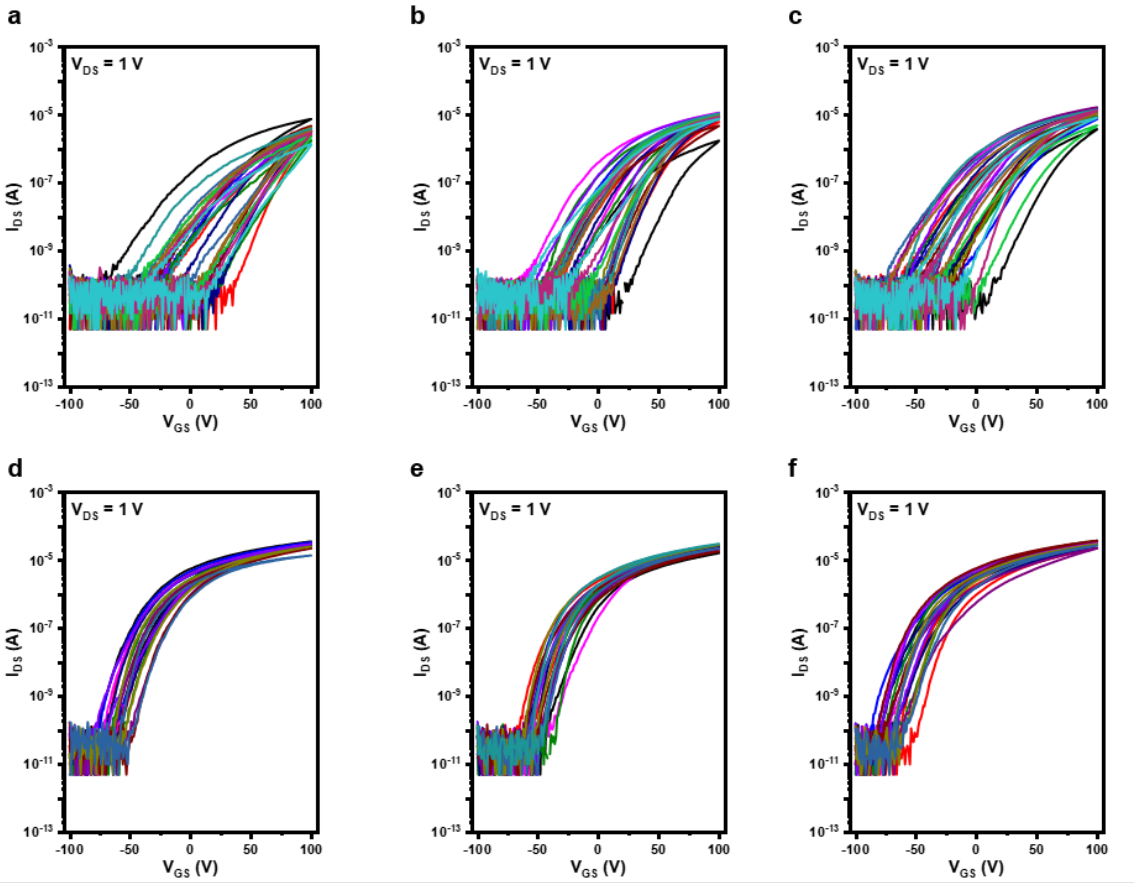


Figure S7. Series of transfer characteristic of 2D ITO devices post-annealed at 200°C for a) 150°C printed 2 layer 20%/20% Sn channels, b) 150°C printed 2 layer 20%/40% Sn channels, c) 150°C printed 2 layer 10%/40% Sn channels. Series of transfer characteristic of 2D ITO channels post-annealed at 250°C and PMMA encapsulated for d) 150°C printed 2 layer 20%/20% Sn channels, e) 150°C printed 2 layer 20%/40% Sn channels, f) 150°C printed 2 layer 10%/40% Sn channels.

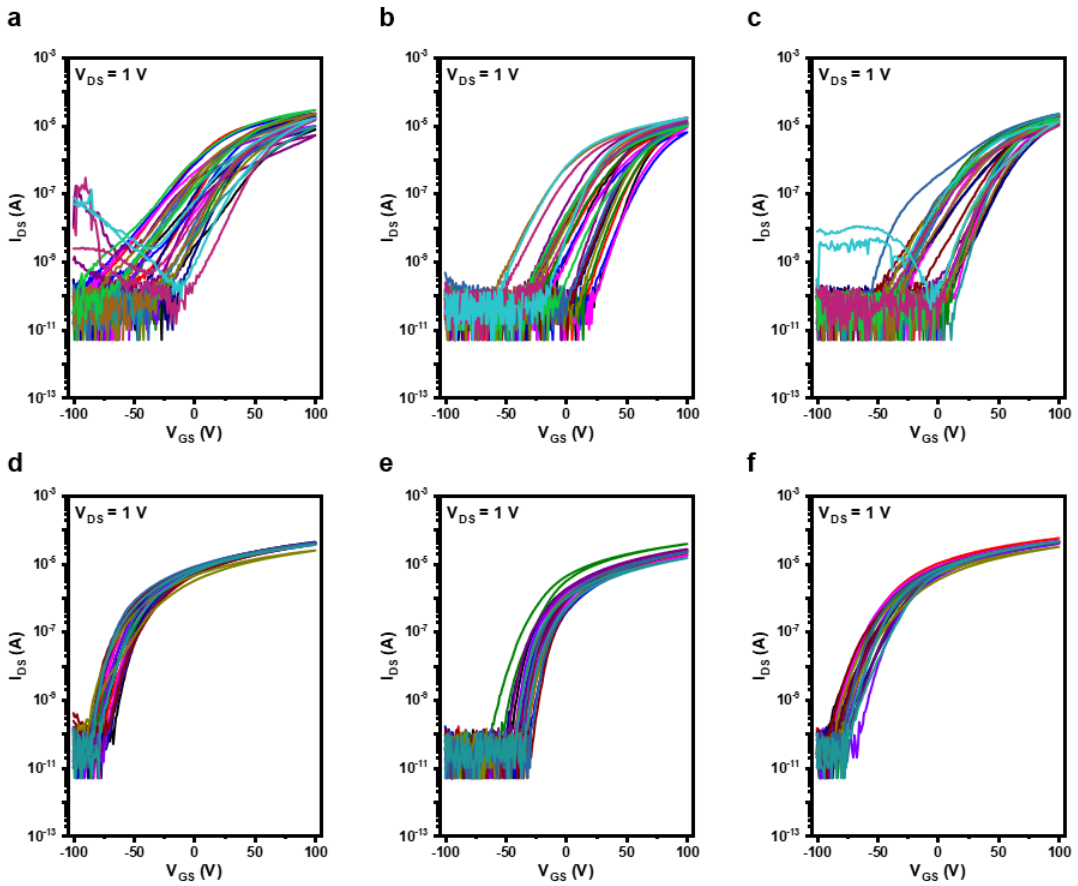


Figure S8. Series of transfer characteristic of 2D ITO film post-anneal at 200˚C for a) 160˚C printed 2 layer 20%/20% Sn channels, b) 160˚C printed 2 layer 20%/40% Sn channels, c) 160˚C printed 2 layers 10%/40% Sn. Series of transfer characteristic of 2D ITO channels post-annealed at 250˚C and PMMA encapsulated for d) 160˚C printed 2 layer 20%/20% Sn channels, e) 160 ˚C printed 2 layer 20%/40% Sn channels, f) 160˚C printed 2 layer 10%/40% Sn channels.

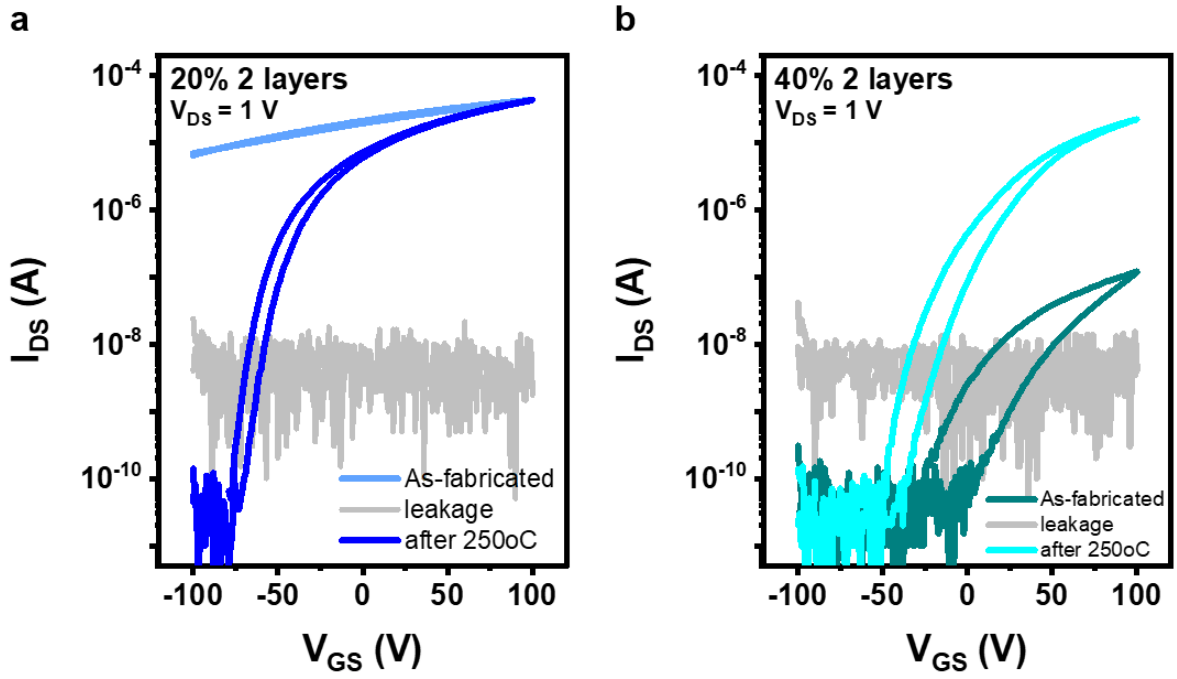


Figure S9. Transfer characteristic of as fabricated and after post-annealing at 250°C 2D oxide films for a) 20% Sn 2D ITO and b) 40% Sn 2D ITO printed at 150 °C.

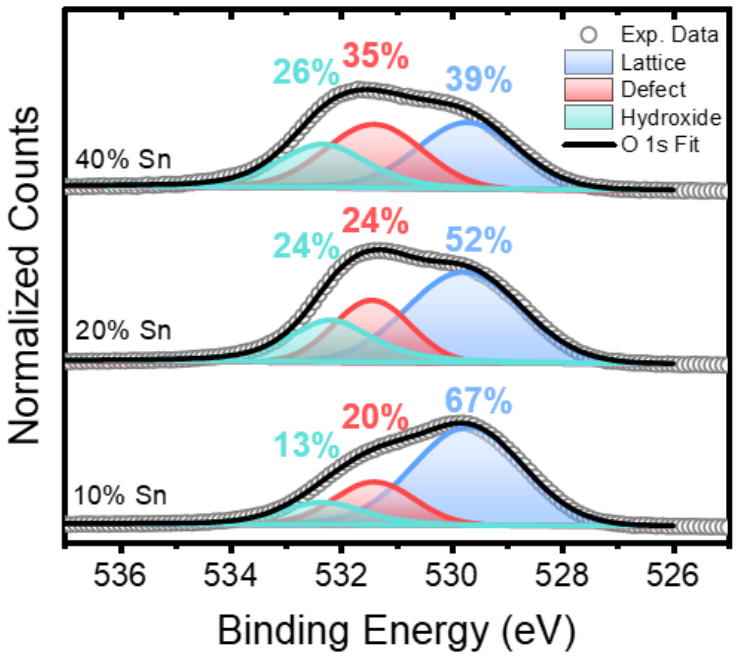


Figure S10. XPS O1s study of as-fabricated 10, 20, 40% Sn 2D oxide films.

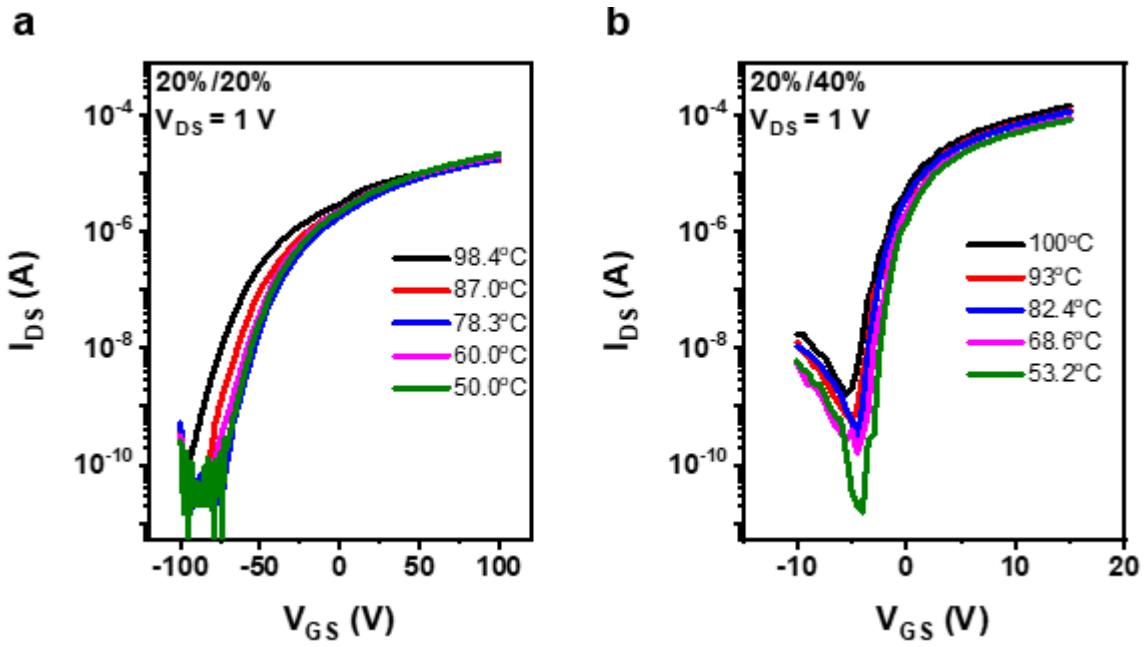


Figure S11. Temperature-dependent transfer characteristics measurements of a) 2 layer homolayer 2D ITO 20%/20% and b) homojunction 2D ITO 20%/40% printed at 160°C with speed of 0.5 cm/s after 250 °C post-annealed and PMMA encapsulation.

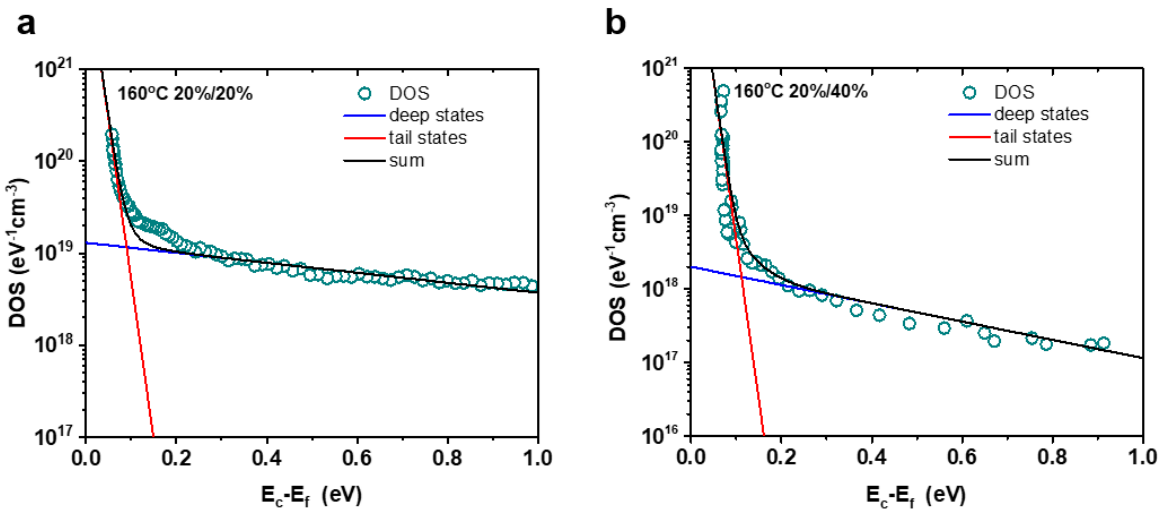


Figure S12: Biexponential DOS distribution fits for extracted DOS of a) homojunction 20%/20% Sn printed at 160°C and b) homojunction 20%/40% Sn printed at 160°C.

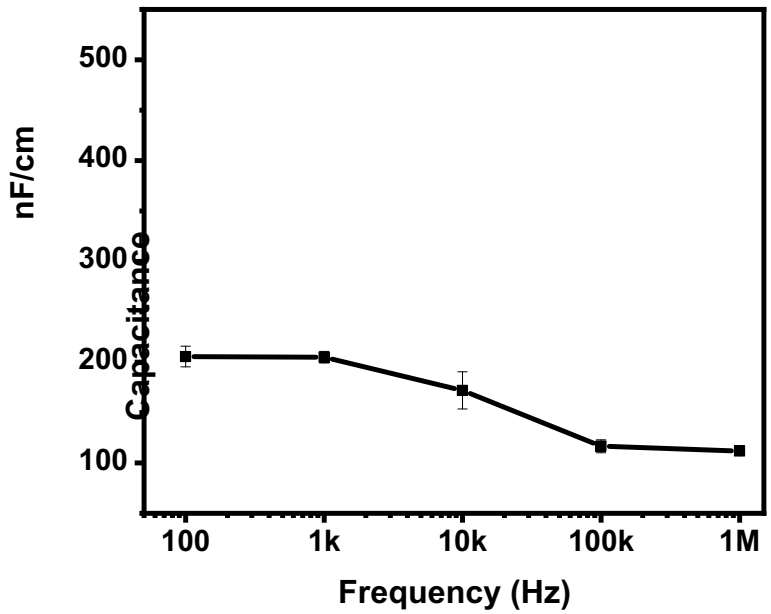


Figure S13. Capacitance versus frequency of sol-gel ZrO_x fabricated at 300°C. The value at 100Hz is used to calculate mobility for champion condition.

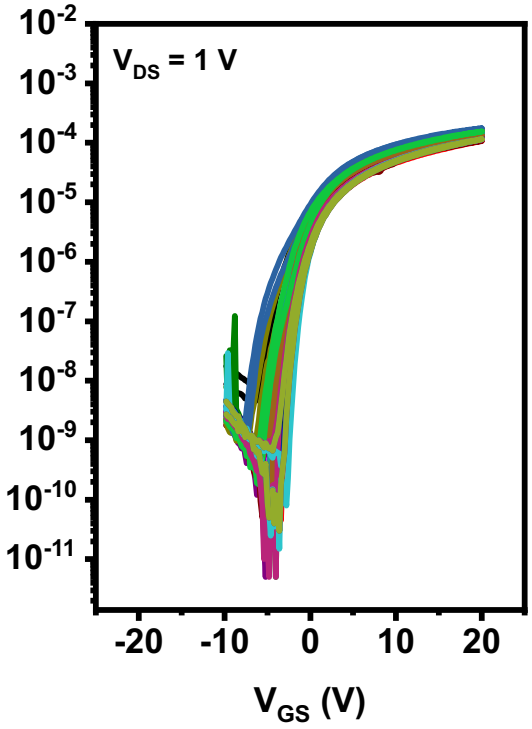


Figure S14. Series of transfer characteristics of homojunction 2D ITO 20%/40% printed at 160 °C with speed of 0.5 cm/s after 250°C post-annealed and PMMA encapsulation.

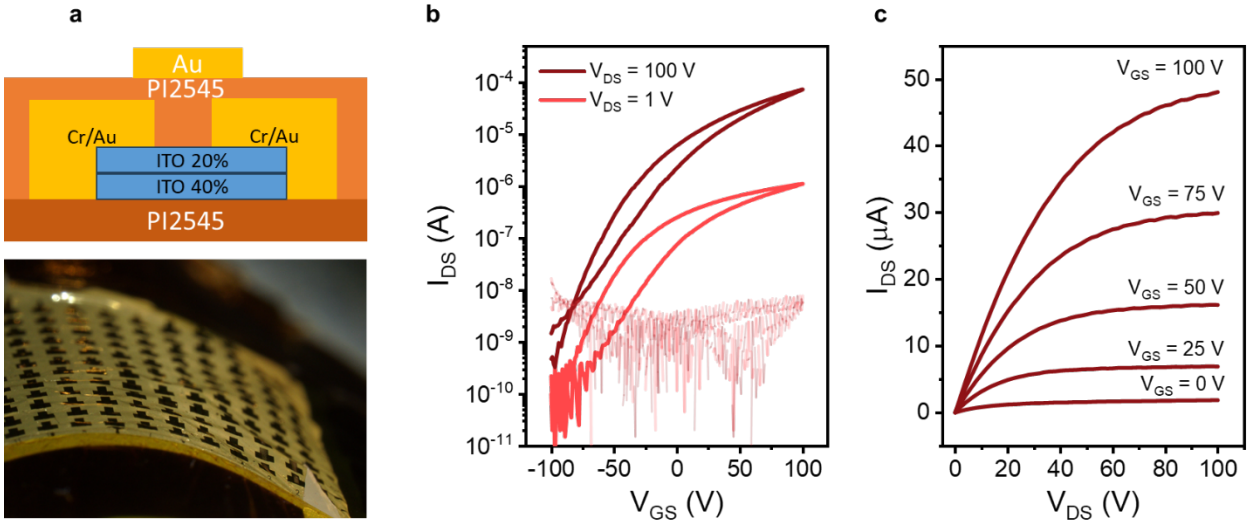
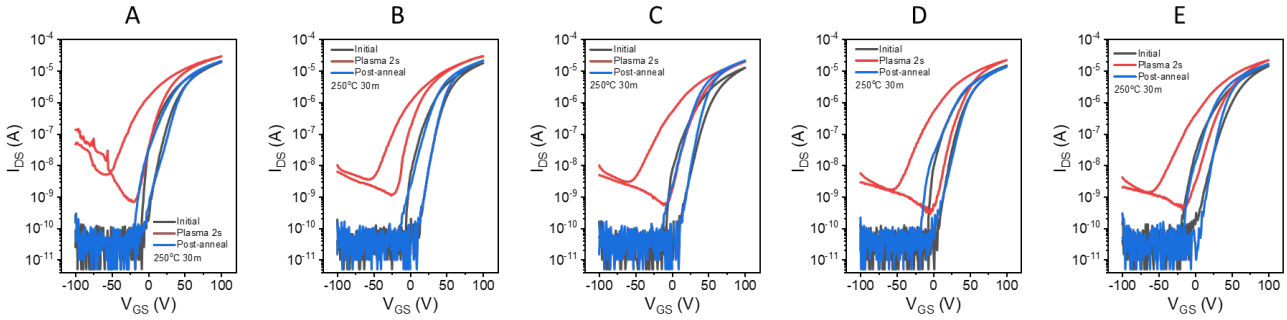


Figure S15. a) Schematic of top-gate structure of 2D ITO 20% (front channel)/40% (back channel) TFT fabricated at 160°C using PI2545 as both dielectric layer and substrate, b) Representative linear and saturation regime transfer characteristics. c) Output characteristic of top-gate 2D ITO 20% (front channel) /40% (back channel) TFT fabricated at 160°C on a flexible PI2545 substrate.



	Device A					Device B					Device C					Device D					Device E				
	Mobility	**V_{on}**	**V_{th}**	**SS**	**On/Off**	**Mobility**	**V_{on}**	**V_{th}**	**SS**	**On/Off**	**Mobility**	**V_{on}**	**V_{th}**	**SS**	**On/Off**	**Mobility**	**V_{on}**	**V_{th}**	**SS**	**On/Off**	**Mobility**	**V_{on}**	**V_{th}**	**SS**	**On/Off**
Initial	20	-8.0	40	2.9	$3.8 \cdot 10^6$	21	-5.0	44.7	3.3	$3.6 \cdot 10^6$	16	-7.0	49	3.4	$2.5 \cdot 10^6$	17	-7.0	45	2.8	$3.0 \cdot 10^6$	17	-17	45	4.2	$2.9 \cdot 10^6$
Plasma	23	-54	23	11	$4.3 \cdot 10^4$	26	-51	20.9	11.5	$2.7 \cdot 10^4$	20	-56	37	13	$3.7 \cdot 10^4$	21	-55	33	11	$7.6 \cdot 10^4$	21	-62	34	14	$5.5 \cdot 10^4$
Post-anneal 250oC 30m	22	-17	40	4.7	$4.1 \cdot 10^6$	24	-11	42.5	4.4	$4.3 \cdot 10^6$	24	-12	42	3.4	$4.3 \cdot 10^6$	14	-15	39	2.7	$2.7 \cdot 10^6$	18	-14	40	4.4	$3.3 \cdot 10^6$

Figure S16. (top) Transfer curves of ITO TFTs before and after plasma treatment as well as after 30 minutes of additional post annealing at 250 °C. The tables below show a summary of the device properties before and after plasma treatment and annealing.

Supporting Information

2D Amorphous Homojunction Transistors Exfoliated from Liquid Metals

*Minh Nhut Le, Md Saifur Rahman, Simon A. Agnew, Samuel W. Ong, and William J. Scheideler**

Thayer School of Engineering
Dartmouth College, Hanover, NH 03755, United States
E-mail: william.j.scheideler@dartmouth.edu

Table S1: *Summary of XPS O1s peak fitting results of 2D ITO with different wt % Sn.*

Condition	Sample	M-O-M peak at 529.7 ± 0.1 eV (%)	M-O-Vac peak at 531.2 ± 0.1 eV (%)	M-O-H peak at 532.2 ± 0.1 eV (%)
As-fabricated	40 wt% Sn	39	35	26
	20 wt% Sn	52	24	24
	10 wt% Sn	67	20	13
200°C post-anneal	40 wt% Sn	78	12	10
	20 wt% Sn	73	18	9
	10 wt% Sn	71	19	10

Table S2: *Summary of 2D printed ITO TFT performance after 250 ℃ annealing. Champion values are indicated with parentheses. A total of 12 devices were characterized on SiO_2 for each condition, except where noted: *16 devices on SiO_2; **20 devices on solution-processed ZrO_x. The values presented in this table are average values ± standard deviation, except for I_{on}/I_{off}, for which only the average value is shown.*

Sample	Printing Temperature (°C)	Number of Printed Layers	Linear Mobility ($cm^2/V \cdot s$)	V_{on} (V)	V_{th}(V)	Subthreshold Slope (V/dec)	I_{On}/I_{Off}
20%	140	3 layers	12±3.3 (15)	-65±6.0	17±7.0	4.4±0.9 (3.3)	$3.1 \cdot 10^6$
20%	150		18±2.2 (22)	-93±3.0	9.0±3.0	4.9±0.6 (4.0)	$4.3 \cdot 10^6$
20%	160		25±3.1 (30)	-100	-11±5.0	6.1±3.3 (3.5)	$1.0 \cdot 10^6$
20%-20%	150	2 layers	19±3.8 (23)	-70±8.0	7.0±10	4.6±0.6 (4.1)	$5.4 \cdot 10^6$
20%-40%			18±3.1 (23)	-59±6.0	18±4.0	4.1±0.9 (3.0)	$4.7 \cdot 10^6$
10%-40%			22±2.7 (26)	-79±7.0	10±8.0	4.7±0.7 (3.7)	$6.1 \cdot 10^6$
* 10%-10%	160	2 layers	30±7.0 (47)	-100	-27±25	14±21 (4.4)	$1.6 \cdot 10^5$
20%-20%			24±3.8 (28)	-84±5.0	-5.0±14	4.4±0.6 (3.5)	$6.8 \cdot 10^6$
*40%-40%			13±4.4 (21)	-71±15	-6.0±7.6	4.0±0.6 (3.0)	$4.8 \cdot 10^6$
10%-40%			27±3.3 (34)	-86±6.0	-2.0±3.0	4.3±0.7 (3.3)	$7.8 \cdot 10^6$
20%-40%			18±3.8(26)	-45±7.0	22±6.0	3.3±0.7 (2.4)	$4.5 \cdot 10^6$
**20%-40%(w/ ZrO_x)			24.7±3.30 (29.9)	-4.90±1.00	1.90±1.90	0.40±0.30 (0.10)	$6.5 \cdot 10^6$ ($2.68 \cdot 10^7$)

Table S3: *Summary of 2D ITO film thickness under various printing conditions. The films were post-annealed at 250 °C for 30 minutes to avoid influence from metal residue.*

Sample	Printing Temperature (°C)	Number of Printed Layers	Thickness (nm)
20%	140	3 layers	12.4±0.4
20%	150		12.8±0.1
20%	160		11.2±0.3
10%-10%	160	2 layers	6.4±0.2
20%-20%			7.6±0.3
40%-40%			6.6±0.2
10%-40%			6.9±0.6
20%-40%			7.1±0.2

Table S4: *Comparison of device statistics for 250 ℃ post-annealed 20/40% Sn homojunction devices fabricated in two independent device batches. All 50/50 devices measured from Batch 2 met a yield criteria of a mobility > 10 cm^2/Vs and an I_{on}/I_{off} ratio > 10^3.*

	μ_{lin} (cm^2/ V·s)	V_{on} (V)	V_{th} (V)	SS (V/dec)	I_{On}/I_{Off}
Batch 1 *(18 devices)*	*19.4±3.7*	*-61.3±6.2*	*12.6±6.2*	*4.8±1.1*	*$5.2 \cdot 10^6$*
Batch 2 *(50 devices)*	*21.1±5.0*	*-56.4 ± 18.0*	*20.2 ± 15.9*	*4.3±0.8*	*$6.7 \cdot 10^6$*

Table S5: *Summarized parameter of bias stress measurement for homolayer and homojunction device after 250 °C post-annealing. A total of 3 devices were characterized on SiO_2 for each condition. The values presented in this table are average values ± standard deviation.*

Printing temperature (°C)	Sample	PBS (30 V 5500s after PMMA) ΔV_{th} (V)	NBS (-30 V 5500s after PMMA) ΔV_{th} (V)
160	20%-20%	26±31	-18±19
	20%-40%	2.8±2.6	-5.3±1.0
	10%-40%	5.6±2.8	-5.4±6.8

Table S6: *Summary of 2D printed ITO TFT performance after 200 ˚C anneal. Champion values are indicated with parentheses. A total of 16 devices were characterized on SiO_2 for each condition. The values presented in this table are average values ± standard deviation, except for I_{on}/I_{off}, for which only the average value is shown.*

Sample	Printing Temperature (°C)	Number of Printed Layers	Linear Mobility ($cm^2/V \cdot s$)	V_{on} (V)	V_{th} (V)	Subthreshold Slope (V/dec)	I_{On}/I_{Off}
20%	140	3 layers	8.8±1.1 (11)	-58±11	28±8.8	5.2±0.9 (4.1)	$2.2 \cdot 10^6$
20%	150		11±1.9 (15)	-80±9.2	18±8.7	5.3±0.9 (4.0)	$2.3 \cdot 10^6$
20%	160		12±1.8 (14)	-59±37	23±4.8	6.0±1.1 (4.4)	$2.6 \cdot 10^6$
20%-20%	150	2 layers	5.4±1.5 (7.7)	-38±14	63±8.8	5.7±0.9 (4.3)	$4.5 \cdot 10^6$
20%-40%			9.0±2.3 (12)	-43±10	44±8.2	5.1±0.9 (4.1)	$1.7 \cdot 10^6$
10%-40%			11±3.0 (15)	-58±14	39±11	5.1±0.8 (4.0)	$1.8 \cdot 10^6$
10%-10%	160	2 layers	20±7.3 (39)	-70±12	31±11	7.6±6.9 (4.4)	$3.9 \cdot 10^6$
20%-20%			15±5.2 (23)	-66±19	32±13	6.0±2.3 (3.4)	$5.9 \cdot 10^6$
40%-40%			9.4±3.0 (17)	-36±8.3	46±14	5.6±2.2 (4.4)	$2.2 \cdot 10^6$
10%-40%			19±3.7 (25)	-40±8.6	47±5.7	4.7±1.3 (3.2)	$1.9 \cdot 10^6$
20%-40%			13±2.1 (17)	-33±15	44±11	4.5±0.9 (3.6)	$3.3 \cdot 10^6$

Table S7: *Summary of as-fabricated ITO TFT performance. Champion values are indicated with parentheses. A total of 3 devices were characterized for each condition. Devices were substrate-gated with a 300 nm thermally-grown SiO_2 gate dielectric. The values presented in this table are average values ± standard deviation, except for I_{on}/I_{off}, for which only the average values are shown.*

Sample	Printing Temperature (°C)	Number of Printed Layers	Linear Mobility ($cm^2/V \cdot s$)	I_{On}/I_{Off}
20%	140	3 layers	2.5±0.5 (3.0)	7.5
20%	150		6.9±1.4 (8.3)	4.6
20%	160		5.1±0.2 (5.3)	1.5
20%-20%	150	2 layers	3.5±0.1 (3.6)	20
20%-40%			6.3±2.3 (8.6)	$1.6 \cdot 10^3$
10%-40%			13±0.6 (14)	$1.3 \cdot 10^2$
20%-20%	160	2 layers	23±1.9 (26)	5.2
20%-40%			16±1.2 (17)	29
10%-40%			25±4.4 (30)	4.0
40%-40%			0.14±0.03 (0.18)	$2.0 \cdot 10^4$
10%-10%			13±4.9 (18)	1.5

Table S8: *Summary of other 2D oxide printed TFTs for benchmark performance comparison.*

Reference	DOI	Material	Carrier Type	Structural Nature	Printing Temperature (°C)	Post-annealing Temperature (°C)	Mobility ($cm^2/V \cdot s$)
[4]	10.1002/admi.202202036	In_2O_3	n	c	250°C	250°C 2h	96
[3]	10.1038/s41699-022-00294-9	In_2O_3	n	c	165°C	250°C 1h	67
[17]	10.1021/acsnano.1c11205	ITO	n	c	200°C	200°C	27
[35]	10.1002/admi.201900007	SnO (bottom)/In_2O_3 (top)	n	c	300°C for Sn, 200°C for In	/	37
[36]	10.1002/adom.202200925	IAO	n	c	250°C	/	40
[20]	10.1021/acsnano.0c06791	IZO	n	c	200°C	/	87
[37]	10.1021/acs.nanolett.2c04555	InO_x/GaO_x	n	c	200°C	/	22.6
[21]	10.1021/acsaelm.3c00127	GaInSnO	n	c	200°C	/	65.4
[38]	10.1021/acsami.1c15990	SnO	p	c	230°C	/	0.47
[39]	10.1002/pssr.201900271	Beta-Ga_2O_3	p	c	180°C	/	21.3
[40]	10.1039/d2nr04535d	IZTO	n	a	200°C	/	0.5
[41]	10.1039/d4tc02312a	IZO/Ga_2O_3	n	a	200°C	/	20.79

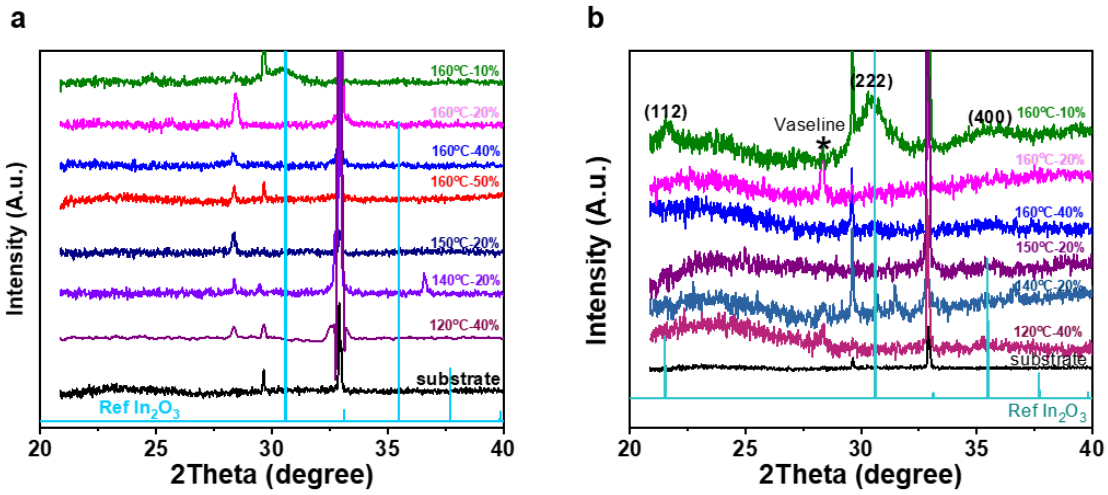


Figure S1. *XRD pattern of series of 2D ITO with variation of temperature and Sn% a) as-fabricated and b) after 250 ℃ post-annealing.*

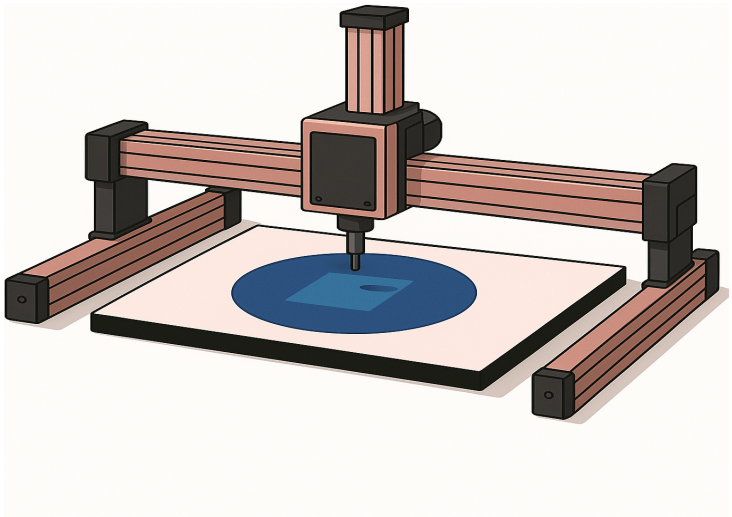


Figure S2. *Schematic of the robotic reflectometry setup used for film thickness mapping. The reflectometer probe is mounted on a Genmitsu system and controlled via GrblControl and Microsoft Power Automate, enabling automatically measurements at 1 mm intervals.*

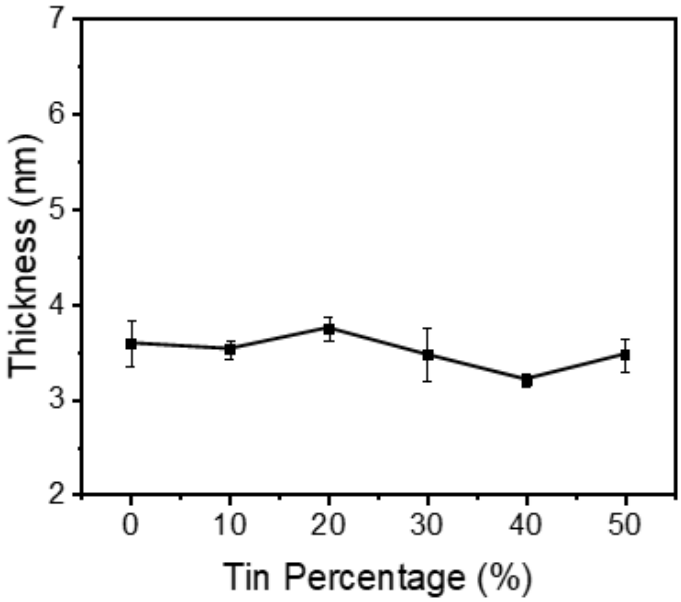


Figure S3. *Measured thickness of 2D ITO films as a function of Sn content (wt% in the precursor metal alloy) printed under identical conditions. All films were post-annealed at 250 °C for 30 min to eliminate potential influence from residual metal. Before 2D oxide thickness measurements, the SiO_2 thickness was also measured to allow the utilization of a two-layer spectral reflectance model. Thickness values represent the average of six measurement points, with error bars indicating the standard deviation. At each point, normal-incidence reflectivity was measured and fitted to an optical model based on the Fresnel equations, using known refractive indices of the film and substrate. The local film thickness was extracted by matching the experimental data to the simulated reflectivity profile. To ensure high accuracy, only data points with a goodness of fit (GoF) greater than 0.995 were included in the final analysis. Error bars shown in this plot are equal to one standard deviation.*

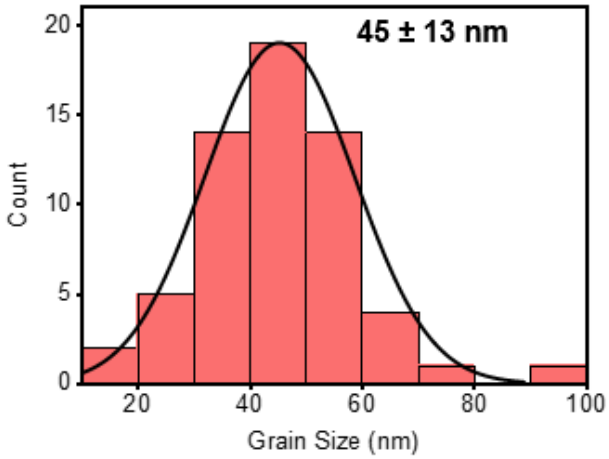
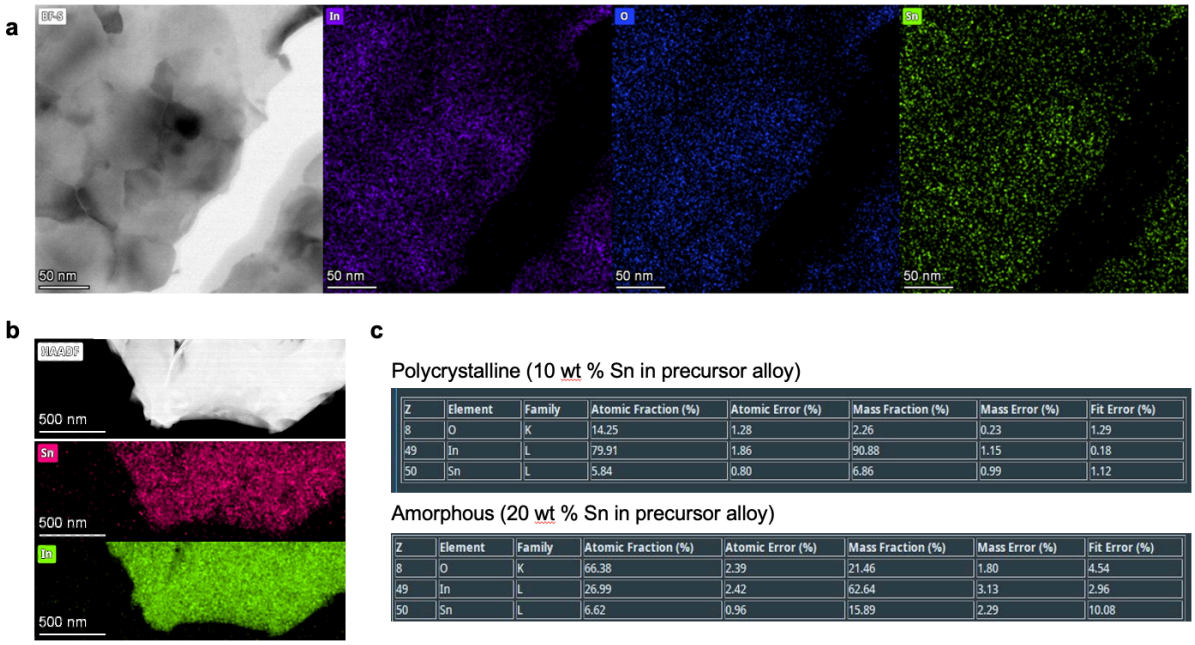


Figure S4. *Grain size histogram of 2D ITO (7.5% Sn) printed 170 °C with 0.5 cm/s speed as extracted from the AFM scan shown in* ***Figure 1****. Annotation shows the average grain size plus / minus a single standard deviation.*



Polycrystalline (10 wt % Sn in precursor alloy)

Z	Element	Family	Atomic Fraction (%)	Atomic Error (%)	Mass Fraction (%)	Mass Error (%)	Fit Error (%)
8	O	K	14.25	1.28	2.26	0.23	1.29
49	In	L	79.91	1.86	90.88	1.15	0.18
50	Sn	L	5.84	0.80	6.86	0.99	1.12

Amorphous (20 wt % Sn in precursor alloy)

Z	Element	Family	Atomic Fraction (%)	Atomic Error (%)	Mass Fraction (%)	Mass Error (%)	Fit Error (%)
8	O	K	66.38	2.39	21.46	1.80	4.54
49	In	L	26.99	2.42	62.64	3.13	2.96
50	Sn	L	6.62	0.96	15.89	2.29	10.08

Figure S5. *(a) Bright-field STEM image (left) and corresponding EDS elemental maps of In (purple), O (blue), and Sn (green) for the 2D crystalline 10% Sn ITO sample printed at 160 °C after 250 °C post-annealing for 1 hour. (b) HAADF TEM showing In (green) and Sn (pink) for amorphous ITO (20 wt% Sn precursor alloy) post-annealed at 250 °C for 1 hr. (c) Table summarizing stoichiometry for polycrystalline (10 wt% Sn) and amorphous (20 wt% Sn) samples measured via EDS.*

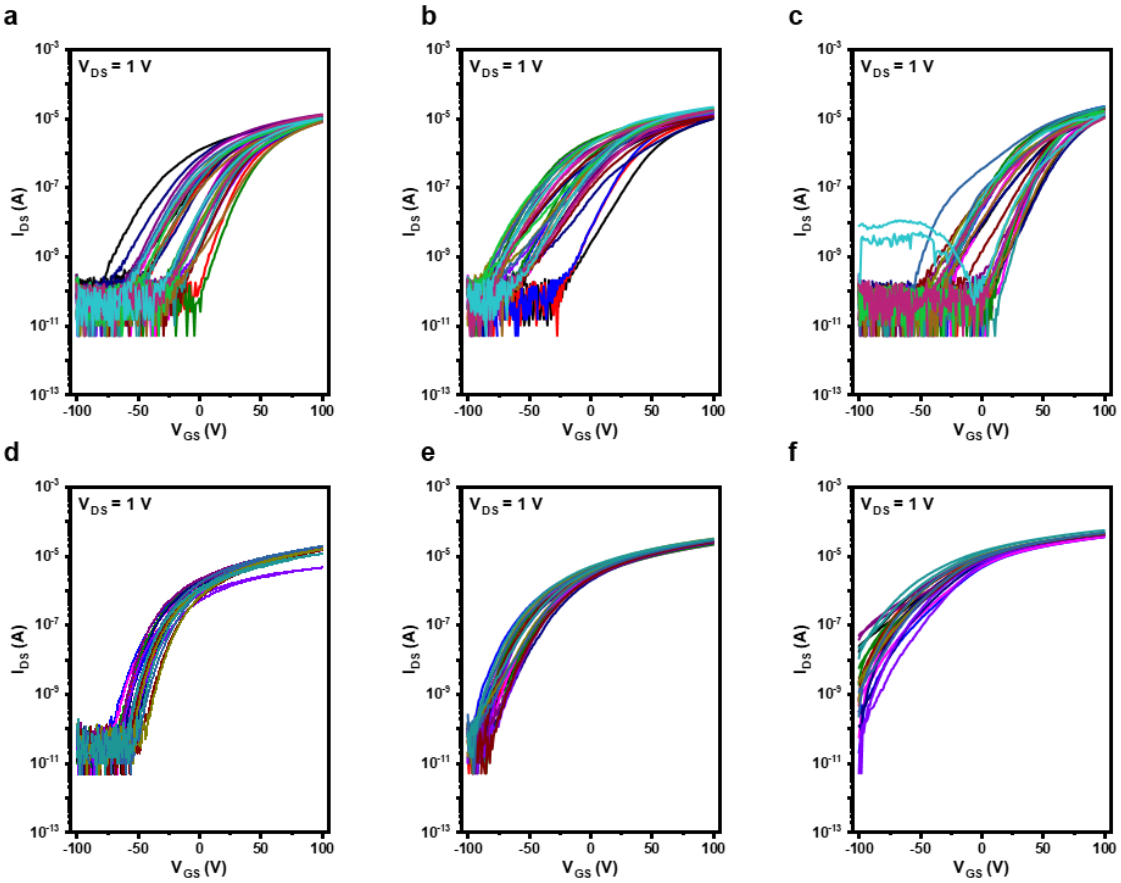


Figure S6. *Series of transfer characteristic of 2D ITO film post-annealed at 200 ˚C for a) 140 ˚C printed 3 layer 20% Sn channels, b) 150 ˚C printed 3 layer 20% Sn channels, c) 160 ˚C printed 3 layer 20% Sn channels, Series of transfer characteristic of 2D ITO devices post-annealed at 250 ˚C and PMMA encapsulated for d) 140 ˚C printed 3 layer 20% Sn channels, e) 150 ˚C printed 3 layer 20% Sn channels, and f) 160 ˚C printed 3 layer 20% Sn channels.*

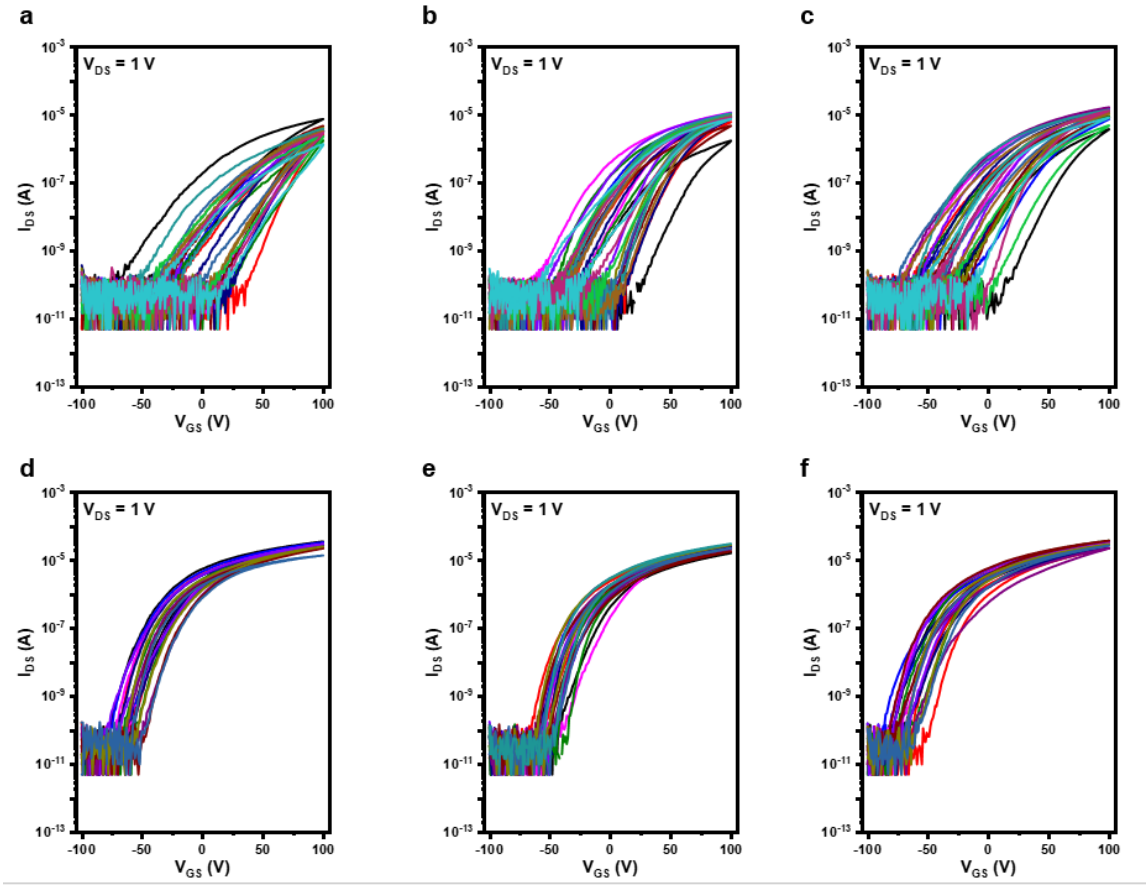


Figure S7. *Series of transfer characteristic of 2D ITO devices post-annealed at 200 °C for a) 150 °C printed 2 layer 20%/20% Sn channels, b) 150 °C printed 2 layer 20%/40% Sn channels, c) 150 °C printed 2 layer 10%/40% Sn channels. Series of transfer characteristic of 2D ITO channels post-annealed at 250 °C and PMMA encapsulated for d) 150 °C printed 2 layer 20%/20% Sn channels, e) 150 °C printed 2 layer 20%/40% Sn channels, f) 150 °C printed 2 layer 10%/40% Sn channels.*

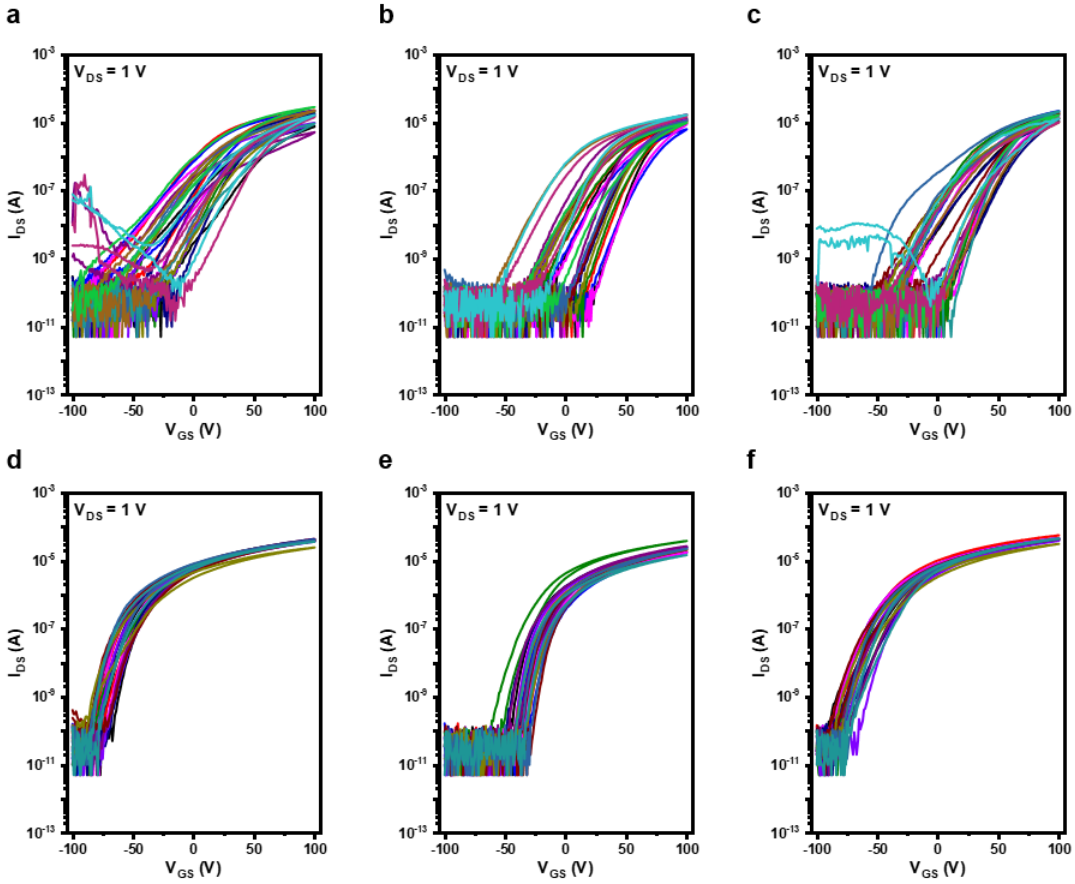


Figure S8. *Series of transfer characteristic of 2D ITO film post-anneal at 200 ˚C for a) 160 ˚C printed 2 layer 20%/20% Sn channels, b) 160 ˚C printed 2 layer 20%/40% Sn channels, c) 160 ˚C printed 2 layers 10%/40% Sn. Series of transfer characteristic of 2D ITO channels post-annealed at 250 ˚C and PMMA encapsulated for d) 160 ˚C printed 2 layer 20%/20% Sn channels, e) 160 ˚C printed 2 layer 20%/40% Sn channels, f) 160 ˚C printed 2 layer 10%/40% Sn channels.*

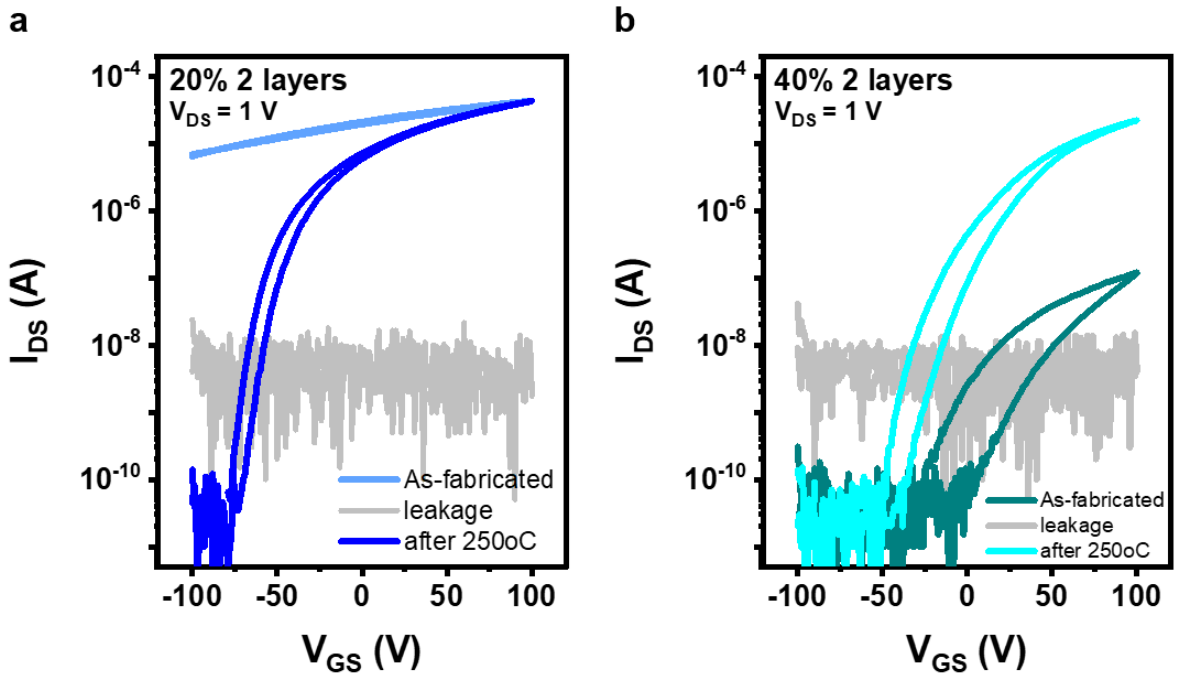


Figure S9. *Transfer characteristic of as fabricated and after post-annealing at 250°C 2D oxide films for a) 20% Sn 2D ITO and b) 40% Sn 2D ITO printed at 150 °C.*

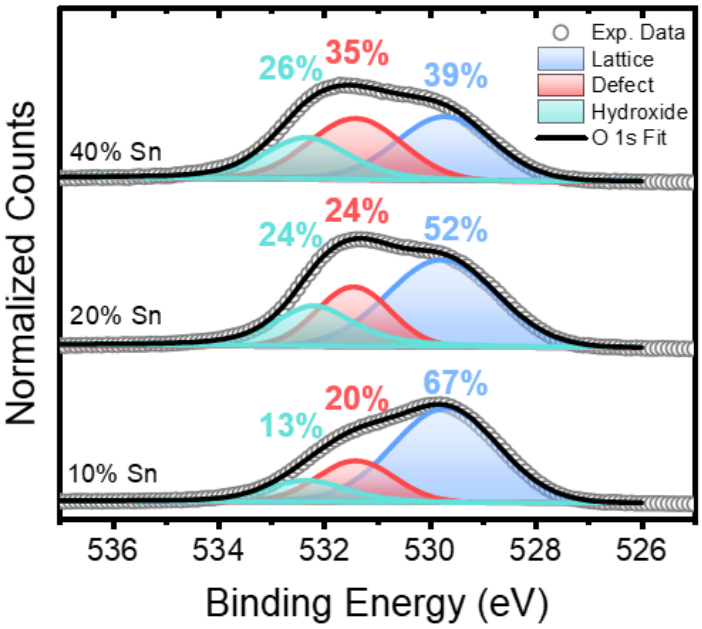


Figure S10. *XPS O1s study of as-fabricated 10, 20, 40% Sn 2D ITO films.*

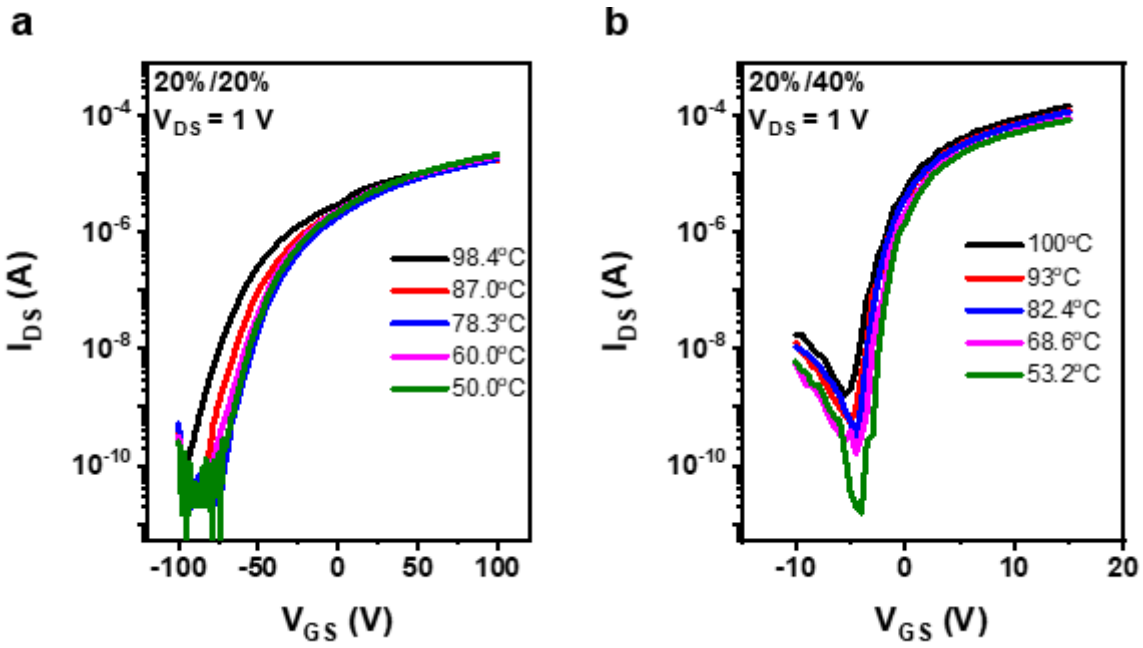


Figure S11. *Temperature-dependent transfer characteristics measurements of a) 2-layer homolayer 2D ITO 20%/20% and b) homojunction 2D ITO 20%/40% printed at 160 ℃ with speed of 0.5 cm/s after 250 ℃ post-annealed and PMMA encapsulation.*

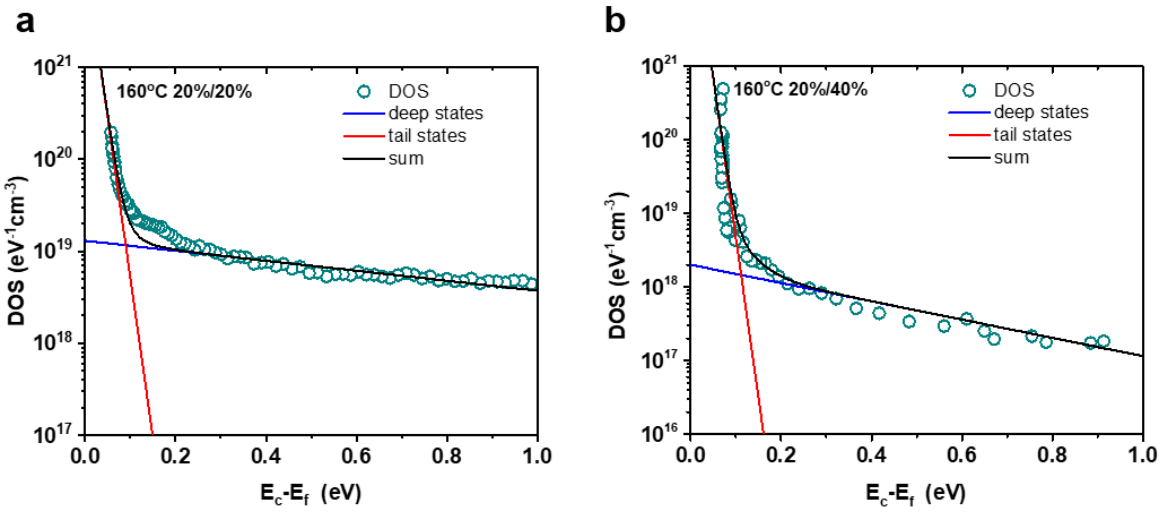


Figure S12: *Biexponential DOS distribution fits for extracted DOS of a) homojunction 20%/20% Sn printed at 160 °C and b) homojunction 20%/40% Sn printed at 160 °C.*

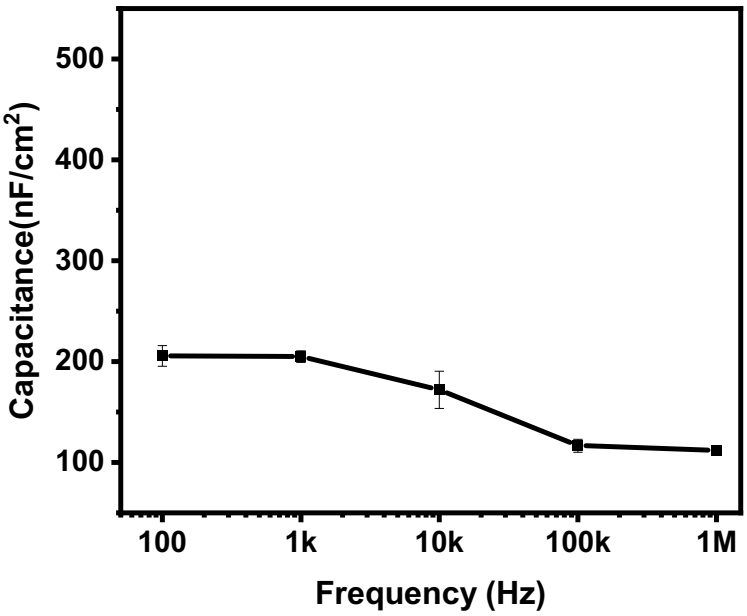


Figure S13. *Capacitance versus frequency of sol-gel ZrO_x fabricated at 300 °C. The value at 100 Hz is used to calculate mobility for champion condition.*

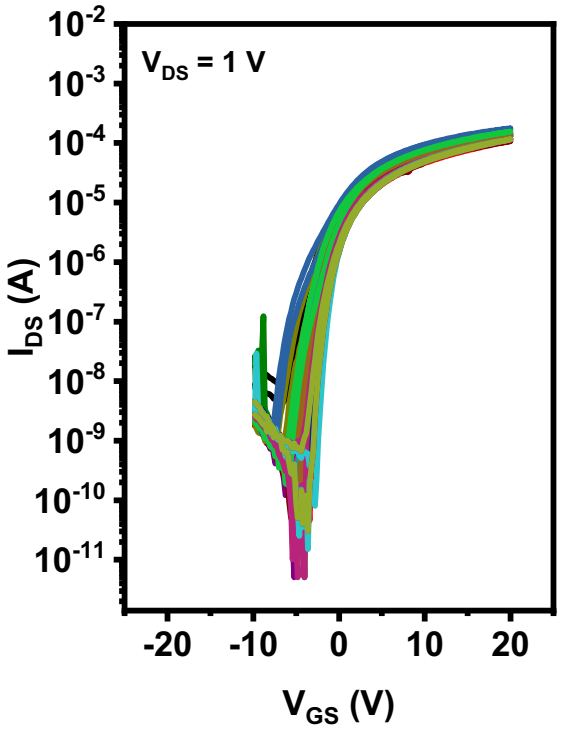


Figure S14. *Series of transfer characteristics of homojunction 2D ITO 20%/40% printed at 160 ℃ with speed of 0.5 cm/s after 250 ℃ post-annealed and PMMA encapsulation.*

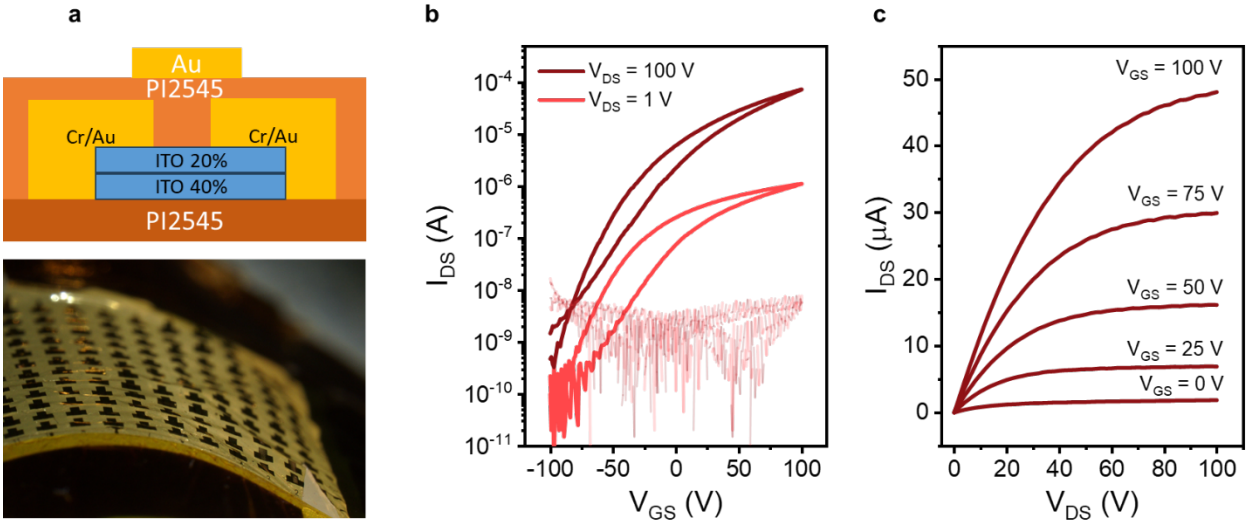
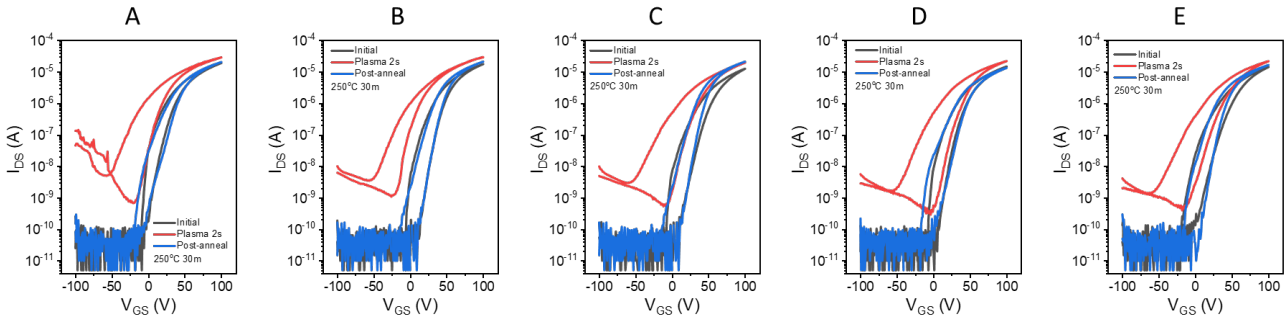


Figure S15. *a) Schematic of top-gate structure of 2D ITO 20% (front channel)/40% (back channel) TFT fabricated at 160 °C using PI2545 as both dielectric layer and substrate, b) Representative linear and saturation regime transfer characteristics. c) Output characteristic of top-gate 2D ITO 20% (front channel) /40% (back channel) TFT fabricated at 160 °C on a flexible PI2545 substrate.*



	Device A					Device B					Device C					Device D					Device E				
	Mobility ($cm^2/V·s$)	V_{on} (V)	V_{th} (V)	SS (V/dec)	On/Off	Mobility ($cm^2/V·s$)	V_{on} (V)	V_{th} (V)	SS (V/dec)	On/Off	Mobility ($cm^2/V·s$)	V_{on} (V)	V_{th} (V)	SS (V/dec)	On/Off	Mobility ($cm^2/V·s$)	V_{on} (V)	V_{th} (V)	SS (V/dec)	On/Off	Mobility ($cm^2/V·s$)	V_{on} (V)	V_{th} (V)	SS (V/dec)	On/Off
Initial	4	-8.0	40	2.9	$3.8·10^6$	21	-5.0	44.7	3.3	$3.6·10^6$	16	-7.0	49	3.4	$2.5·10^6$	17	-7.0	45	2.8	$3.0·10^6$	17	-17	45	4.2	$2.9·10^6$
Plasma	23	-54	23	11	$4.3·10^4$	26	-51	20.9	11.5	$2.7·10^4$	20	-56	37	13	$3.7·10^4$	21	-55	33	11	$7.6·10^4$	21	-62	34	14	$5.5·10^4$
Post-anneal 250 °C 30m	22	-17	40	4.7	$4.1·10^6$	24	-11	42.5	4.4	$4.3·10^6$	24	-12	42	3.4	$4.3·10^6$	14	-15	39	2.7	$2.7·10^6$	18	-14	40	4.4	$3.3·10^6$

Figure S16. *(top) Transfer curves of ITO TFTs before and after plasma treatment as well as after 30 minutes of additional post annealing at 250 °C. (bottom) Tables showing a summary of the device properties before and after plasma treatment and annealing.*