

Introducing Semiconducting-to-Metallic Transitions into Wafer-Scale 2D PdSe₂ Layers by Low-Temperature Anion Exchange and Thickness Modulation

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Cite This: *ACS Nano* 2024, 18, 35336–35346



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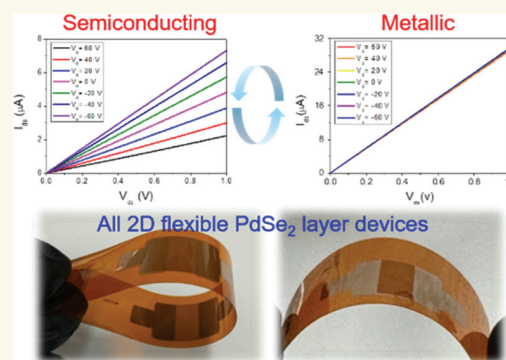
ABSTRACT: Two-dimensional (2D) palladium diselenide (PdSe₂) layers are projected to exhibit a number of intriguing electrical properties such as semiconducting-to-metallic transitions. Precisely modulating their morphology and chemistry is essential for realizing such opportunities, which is particularly demanded on a large dimension under flexible processing conditions toward broadening their practical device applicability. Herein, we explore a wafer-scale growth of 2D PdSe₂ layers and introduce semiconducting-to-metallic transitions into them at as low as 330 °C, a temperature compatible with a range of polymeric substrates as well as the back-end-of-line (BEOL) processes. Two independent physical and chemical approaches of thickness modulation and anion exchange are demonstrated to induce the low-temperature-driven electrical transitions. Wafer-scale 2D PdSe₂ layers grown from a scalable selenization of thin (~2 nm) Pd exhibit *p*-type semiconducting characteristics, which completely vanish with increasing thickness. Furthermore, a postgrowth reaction involving an exchange of selenium (Se)-to-tellurium (Te) ions chemically introduces the semiconducting-to-metallic transitions through the conversion of PdSe₂-to-palladium ditelluride (PdTe₂). A significant reduction of the bandgap energy from 0.7 to 0 V is observed to be associated with the transitions, while the converted 2D layers remain to be highly metallic irrespective of thickness variations. These controlled transition characteristics are employed to fabricate “all-2D” flexible devices employing semiconducting 2D layer channels and metallic 2D layer electrodes on a wafer-scale.

KEYWORDS: 2D TMD, PdSe₂, PdTe₂, anion exchange, thickness control, semiconducting-to-metallic transition

INTRODUCTION

Investigations of two-dimensional (2D) transition metal dichalcogenide (TMD) layers have rapidly accelerated with emphasis on unveiling their morphology- and/or chemistry-dependent transitions of electrical and optical properties. A number of 2D TMD layers have been identified to exhibit such transition characteristics (e.g., layer number-dependent tunability of bandgap energy), mostly in those employing group VI transition metals such as molybdenum (Mo) and tungsten (W).^{1,2} Recently, group X elements (e.g., platinum (Pt) and palladium (Pd)) have emerged as the transition metal components for 2D TMDs owing to their distinct advantages over the conventional VI metals. For example, their significantly lower melting temperatures enable the direct chemical reaction and growth of 2D layers even on polymeric substrates.^{3–6} Furthermore, group X-based 2D TMD layers are also projected to exhibit the aforementioned layer morphol-

ogy-dependent transient characteristics, mostly predicted by theoretical studies.^{7,8} Among them, Pd-based TMDs such as 2D palladium diselenide (PdSe₂) layers exhibit favorable properties over Pt-based ones mainly due to the easier processability of Pd with low cost and ambient stability.⁹ In fact, 2D PdSe₂ layers are particularly attractive for digital electronics with a large set of process-property advantages; for example, tunable bandgap energies accompanying semiconducting-to-metallic transitions^{10–14} and low-temperature manufacturability.^{15–20} Synthesis of 2D PdSe₂ layers with



Received: August 22, 2024

Revised: November 30, 2024

Accepted: December 10, 2024

Published: December 17, 2024



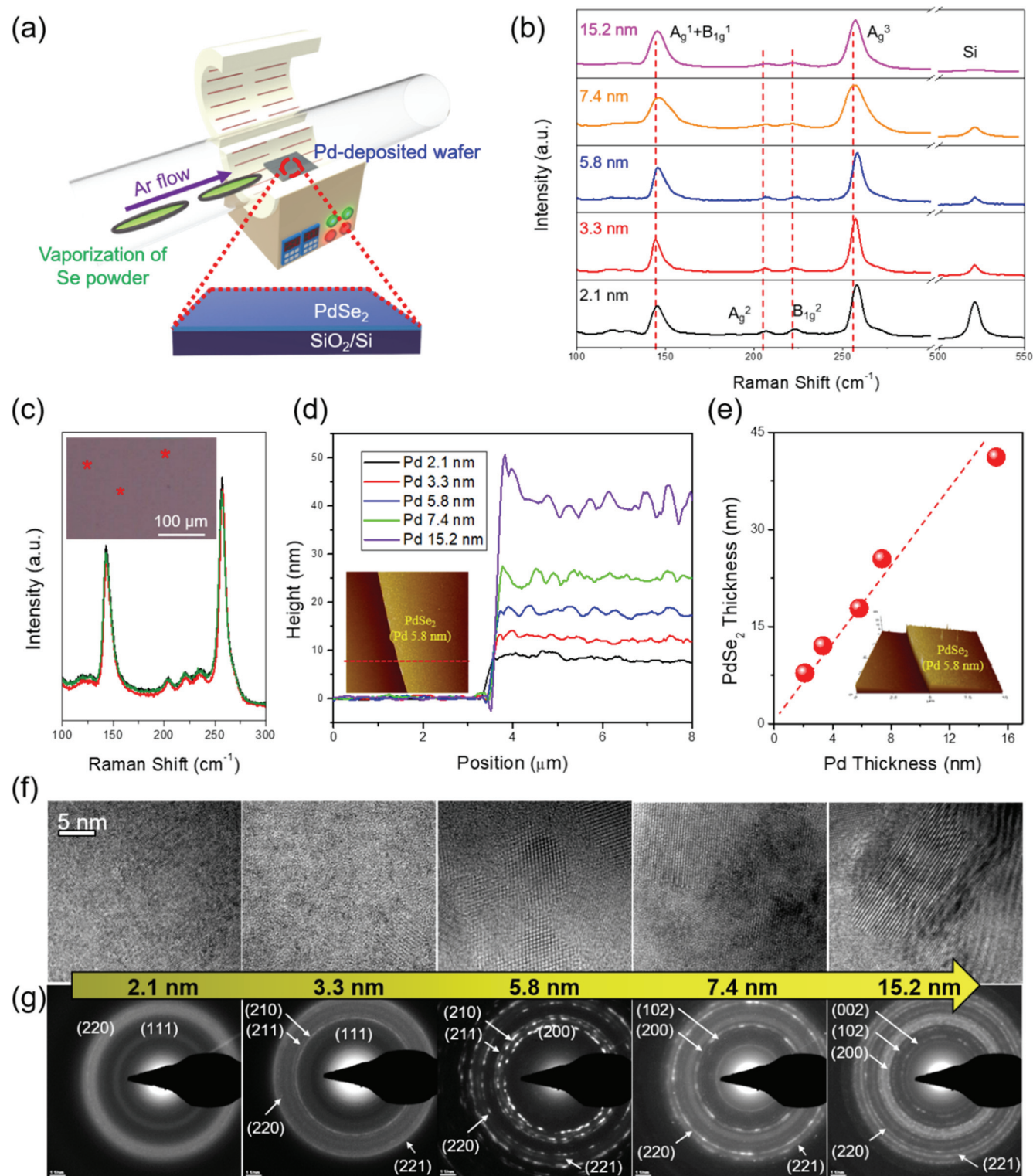


Figure 1. Thickness-variant growth and characterization of 2D PdSe₂ layers. (a) Schematic for CVD growth of 2D PdSe₂ layers. (b) Raman spectra of 2D PdSe₂ layers prepared with five different Pd thicknesses. (c) Raman spectra obtained from various locations of an identical sample prepared with Pd thickness of 2.1 nm. The inset shows an optical microscopy image of the sample. (d) AFM height profiles of 2D PdSe₂ layers prepared with five different Pd thicknesses along with a representative AFM topography image (inset). (e) Correlation of Pd thickness with resulting 2D PdSe₂ layers' thickness along with a representative AFM topography image (inset). (f), (g): TEM characterizations of thickness-variant 2D PdSe₂ layers manifested by (f) HR-TEM and (g) SAED images.

desired thickness and crystallinity has been explored with a variety of methods, among which, a chemical vapor deposition (CVD) is promising due to its process scalability of guaranteeing

a high spatial uniformity.^{21–23} This intrinsic advantage can facilitate systematic studies on the structure–property relations of 2D PdSe₂ layers, vastly broadening their application aspects

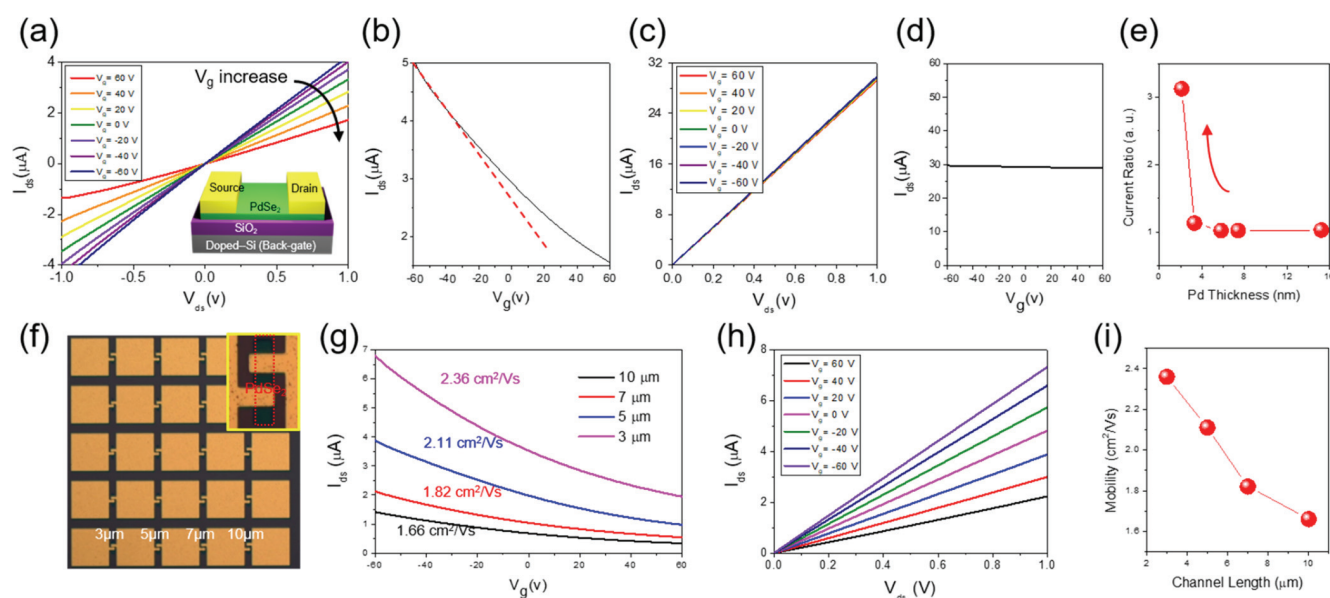


Figure 2. Semiconducting-to-metallic transition in thickness-variant 2D PdSe₂ layers manifested by FET measurements. (a) I_{ds} – V_{ds} curves with varying V_g obtained from a FET employing thin 2D PdSe₂ layers (Pd thickness = 2.1 nm). (b) I_{ds} – V_g curve obtained from the same FET in (a) at V_{ds} = 1 V along with its device schematic (inset). (c) I_{ds} – V_{ds} curves with varying V_g obtained from a FET employing thick 2D PdSe₂ layers (Pd thickness = 7.4 nm). (d) I_{ds} – V_g curve obtained from the same FET in (c) at V_{ds} = 1 V. (e) Comparison of I_{ds} ratios at V_g = ± 60 as a function of Pd thickness. (f) Optical microscopy image of patterned FET array. (g) I_{ds} – V_g curves with varying channel lengths. (h) V_g -dependent I_{ds} – V_{ds} curves obtained from 3 μ m channel FET. (i) Correlation of mobility value vs channel length.

in electronics, optoelectronics and beyond.^{24–30} Modulating the morphology and chemistry of wafer-scale 2D PdSe₂ layers during and/or after their growth stages is essential toward tuning their resulting electrical and optical properties. This approach mainly aims at unveiling their coexisting semiconducting and metallic transport properties; i.e., semiconducting and metallic 2D layers function as active channels and passive electrodes for digital electronics, respectively.

Herein, we report a wafer-scale (>cm²) CVD growth of 2D PdSe₂ layers via a direct selenization of Pd seed films at growth temperature as low as 330 °C. By leveraging their precisely controlled composition and morphology, we systematically introduce strong semiconducting-to-metallic transitions into them via two independent physical and chemical methods; i.e., thickness modulation and anion exchange of Se-to-Te, respectively. Regarding the physical method, thinner 2D PdSe₂ layers prepared with Pd films of <3 nm thickness display notable semiconducting characteristics accompanying a hole mobility of 2.32 cm²/V·s while thicker ones remain metallic irrespective of thickness variations. Regarding the chemical method, the thin semiconducting 2D PdSe₂ layers are demonstrated to be converted to metallic stoichiometric 2D palladium ditelluride (PdTe₂) layers via a postgrowth tellurization reaction at 330 °C. The converted 2D PdTe₂ layers display a significant reduction in the bandgap energy from 0.7 to 0 eV accompanying thickness-invariant metallic characteristics, verified by a variety of spectroscopic techniques.

RESULTS

Figure 1a outlines a schematic for the CVD growth of thickness-controlled wafer-scale 2D PdSe₂ layers and the tellurization reaction for their conversion to 2D PdTe₂ layers. For the CVD growth, a thickness-controlled Pd film is deposited onto a silicon dioxide/silicon (SiO₂/Si) wafer by

an electron beam deposition at a rate of about 0.05 Å/s. Subsequently, the Pd deposited-SiO₂/Si wafer is reacted with a vaporized Se at 330 °C for 60 min, following the temperature ramping rate of 10 °C/min. During the reaction, argon (Ar) gas is continuously supplied into the CVD chamber at a flow rate of ~100 standard cubic centimeters per minute (SCCM) and at a pressure of 100 mTorr. For the conversion reaction, as-prepared 2D PdSe₂ layers are reacted with vaporized Te instead of Se under the exactly identical conditions employed for the CVD growth reaction at 330 °C. Figure 1b depicts the Raman spectroscopy analysis of 2D PdSe₂ layers prepared with five different Pd thickness of 2.1, 3.3, 5.8, 7.4, and 15.2 nm. Raman peaks corresponding to A_g and B_g vibration modes are distinctively observed at 143.6, 205.3, 220.8, and 255.7 cm^{−1}, which perfectly aligns with earlier studies on 2D PdSe₂ layers.³¹ Furthermore, we inspected the location-specific spatial uniformity of single samples. Figure 1c presents Raman spectra of a representative sample of 2D PdSe₂ layers prepared with 2.1 nm Pd, collected from the randomly selected locations on a large area of >100 μ m² (inset image). Nearly identical Raman characteristics are identified, which strongly supports the high spatial homogeneity of 2D PdSe₂ layers within/across samples. Figure 1d provides atomic force microscopy (AFM) profiles of the samples prepared with various Pd thickness, where the distance-dependent height variations denote the thickness of 2D PdSe₂ layers with respect to the surfaces of bare substrates. A representative AFM topography image along with a line scan orientation (red line) is also provided in the inset. Figure 1e shows a linear relation in the thickness of Pd films vs 2D PdSe₂ layers determined by AFM characterizations, indicating a thickness increase of ~2.5 times through the CVD selenization. The inset presents an AFM topography image of 2D PdSe₂ layers prepared with 5.8 nm Pd in a projected view. Additional AFM images of samples prepared with various Pd thicknesses are presented in Supporting Information, Figure S1. As-

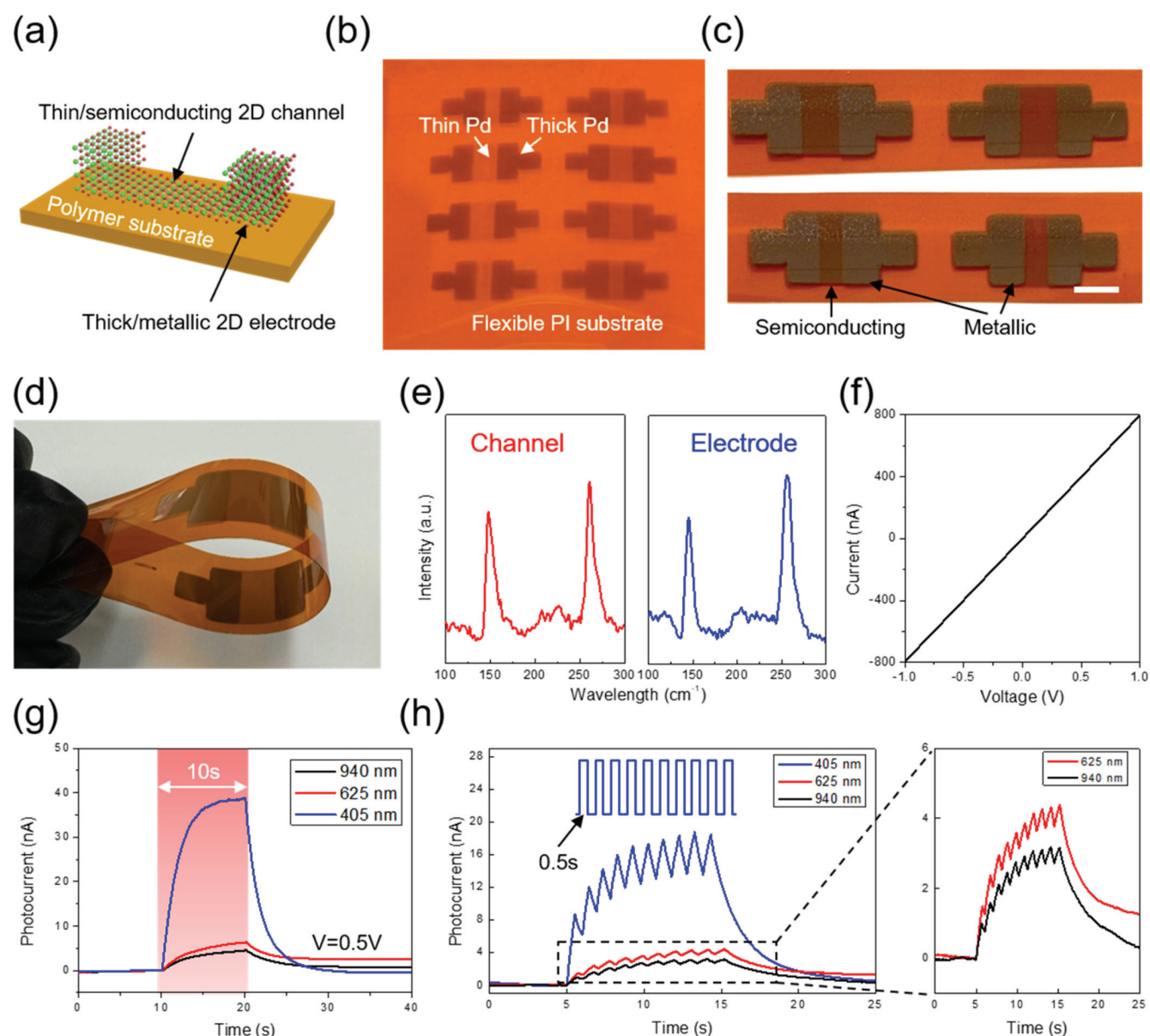


Figure 3. Application of thickness-variant semiconducting-to-metallic transition for all-2D PdSe₂ layers-based flexible devices. (a) Schematic of all-2D flexible device employing thickness-modulated 2D PdSe₂ layers. (b) Image of thickness-modulated Pd arrays patterned on PI substrate. (c) Image of patterned thin/thick 2D PdSe₂ layers. The scale bar is 5 mm. (d) Mechanical bending of patterned thin/thick 2D PdSe₂ layers on PI substrate. (e) Raman spectra obtained from thin channels and thick electrodes. (f) *I*–*V* curve showing Ohmic transport. (g) Temporal plot of photoresponsiveness under continuous illuminations for 10 s at three different wavelengths. (h) Temporal plot of broadband synaptic plasticity under optical pulse illuminations with 0.5 s intervals. The smaller photocurrents for 625 and 940 nm wavelengths reflect their lower illumination intensities compared to that of 405 nm illumination.

prepared 2D PdSe₂ layers were characterized via transmission electron microscopy (TEM) imaging and diffraction techniques, toward better clarifying their thickness-microstructure correlation. Figure 1f depicts high-resolution TEM (HR-TEM) images of thickness-varying samples taken at an identical magnification, revealing lattice fringes regardless of thickness variations. Figure 1g displays selected area electronic diffraction (SAED) patterns corresponding to the thickness-variant 2D PdSe₂ layers in Figure 1f. The multiple diffraction rings observed in each sample are indexed to the crystalline planes of PdSe₂ crystals in an orthorhombic structure with a *P*_{bca} space group, characterized by lattice parameters of *a* = 5.75 Å, *b* = 5.87 Å, and *c* = 7.69 Å.^{9,11,32}

Having verified the structural morphology of 2D PdSe₂ layers, we systematically investigated their thickness-dependent electrical properties by employing field effect transistor (FET) characterizations. Figure 2a inset provides a schematic illustration of a SiO₂/Si back-gate FET featuring thickness-variant 2D PdSe₂ layers as a channel. Figure 2a presents FET characteristics of drain-source current (*I*_{ds}) vs voltage (*V*_{ds}) with a varying back-gate voltage (*V*_g) obtained from a 2D PdSe₂ layers-incorporated FET (Pd thickness = 2.1 nm). The FET exhibits a strong *p*-type gate response manifested by a systematic decrease of *I*_{ds} with increasing *V*_g. Figure 2b presents the corresponding FET transfer curve of *I*_{ds} vs *V*_g obtained at *V*_{ds} = 1 V, further supporting the *p*-type

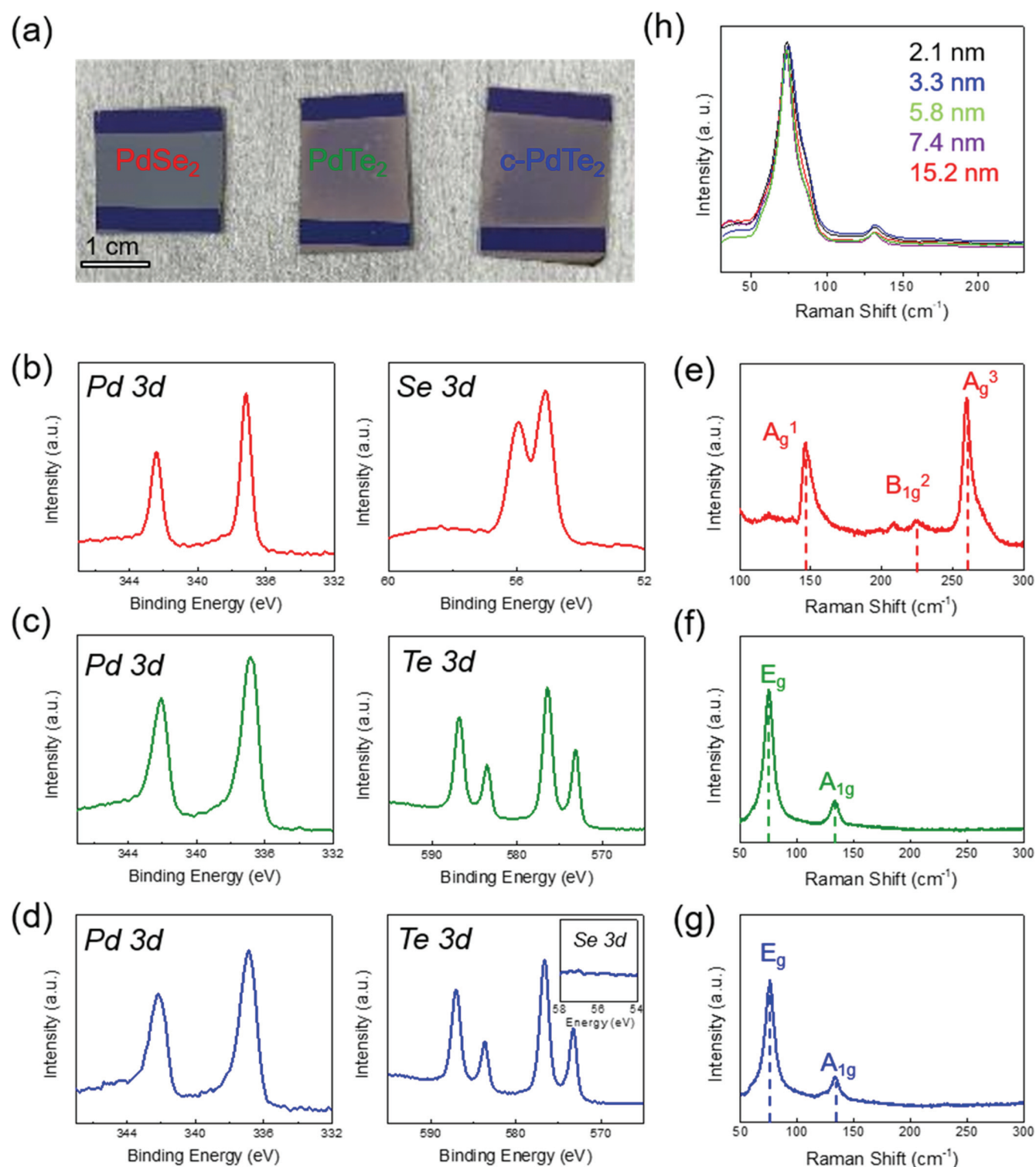


Figure 4. Anion exchange-driven conversion of 2D PdSe₂ layers to 2D PdTe₂ layers and its spectroscopic characterization. (a) Sample images of as-prepared PdSe₂ and PdTe₂ layers as well as converted (c) PdTe₂ layers. (b)–(d): XPS core binding energy spectra of (b) as-prepared PdSe₂, (c) as-prepared PdTe₂, and (d) c-PdTe₂ layers. (e)–(g): Raman spectra of (e) as-prepared PdSe₂, (f) as-prepared PdTe₂, and (g) c-PdTe₂ layers.

semiconducting transport. The linear regime (red tangential line) of the FET yields its hole mobility^{30,33} which is determined to be ~ 2.32 cm²/V·s. Meanwhile, FETs incorporating thick 2D PdSe₂ layers exhibit completely distinct characteristics, as presented in Figure 2c,d. For example, Figure 2c provides I_{ds} – V_{ds} plots of a FET employing 2D PdSe₂

layers prepared with Pd thickness of 7.4 nm, revealing negligible gate responses with varying V_g . Figure 2d presents the corresponding FET transfer curve of I_{ds} vs V_g , which further confirms that the FET employing thick 2D PdSe₂ layers exhibits metallic characteristics without noticeable gate responses. For an accurate assessment of thickness-variant

FET characteristics, we fabricated various 2D PdSe₂ layers-based FETs by systematically modulating their thickness using identical fabrication conditions; i.e., direct selenization of Pd films prepatterned by identical shadow masks. Figure 2e shows a plot of I_{ds} ratios measured at $V_g = \pm 60$ V for FETs employing 2D PdSe₂ layers of various thickness, prepared in identical fabrication batches. An abrupt increase of I_{ds} ratios is observed at Pd thickness of ~ 3 nm which corresponds to ~ 7.5 nm thick 2D PdSe₂ layers, while the ratios nearly saturate to unity beyond the thickness. In fact, thicker 2D PdSe₂ layers prepared with Pd thickness of slightly larger than 3 nm (e.g., 5.8 nm) exhibit much relaxed *p*-type semiconducting characteristics accompanying a reduced mobility of ~ 0.77 cm²/V·s, as presented in Supporting Information, Figure S2. This observation confirms a prominent and drastic onset of thickness-dependent semiconducting-to-metallic transitions in wafer-scale 2D PdSe₂ layers. In order to gain more insights about the semiconducting characteristics observed with small Pd thickness and their device preparation dependency, we also fabricated FETs employing semiconducting 2D PdSe₂ layers of various channel lengths. The fabrication was performed by e-beam lithography patterning techniques and a representative image of an array of fabricated FETs is presented in Figure 2f. The array contains a number of FETs with varying channel lengths; i.e., 3, 5, 7, and 10 μ m, and the inset shows an image of a 10 μ m-channel FET. Figure 2g shows I_{ds} – V_g FET transfer curves with varying channel lengths along with their corresponding mobility values, revealing strong *p*-type gate responses. A maximum hole mobility of 2.36 cm²/V·s is observed at a channel length of 3 μ m, and this mobility value is similar to those of FETs fabricated by the direct patterned growth of 2D PdSe₂ layers with shadow masks (Figure 2b). Figure 2h presents V_g -dependent I_{ds} – V_{ds} curves corresponding to the 3 μ m channel FET, further confirming its strong semiconducting characteristics. Figure 2i presents a correlation of mobility value vs channel length, clarifying that FETs with shorter channels yield higher mobilities.

Application opportunities of the thickness-modulated semiconducting-to-metallic transition characteristics were explored by a scalable and monolithic fabrication of all-2D patterned arrays; i.e., flexible devices employing thin (thick) semiconducting (metallic) 2D PdSe₂ layer channels (electrodes) in a single platform. Figure 3a illustrates a schematic of the proposed all-2D flexible device composed of thin/thick PdSe₂ layer arrays, highlighting their atomically sharp interfaces. The device is fabricated on a polymeric polyamide (PI) substrate via a direct CVD growth of 2D PdSe₂ layers on it, enabled by the low reaction temperature of 330 °C. Figure 3b shows a representative image of thin/thick Pd patterned arrays sequentially prepared on a PI substrate by a stencil printing technique using a shadow mask. Details about the stencil printing process are described in Supporting Information, Figure S3. Figure 3c displays images of isolated patterned arrays of thin (2.1 nm Pd)/thick (7.4 nm Pd) PdSe₂ layers, obtained from a direct CVD tellurization of the sample in Figure 2h. Figure 3d demonstrates an excellent mechanical bendability of this all-2D PdSe₂ layers-based device. Figure 3e presents Raman spectra obtained from the same sample revealing nearly identical characteristics in both thin/semiconducting and thick/metallic regions. This observation confirms the monolithic and spatially localized growth of thickness-modulated 2D PdSe₂ layers even on flexible PI substrates. Figure 3f shows a current–voltage (I – V) plot of the

same sample, revealing a formation of highly Ohmic contacts at the interfaces of thin/semiconducting layers and thick/metallic layers. Figure 3g showcases a photoresponsiveness of this flexible device under continuous 10 s illuminations at three different wavelengths of 405, 625, and 940 nm. The significant increase of photocurrents measured at a bias of 0.5 V confirms that the semiconducting 2D PdSe₂ layer channels efficiently generate electron–hole pairs which are collected by the metallic 2D PdSe₂ layer electrodes. Figure 3h presents a photoresponsiveness obtained from a periodically applied optical pulses with 0.5 s intervals. The photocurrents are observed to steadily increase during the illumination periods of total 10 s while they slowly decay once the illuminations are terminated. This observation indicates that the device exhibits characteristics of optically modulated synaptic plasticity which is strongly dependent on illumination frequencies, as observed in our previous studies^{34,35}. These synaptic characteristics are observed at a broad spectrum of visible-to-near-infrared (NIR), i.e., ranging from 405 to 625 and 940 nm (zoom-in view), indicating the device's intrinsic broadband responsiveness.

Beyond establishing the transition characteristics by the physical thickness modulation, we explored an anion exchange-based chemical method of introducing semiconducting-to-metallic transitions in 2D PdSe₂ layers. Thin semiconducting 2D PdSe₂ layers initially prepared with 2.1 nm Pd thickness were directly tellurized and completely converted to 2D PdTe₂ layers, as described in Figure 1a. Figure 4a shows photographs of three independently prepared samples of as-grown 2D PdSe₂ and PdTe₂ as well as converted-PdTe₂ (c-PdTe₂) layers. X-ray photoelectron spectroscopy (XPS) characterizations were performed on these samples with a major emphasis on identifying the chemical structure of c-PdTe₂ to unveil the Se-to-Te anion exchange efficacy. Figure 4b shows XPS core-level spectra of Pd 3d and Se 3d obtained from as-grown 2D PdSe₂ layers, revealing binding energy peaks consistent with earlier studies.²⁷ Figure 4c shows XPS core-level spectra of Pd 3d and Te 3d obtained from separately prepared 2D PdTe₂ layers whose peak characteristics are highly consistent with previous observations.³⁶ Figure 4d presents XPS core-level spectra of Pd 3d and Te 3d corresponding to the initial sample of PdSe₂ in Figure 4b after its subsequent conversion to c-PdTe₂. Interestingly, the XPS characteristics of c-PdTe₂ are exactly identical to those of as-grown PdTe₂ in Figure 4c, which indicates a Se-to-Te exchange-driven complete conversion of PdSe₂-to-PdTe₂. Specifically, the Se 3d peaks observed at the binding energy of 60-to-52 eV range in Figure 4b is observed to completely disappear, as clarified in the inset plot of Figure 4d right. Furthermore, Raman spectroscopy characterizations were performed to further confirm the anion exchange conversion of PdSe₂-to-PdTe₂. Figure 4e presents a Raman spectrum of the as-grown PdSe₂ sample corresponding to Figure 4b with well-resolved A_g and B_g characteristic peaks. Figure 4f presents a Raman spectrum of the as-grown PdTe₂ sample corresponding to Figure 4c, revealing peaks at 75 and 133 cm^{−1} associated with in-plane E_g and out-of-plane A_{1g} vibration modes of PdTe₂, respectively, consistent with previous observations.³⁷ Figure 4g displays a Raman spectrum of the c-PdTe₂ sample converted from PdSe₂, which exhibits exactly identical characteristics to those of Figure 4f. In fact, all the peaks observed with as-grown 2D PdSe₂ layers in Figure 4e are no longer present in Figure 4g, further supporting the complete conversion of PdSe₂-to-PdTe₂. Figure 4h presents Raman spectra obtained from multiple samples of c-PdTe₂

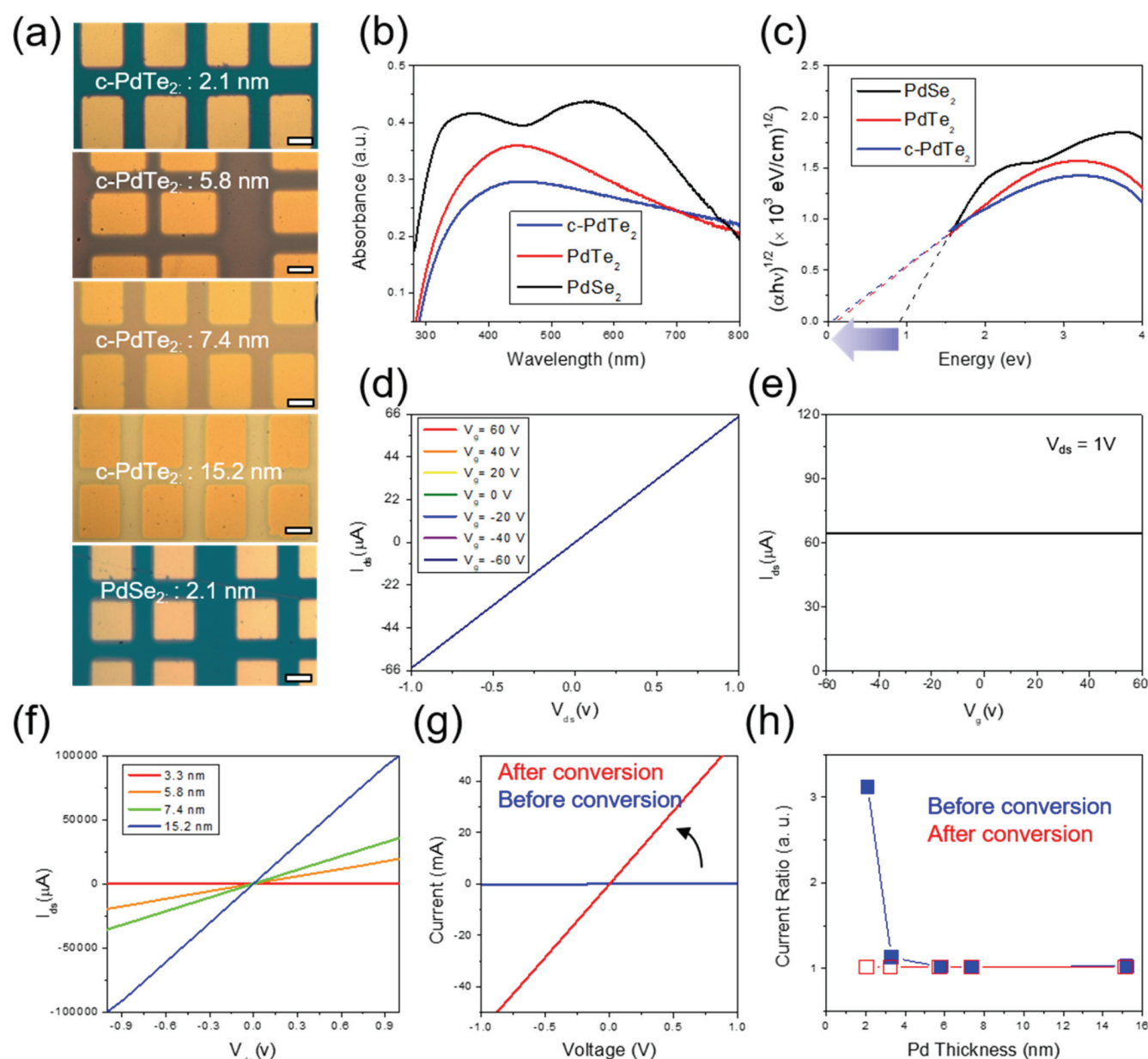


Figure 5. Semiconducting-to-metallic transition associated with conversion of 2D PdSe₂ layers to 2D PdTe₂ layers. (a) Optical microscopy images of Au electrodes-patterned c-PdTe₂ layers prepared with various Pd thickness as well as as-prepared PdSe₂ layers. The scale bars in all images are 100 μm . (b, c) Optical property comparison of as-prepared PdSe₂ and PdTe₂ as well as c-PdTe₂ layers characterized by (b) UV-vis absorbance, and (c) Tauc plots. (d) $I_{\text{ds}}-V_{\text{ds}}$ curves obtained from a FET employing c-PdTe₂ layers converted from thin PdSe₂ layers (Pd thickness = 2.1 nm). (e) $I_{\text{ds}}-V_{\text{g}}$ curve obtained from the same FET in (d) at $V_{\text{ds}} = 1$ V. (f) Comparison of $I_{\text{ds}}-V_{\text{ds}}$ curves obtained from c-PdTe₂ FETs with varying Pd thicknesses at $V_{\text{g}} = 0$ V. (g) Comparison of two-terminal $I-V$ characteristics for 2D PdSe₂ layers before/after their conversion. (h) Comparison of I_{ds} ratios at $V_{\text{g}} = \pm 60$ obtained from FETs employing as-prepared PdSe₂ (blue) vs c-PdTe₂ (red) layers as a function of Pd thickness.

prepared with various Pd thickness. The identical peak characteristics irrespective of Pd thickness variations support the highly homogeneous nature of the conversion process which involves minimal sample-to-sample variations. It is noteworthy that similar anion exchange-based conversions have been demonstrated in Pt-based 2D and 3D materials.^{34,38}

Possible transitions of the electrical and/or optical properties of 2D PdSe₂ layers associated with their anion exchange-driven conversion were inspected by FET and spectroscopic measurements. Figure 5a shows a series of optical microscopy images of gold (Au) top electrodes-patterned c-PdTe₂ samples

prepared with various Pd thickness fabricated for electrical measurements. Highly homogeneous color (thus, uniform morphology) and its progressive change are observed, which is also compared to the color of as-prepared 2D PdSe₂ layers before their conversion (bottom image). Energy band structures of samples before/after the conversion were inspected and compared by ultraviolet (UV)-visible spectroscopy. Figure 5b presents UV-visible absorbance spectra of samples in three different states of pristine 2D PdSe₂ and PdTe₂ as well as c-PdTe₂ layers. The optical absorbance of the PdSe₂ sample is observed to be higher than those of both

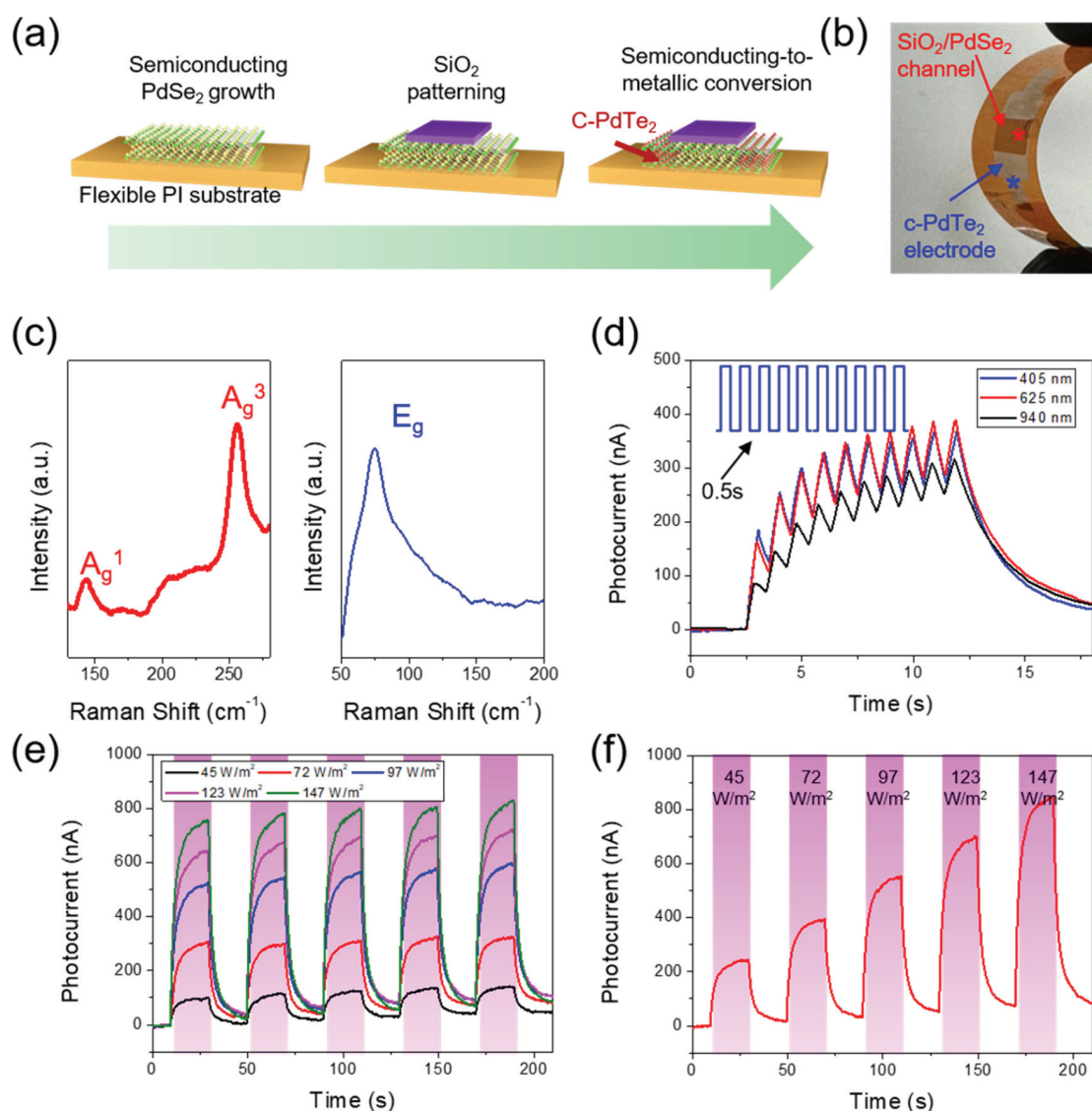


Figure 6. Application of anion exchange-driven semiconducting-to-metallic transition for all-2D PdSe₂ layers-based flexible devices. (a) Schematics to illustrate fabrication procedures for all-2D PdSe₂/c-PdTe₂ in-plane heterojunction device employing site-specific anion exchange reaction. (b) Image of all-2D flexible device composed of SiO₂/PdSe₂ channel interfaced with c-PdTe₂ electrodes. (c) Raman spectra obtained from the red and blue marks in Figure (b), revealing PdSe₂ (left) and PdTe₂ (right) characteristics, respectively. (d) Temporal plot of broadband synaptic plasticity under optical pulse illuminations with 0.5 s intervals. (e) Temporal plots of photoresponsiveness with long 20 s illumination intervals and varying intensities. (f) Illumination intensity-dependent photoresponsiveness.

PdTe₂ and c-PdTe₂ samples and is in good agreement with earlier studies on 2D PdSe₂ layers fabricated differently.³⁴ Furthermore, Tauc plots are extracted from the absorbance spectra, which yields bandgap energies of the three samples.³⁴ Figure 5c presents the corresponding Tauc plots of energy vs $(\alpha h\nu)^{0.5}$, where α represents the absorption coefficient, h is Planck's constant, and ν is the velocity of light. Bandgap energies are determined by extrapolating the linear tangents to the plots at the intercepts of the x -axis. An indirect bandgap value of ~ 0.7 eV is obtained for the PdSe₂ sample confirming its semiconducting nature, consistent with previous studies.^{9,24,27} Meanwhile, both the PdTe₂ and c-PdTe₂ samples exhibit nearly negligible bandgap energies, indicating their metallic properties. Particularly, it is interesting to note that the c-PdTe₂ sample was converted from thin semiconducting 2D PdSe₂ layers, which indicates that the anion exchange conversion leads to notable semiconducting-to-metallic tran-

sitions. These chemically driven transition characteristics were also characterized by FET measurements. Figure 5d presents I_{ds} - V_{ds} plots of a c-PdTe₂-based FET, which reveals metallic transports of V_g -independent negligible gate responses. The results are interesting given that the c-PdTe₂ FET channel was converted from thin semiconducting 2D PdSe₂ layers, highly consistent with optical characterizations in Figure 5c. Figure 5e shows the corresponding I_{ds} - V_g FET transfer curve, which further supports the metallic nature of the c-PdTe₂ converted from semiconducting 2D PdSe₂ layers. Various FET I_{ds} - V_g curves of c-PdTe₂-based FETs prepared with different Pd thickness are presented in Supporting Information, Figure S4. Figure 5f presents a comparison of I_{ds} - V_{ds} curves for c-PdTe₂ FETs converted from 2D PdSe₂ layers prepared with various Pd thicknesses, measured at $V_g = 0$ V. A steady increase in I_{ds} is observed with increasing Pd thickness, while the conductance values of c-PdTe₂ FETs are much higher than those observed

before the conversion; for example, typically >100 times conductance increase before vs after conversion. In fact, Figure 5g compares two-terminal I – V characteristics of an identical 2D PdSe₂ layers-based device before/after their conversion, revealing a conductance increase from 1.46×10^4 S/m (before; blue line) to 1.68×10^4 S/m (after; red line). Figure 5h compares plots of I_{ds} ratios measured at $V_g = \pm 60$ V for FETs employing 2D PdSe₂ layers of various thickness before/after their conversion. It is noted that the thickness-dependent onset of the semiconducting-to-metallic transitions in 2D PdSe₂ layers at ~ 3 nm Pd thickness no longer appears after their conversion to c-PdTe₂. Additionally, TEM-SAED analysis conducted on an identical sample of 2D PdSe₂ layers before/after the conversion confirms a preservation of their polycrystalline structures associated with the electrical transitions (Supporting Information, Figure S5). These comprehensive optical and electrical characterizations strongly support that 2D PdSe₂ layers undergo semiconducting-to-metallic transitions enabled by the Se-to-Te anion exchange. This chemistry-driven approach offers another degree of material property tunability in addition to the intrinsic physical thickness-modulated transitions, vastly broadening the applicability of wafer-scale 2D PdSe₂ layers in digital electronics and/or optoelectronics.

Similar to the demonstration of all-2D flexible devices by their thickness control in Figure 3, we also employed the anion exchange-driven conversion process to fabricate all-2D PdSe₂/c-PdTe₂ lateral heterojunction flexible devices; i.e., semiconducting PdSe₂ channels are seamlessly interfaced with metallic c-PdTe₂ electrodes. Figure 6a illustrates the fabrication process of all-2D PdSe₂/c-PdTe₂ flexible devices, which begins with growing semiconducting 2D PdSe₂ layers directly on flexible PI substrates. Subsequently, SiO₂ is selectively patterned and deposited on the pregrown PdSe₂, serving as a protective layer for the underlying semiconducting channel. A subsequent CVD tellurization reaction converts the 2D PdSe₂ layers exposed outside of the SiO₂ protection layer to metallic c-PdTe₂ layers. Figure 6b displays a photograph of an all-2D flexible device composed of a SiO₂/PdSe₂ channel laterally interfaced with c-PdTe₂ electrodes subjected to a mechanical bending. Figure 6c shows the Raman spectra corresponding to Figure 6b, with the spectra taken from the SiO₂/PdSe₂ channel region (left) and the c-PdTe₂ electrode regions (right). Distinct Raman peaks are observed in the channel vs electrode regions, consistent with spectral characteristics of 2D PdSe₂³¹ and 2D PdTe₂³⁷ layers, respectively. This Raman analysis verifies that the deposited-SiO₂ layer efficiently protects its underlying 2D PdSe₂ layers against the subsequent tellurization reaction, while the exposed 2D PdSe₂ layers become fully converted to 2D PdTe₂ layers. This all-2D flexible device was employed to demonstrate optical synaptic characteristics as well as standard photodetection applications under modulated optical pulse conditions. Figure 6d presents a temporal plot of the photoresponsiveness obtained from the device illuminated at three different wavelengths of 405, 625, and 940 nm, by optical pulses with short 0.5 s intervals. Similar to the observations with all-2D thin/thick PdSe₂ layers in Figure 3h, the device exhibits wavelength-independent broadband characteristics of optically introduced synaptic plasticity (i.e., optical potentiation), essential for optoelectronic artificial synapse applications.³⁵ The device was further inspected with optical illuminations accompanying much longer pulse intervals. Figure 6e presents intensity-dependent photoresponsiveness characteristics of the same device under

periodically applied 625 nm illuminations with 20 s intervals, measured at 1 V. A complete decay of the generated photocurrent is observed at each illumination cycle of 20 s, unlike the observations with much shorter intervals in Figure 6d. Figure 6f shows a temporal photoresponsiveness of the device with systematically increasing illumination intensities. These comprehensive optical measurement data confirm the semiconducting nature of 2D PdSe₂ layers capable of yielding electron–hole pairs under broadband illuminations, which are efficiently collected by seamlessly connected metallic 2D PdTe₂ layers. Additional data of intensity-dependent photoresponsiveness obtained under illuminations at three different wavelengths are also presented in Supporting Information, Figure S6. Lastly, FET characteristics of our wafer-scale CVD-grown 2D PdSe₂ layers are compared to those of previously reported CVD-2D PdSe₂ layers, and its corresponding comparison table is presented in Supporting Information, Figure S7.

CONCLUSIONS

In conclusion, we report on two independent approaches of physically or chemically introducing semiconducting-to-metallic transitions in wafer-scale 2D PdSe₂ layers grown at low temperatures. We envision that a judicious combination of these physical–chemical methods should be able to provide an excellent controllability of manipulating complex functionalities in the materials. Accordingly, this study is believed to be highly encouraging toward exploring all-2D devices adopting both metallic and semiconducting components in atomically thin forms.

METHODS

Growth of 2D PdSe₂ and PdTe₂ Layers, and Conversion of 2D PdSe₂-to-PdTe₂. Pristine 2D PdSe₂ and PdTe₂ layers were grown by CVD selenization and tellurization reactions, respectively. Initially, Pd films with various thicknesses were deposited onto SiO₂/Si (300 nm SiO₂ thickness) substrates by an electron beam evaporator (Thermionics E-beam Evaporator) at a fixed evaporation rate of 0.05 Å/s. The Pd-coated substrates were positioned in the central heating zone of a horizontal quartz tube CVD furnace (Lindberg/Blue M Mini-Mite). Alumina boats containing precursor powders (selenium: 99.9% and tellurium: 99%, Millipore Sigma) were placed upstream in the quartz tube. The system was evacuated to a base pressure of ~ 25 mTorr and was subsequently purged with Ar gas for 10 min to eliminate residual organics within the tube. The furnace was then heated at a rate of 11 °C/min to 330 °C and was held at that temperature for 60 min for both selenization and tellurization reactions. During the reactions, the furnace was supplied with a continuous Ar gas flow of ~ 150 standard cubic centimeters per minute (sccm). For the PdSe₂-to-PdTe₂ conversion, as-grown 2D PdSe₂ layers were subjected to the CVD tellurization reaction under the identical conditions as described above.

Structural, Chemical, and Optical Characterizations. HR-TEM and SAED analyses were conducted using a FEI Tecnai F30 TEM. Raman spectroscopy was performed using a Horiba LaRAM HR Evolution Nano system with a 532 nm laser source. XPS characterization was carried out using an Escalab 250Xi system. UV–visible optical absorbance spectra were acquired in transmittance mode using a UV–vis spectrophotometer (Evolution 220). For the optical characterization, 2D PdSe₂, PdTe₂, and c-PdTe₂ layers were directly grown on optically transparent willow glass substrates.

FET Fabrication and Electrical Measurements. For the fabrication of back-gated FETs, Au contacts (50 nm) were deposited onto 2D PdSe₂, PdTe₂, and c-PdTe₂ layers using shadow masks to pattern the source and drain electrodes. For the inspection of the 2D PdSe₂ channel length-dependent FET performances, a direct laser

lithography was employed to define various micrometer-scale channel lengths using a 405 nm diode laser. All FET measurements were conducted at room temperature in ambient conditions using a home-built micromanipulator probe station paired with a semiconductor parameter analyzer (HP 4156A).

Fabrication of All-2D Flexible Devices and Photoresponsiveness Measurements. All-2D flexible devices with laterally interfaced semiconducting/metallic heterostructures were fabricated on PI substrates. The first strategy employed the thickness-variant semiconducting-to-metallic transition in all-2D PdSe₂ layers. In this approach, thin/thick Pd films were prepatterned and deposited in array forms using a thermionic electron beam evaporation and shadow masks. The patterned Pd/PI arrays were subsequently selenized under the previously described CVD conditions, yielding all-2D semiconducting/metallic PdSe₂ layers. The second strategy involved the anion exchange-driven semiconducting-to-metallic transition in 2D PdSe₂ layers. Thin semiconducting 2D PdSe₂ layers were directly grown on PI substrates using the same CVD conditions described above. Subsequently, SiO₂ (70 nm thickness) protection layers were deposited over the central region of the as-grown 2D PdSe₂ layers. Then, CVD tellurization reactions were employed, converting the 2D PdSe₂ layers exposed outside of the SiO₂ layers to metallic 2D PdTe₂ layers. The reactions were performed at 330 °C for 5 min under Ar flow of 150 sccm, accompanying a ramp rate of 13.2 °C/min. For both the thickness variation and anion exchange approaches, Au contacts were deposited onto the metallic 2D layers defining source and drains. Photoresponsiveness characterizations of the all-2D flexible heterostructure devices were carried out using LED lasers at wavelengths of 405, 625, and 940 nm as well as the home-built probe station.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsnano.4c11627>.

AFM images, FET transfer curves, Fabrication details, TEM/SAED images, Photoresponsiveness, and FET comparison table (PDF)

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Author Contributions

Y.J. conceived and directed the project. A.G. prepared all samples, conducted device measurements, and performed data analyses with assistance from S.S.H. and C.Y. S.S.H. performed TEM, XPS characterizations and photoresponsiveness measurements. C.Y. performed AFM measurements. C.W.L. performed Raman characterizations. A.G. and Y.J. wrote the manuscript incorporating data and inputs from all authors.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

Y.J. acknowledges financial support from the US National Science Foundation (CAREER: 2142310). S.S.H. acknowledges financial support from the Preeminent Postdoctoral Program (P3) at UCF.

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