Wideband Digital $N-$Beam Delay-Sum Apertures at $\mathcal{O}(N)$ Complexity: Towards 64 GS/s 8-Beams on Intel Agilex-9 Direct-RF Chiplets

Sirani M. Perera ⋆
Arjuna Madanayake †
⋆ Embry-Riddle Aeronautical University, Daytona Beach, FL
Emails: pereras2@erau.edu
† Florida International University, Miami, FL
Emails: amadanay@fiu.edu

2024 IEEE International Conference on RFID Technology and Applications (RFID-TA) | 979-8-3315-4022-7/24/$31.00 ©2024 IEEE | DOI: 10.1109/RFID-TA64374.2024.10965176

***Abstract*—Formation of N simultaneous true-time delay-and-sum (DAS) RF beams from an N-element array of wideband antennas has many applications in wireless communications, electronic warfare, spectrum sensing, radar, and signals intelligence. A conventional DAS wideband beamformer scales as $\mathcal{O}(N^2)$ different individual delay line segments (i.e., the delay complexity) which makes large arrays with many antennas and wideband beams impractical. This paper introduces a method based on the factorization of the approximate DFT matrix that reduces the delay complexity from $\mathcal{O}(N^2)$ to $\mathcal{O}(N)$ which in turn makes dense aperture antenna arrays with large N elements lead to N DAS beams at significantly smaller delay line count. Each delay can be realized in DSP as a FIR filter. Therefore, a wideband N-beam system at $\mathcal{O}(N)$ delay line complexity as opposed to $\mathcal{O}(N^2)$ implies a significant reduction leading to smaller chip area and power consumption for hardware realization on a digital ASIC chip. We provide an overview of ongoing work on realizing an 8-beam DAS digital multi-beam beamformer using the state-of-the-art (SOTA) Agilex-9 Direct-RF chiplets from Intel which supports sample rates up to 64 GS/s per channel.**

***Index Terms*—full**

I. Introduction

The selective directional enhancement of a uniform plane wave based on its direction of propagation constitutes a beamforming operation. For ultrawideband plane waves contaminated by wide sense stationary additive white Gaussian noise (AWGN), the optimal beamformer takes the form of a true time delay-based delay-end-sum operation. For example, to directionally enhance a wideband wave arriving at angle ϕ measured from the broadside direction from an $N-$element linear aperture of antennas, the delay and sum operation for beamforming requires the computation of $y(t)=\sum_{k=1}^{N} x_k(t-k\tau)$ where $\tau=\frac{\Delta x}{c}\sin\phi$ and where Δx is the inter antenna distance and c is the speed of light. A single beam requires N delay elements; thus, N simultaneous beams at arbitrarily chosen angles would naturally lead to N parallel copies of the beamformer thus leading to $\mathcal{O}(N^2)$ delay elements in total. The $N\times N$ delay Vandemonde matrix (DVM) $N-$beam beamformer is a special case where each $p=1,2,...,N$ beam is realized by integer multiple delays of $\tau_p=p\tau/N^2$. The frequency responses (beam shapes) of the DVM for $N=16$ beams are shown in Fig. 1. The DVM-form of the $N-$beam wideband beamformer will be reviewed in Section II.

This effort is an extension of work done followed by the United States National Science Foundation (NSF) award numbers 2229473 and 2229471.

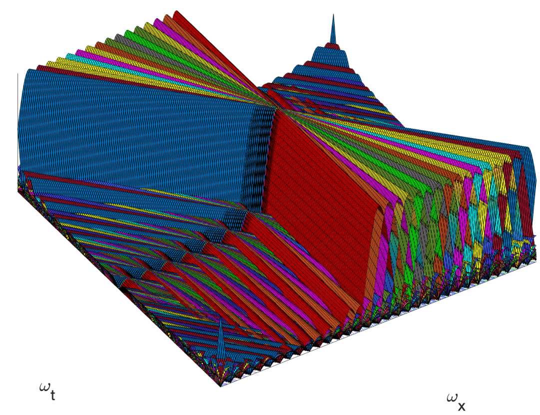

Fig. 1. DVM frequency response for $N=16$ wideband DAS beams. Each beam is fully wideband and squint free. Here, $\omega_t=2\pi f$ is the temporal frequency, and ω_x is the normalized spatial frequency. All 16 beams are shown in the same plot. Beam cross section takes the familiar *sinc* ω_x form.

The straightforward realization of $N-$beams using the DVM-vector operation leads to a parallel hardware realization that essentially uses N^2 delays. The circuit complexity associated with this multi-beam receiver/transmitter thus scales as $\mathcal{O}(N^2)$; such as "quadratic complexity" makes scaling to a large number of beams from a high valued N (dense aperture arrays) extremely challenging. To address this problem, our recent work led to a new class of DVM beamforming algorithms that factor the matrix-vector product into a sequence of sparse matrices-vector products so that the net number of delays is reduced to $\mathcal{O}(N \log N)$, where $N = 2^r (r \geq 2)$; this is the same $\frac{\log N}{N}$ factor of reduction albeit for the number of delays just like for the well-known case of applying fast Fourier transforms (FFTs) in place of direct matrix-vector operations when one is computing a discrete Fourier transform (DFT). FFTs exhibit butterfly networks in their signal flow graph representations. We refer you to our recent work [1] for a treatment of the $\mathcal{O}(N \log N)$ wideband DVM beamformers.

II. Mathematical Interpretation of $\mathcal{O}(N)$ approximate DVM N-beam Beamformer

Here, we disclose our most recent innovation: a DVM wideband multi-beam beamforming algorithm that achieves $N-$ wideband beams at linear complexity; that is, the proposed DVM beamformer requires only $\mathcal{O}(N)$ delays to realize $N-$ beams. The realized beams are within about 2 dB of the ideal DVM beams in their directional selectivity. We achieve this massive reduction by starting from the recently proposed $\mathcal{O}(N \log N)$ DVM multi-beam algorithm [1] which makes use of the exact-DFT. Here, we propose to replace the DFT in [1] with an approximate DFT instead [2]–[4]. An exact DFT can be realized at $\mathcal{O}(N \log N)$ via FFTs while the approximate DFT has a corresponding matrix sparse factorization that exhibits $\mathcal{O}(N)$ delays in DVM aggregated across its butterfly networks [2]–[4]. Therefore, even though there is a small (1.5 dB or less) loss of directional selectivity, we can achieve a massive reduction in number of true time delay (TTD) circuits while still achieving $N-$ simultaneous beams [2]–[4].

A. Construction of the Delay Vandermonde Matrix (DVM) [5]–[7]

The DVM is explicitly defined by

$$\mathbf{A}_N := [\mathbf{A}_{kl}]_N = [\alpha^{kl}]_{k=1,l=0}^{N,N-1},$$

where $N = 2^r (r \geq 1)$, $\{\alpha, \alpha^2, \ldots, \alpha^N\}$ are distinct complex nodes s.t. $\alpha = e^{-j\omega\tau}$, $j^2 = -1$, ω is the temporal frequency, and τ is the delay. The scaled DVM, i.e., scaling w.r.t. a diagonal matrix, is defined as

$$\widetilde{\mathbf{A}}_N := [\widetilde{\mathbf{A}}_{kl}]_N = [\alpha^{kl}]_{k,l=0}^{N-1}.$$

The coefficient α^{kl} is a temporal Fourier transform of a pure time-delay of duration τ. The signal $x(t)$ with Fourier transform $X(\omega)$ is related to the delayed version of the signal $x(t - p\tau)$ via the relationship $X(\omega)e^{-jp\omega\tau}$. So the corresponding phase rotation of $X(\omega)$ is simply $\alpha^p = e^{-j\omega p\tau}$. Crucially, the DVM contains closed-form complex functions of ω given as complex phase rotations in integer powers p of α. That is, α^p are not numerical values; they are complex functions of frequency ω raised to power p. So an $N \times N$ DVM containing powers of α *looks like a matrix-vector product* but remember, we are in the temporal Fourier domain; so this is defined $\mathcal{O}(N^2)$ number of delay-and-sum dot product, not the usual $\mathcal{O}(N^2)$ number of multiply-and-sum dot product.

B. Review of DVM vs DFT, and FFT Algorithms

There are several mathematical techniques available to derive radix-2 and split-radix FFT algorithms, as described in [1], [8]–[14]. Even though the derivation of size-N DFT into two size-$\frac{N}{2}$ DFTs can be done easily, the extension of this idea to the DVM is cumbersome because the useful DFT matrix properties, like periodicity and unitary, are **not** present in the DVM [1], [5]. Consequently, considering these mathematical properties and the representation of DVM elements through TTD wideband multi-beam—unlike the narrowband representation characterized by the FFT-beams—it becomes evident that DVM serves as a superclass of DFT matrices.

Our previous work introduced various DVM algorithms designed to accurately compute the exact DVM-vector product for both narrowband and wideband communication systems. Our latest study [1] presents a derivation of the DVM algorithm, successfully reducing the complexity of RF N-beam analog beamforming systems from $\mathcal{O}(N^2)$ to $\mathcal{O}(N \log N)$. While the DVM algorithms proposed in [5], [7] show greater efficiency compared to brute-force matrix-vector calculations, their arithmetic complexity remains substantially higher than $\mathcal{O}(N \log N)$ [1]. On the other hand, our work in [6] focuses on numerically stable DVM algorithms with complexity of $\mathcal{O}(N \log N)$ that apply to Vandermonde matrices with nodes positioned on the unit circle (not exclusively at the roots of unity) and also on circles with their center at the origin and a radius exceeding one. Unlike the DVM algorithms highlighted in [5]–[7], which are specifically designed for narrowband communication systems, the radix-2 DVM algorithm presented in [1] is tailored for TTD wideband communication systems.

With these said, we introduce sparse factors to compute an approximate DVM (ADVM) using approximate DFT to reduce delay complexity from quadratic to linear. Before stating the factorization formula for the approximate DVM, we state the factorization leading $\mathcal{O}(N \log N)$ DVM algorithm as follows.

C. Review of DVM factorization [1]

The scaled DVM factorization resulting in an $\mathcal{O}(N \log N)$ DVM algorithm is presented in [1], and it executes based on the DVM factorization defined below

$$\tilde{\mathbf{A}}_N = \hat{\mathbf{D}}_N [\mathbf{J}_{M \times N}]^T \mathbf{F}_M^* \breve{\mathbf{D}}_M \mathbf{F}_M \mathbf{J}_{M \times N} \hat{\mathbf{D}}_N,$$

where $M = 2N$, $\mathbf{J}_{M \times N} = \begin{bmatrix} \mathbf{I}_N \\ \hline \mathbf{0}_N \end{bmatrix}$ is a highly sparse matrix containing the identity matrix $\mathbf{I}_N$ and the zero matrix $\mathbf{0}_N$, ^{T} denotes the transpose of matrices. The matrices $\mathbf{D}_N = \text{diag}[\alpha^k]_{k=0}^{N-1}$, $\hat{\mathbf{D}}_N = \text{diag}\left[\alpha^{\frac{k^2}{2}}\right]_{k=0}^{N-1}$ and $\breve{\mathbf{D}}_M = \text{diag}\left[\tilde{\mathbf{F}}_M \mathbf{c}\right]$ are diagonal matrices, and a circulant matrix $\mathbf{C}_M := \mathbf{F}_M^* \breve{\mathbf{D}}_M \mathbf{F}_M$, which is defined by the first column $\mathbf{c}$ s.t. $\mathbf{c} = \left[1, \alpha^{-\frac{1}{2}}, \cdots, \alpha^{-\frac{(N-1)^2}{2}}, 1, \alpha^{-\frac{(N-1)^2}{2}}, \alpha^{-\frac{(N-2)^2}{2}}, \cdots, \alpha^{-\frac{1}{2}}\right]^T$. The DFT matrix is defined by $\mathbf{F}_N = \frac{1}{\sqrt{N}} [w_N^{kl}]_{k,l=0}^{N-1}$, having the primitive N^{th} roots of unity $w_N = e^{-\frac{2\pi j}{N}}$ as the nodes of the DFT matrix. The scaled DFT matrix is denoted by $\tilde{\mathbf{F}}_N = \sqrt{N}\,\mathbf{F}_N$.

Remark 2.1: It is important to highlight that the $\mathcal{O}(N \log N)$ DVM algorithm in [1] executes recursively utilizing the well-known FFTs in [8], [9].

Following the discussion on implementing the DVM algorithm using the FFT, we would like to explicitly refer the reader to papers [15], [16] to compute multiplierless approximated 16-point and 32-point DFT matrices having a product of highly sparse matrices. The approximate DFT factorization is then embedded into the DVM algorithm in [1] to reduce the complexity of computing the DVM-vector product, reducing it from $\mathcal{O}(N^2)$ to $\mathcal{O}(N)$.

D. Proposed ADVM-Factorization for $\mathcal{O}(N)$ DVM Algorithm

Building on the DVM factorization [1] and multiplierless approximate DFT factorization [15], [16], we state a factorization to approximate DVM. For a comprehensive understanding and in-depth algorithmic interpretation, we refer readers to [17].

Proposition 2.2: [from [17]] Let the scaled DVM $\widetilde{\mathbf{A}}_N = [\alpha^{kl}]_{k,l=0}^{N-1}$ be defined by nodes $\{1, \alpha, \alpha^2, \ldots, \alpha^{N-1}\} \in \mathbb{C}$, $N = 2^r (r \geq 3)$, and $M = 2N$. Then, an approximation for the scaled DVM denoted as $\widehat{\mathbf{A}}_N$ by vector $\mathbf{x} \in \mathbb{R}^{\aleph}$ or $\mathbb{C}^n$, i.e., $\mathbf{y} = \widehat{\mathbf{A}}_N \mathbf{x}$ can be computed through the following:

$$\mathbf{y} = \widehat{\mathbf{A}}_N \mathbf{x} = \hat{\mathbf{D}}_N [\mathbf{J}_{M \times N}]^T \widehat{\mathbf{F}}_M^* \breve{\mathbf{D}}_M \widehat{\mathbf{F}}_M \mathbf{J}_{M \times N} \hat{\mathbf{D}}_N \mathbf{x}, \qquad (1)$$

where $\widehat{\mathbf{F}}_N$ is the approximate DFT matrix.

Remark 2.3: Let us assume that we had utilized multiplierless approximated DFT matrices in computing the approximated scaled DVM-vector product in Proposition 2.2, then the explicit delay complexity in computing the scaled DVM-vector product is $4N - 2$, which intern has $\mathcal{O}(N)$ complexity.

Furthermore, by following the multiplierless 16-point and 32-point DFT algorithms in [15], [16], we could explicitly compute the approximated scaled DVM-vector product with $6N-6$, $8N-14$, and $10N-30$ when $N = 32, 64, 128$. Thus, by following a series of complexity counts, we could state that the proposed approximated scaled DVM-vector product has the linear order, i.e. multiplication complexity of $\mathcal{O}(N)$ as opposed to the FFT-like $\mathcal{O}(N \log N)$ complexity algorithms, for $N = 16$ to 1024 [17]. On the other hand, we note that the proposed DVM-vector product calculates an approximated DVM algorithm as opposed to the exact DVM algorithms in [1], [5]–[7], but with $\mathcal{O}(N)$ complexity.

III. Proposed DVM Beamforming Receiver

A. RF Front-Ends

The wideband low-noise amplifiers (LNAs) and Vivaldi antennas must cover the frequency span of up to 32 GHz as this is a direct-digital architecture. Design of such components can be difficult and procurement very expensive. For example, the LNA ZVA-0.5W303GX+ from MiniCircuits cover up to 30 GHz, with gain of and noise figure 4.2 dB, can be used as

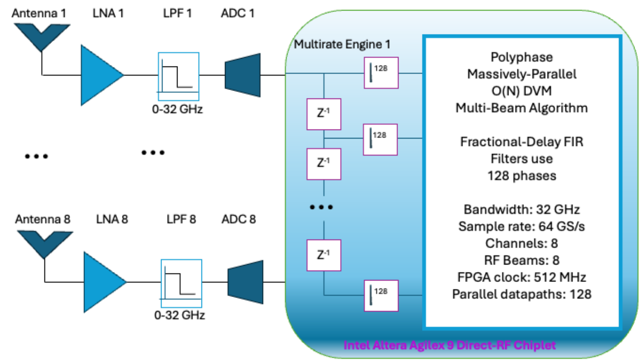

Fig. 2. The envisaged 8-channel 0-32 GHz $\mathcal{O}(N)$ wideband direct-digital DVM beamformer using Intel Altera Agilex 9 Direct-RF chiplet technology.

a transmit device. Similarly, MiniCircuits LVA-273PN-DG+ has frequency response up to 26.5 GHz, noise figure of about 10 dB, and gain of around 18 dB. The design of the front-end with up to 8 such amplifiers requires further study as these amplifiers cost several thousand dollars per unit and therefore careful optimized and cost-minimum design is a crucial requirement.

B. Wideband Data Conversion

The signals of interest are assumed to be of immense bandwidth, typically in the order of $F_s/2 = B = 32$ GHz per channel. Sampling such wideband signals requires special circuitry as a single analog-to-digital converter (ADC) typically would not be able to sample, hold, and quantize such bandwidth at reasonable levels of precision and power consumption. We assume a time-interleave ADC with P parallel time-interleaved ADC sub-circuits. Each of these P sub-ADCs is further assumed to undergo temporal decimation by factor L such that the total number of parallel digital channels on the digital signal processor (DSP) would be PL and the digital clock period would be $F_{Clk} = \frac{F_s}{PL}$. For example, assuming a channel bandwidth of 32 GHz and a Nyquist rate of $F_s = 64$ GS/s, and a $P = 16$ phase time-interleaved ADC, each sub-ADC will be sampling at 4 GS/s, with the DSP operating at $F_{Clk} = 256$ MHz for a temporal decimation factor of $L = 16$.

C. Digital Delay Filters

The digital delays operate within the field programmable gate array (FPGA) or application specific integrated circuit (ASIC) fabric at a sample rate of F_{Clk} MHz, over PL parallel channels that make up the multirate-DSP core that must finally realize any fractional delays or dot-products that are needed for the realization of the matrix analysis required in DVM wideband beamforming in real-time. The basic principle is as follows: let τ_u be a fractional delay filter, which implies $0 \leq \tau_u < 1$ with reference to the full-scale clock F_s GHz. A delay τ_u causes a phase rotation in the frequency domain $exp(-j\omega\tau_u)$ where ω is the normalized frequency variable with reference to the master sample rate F_s GHz.

An M-th order finite impulse response (FIR) can be designed and realized as a multirate filter to achieve the necessary fractional time sample delays. Typically, multiplications are directly correlated to filter order M that is required for the FIR filter for high bandwidth and precise operation therein causing FIR delays to be a major factor for complexity in multi-beam systems. In our hypothetical design, with $PL = 256$ we may assume $M = 16$ for a reasonable reference design. The block-wise computation of the order-M FIR fractional delay filter (an interpolation operation between integer multiples of the clock at frequency F_s) can be realized as a matrix-vector product of the form $y = \mathbf{T}x$ where $\mathbf{T}$ is a banded Toeplitz matrix.

The structure of the banded Toeplitz matrix lends itself well for FFT-based computation and can be realized using the maximally-decimated uniform-DFT polyphase filterbank approach to efficient FIR filter realization. Here, the number of phases is $PL = 256$ thus leading to a massively parallel digital architecture.

D. Wideband Digital FPGA Platforms

In the past, fully-digital realizations of wideband beamforming networks that operate over multi-GH bandwidths have been only a dream due to the lack of ADC/DAC and fast DSP technologies. However, the most recent innovations from Intel Corporation, namely the Series 9 Direct-RF Agilex system on chip (SoC) using multi-chiplets packaged together offers exciting possibilities for multi-beam wideband DVM beamformers that span the legacy bands up to 7 GHz (FR1), and upper mid-band (7-24 GHz) and frequency range two (24-32 GHz) in a single antenna system and DSP platform. Our proposed low-complexity $\mathcal{O}(N)$ linear delay-complexity digital DVM algorithm is a key enabler that when coupled with the latest Direct-RF chiplets leads to a new realm of possibilities for fully digital broadband antenna aperture arrays. The Series 9 Agilex Direct-RF chiplets offer 8 ADCs, 8 DACs, and a field programmable gate array (FPGA) device on the same package, where each DAC/DAC can operate up to 64 GS/s (bandwidth of 32 GHz).

IV. Conclusions

The paper presents our innovative, patent-pending algorithm for low-complexity true time delay DAS multi-beam beamforming, which is based on delay Vandermonde matrices. The proposed DVM factorization significantly enhances efficiency by reducing the complexity of computing the DVM-vector product from $\mathcal{O}(N^2)$ to $\mathcal{O}(N)$. This significant reduction in computational complexity allows us to develop an algorithm for TTD wideband multi-beam beamformers enabling approximating DVM with $\mathcal{O}(N)$ complexity, streamlining the process and improving performance. The algorithm uses only $\mathcal{O}(N)$ delay lines, which is a linear complexity system, as opposed to traditional multi-beam wideband beamformers that have $\mathcal{O}(N^2)$ which is quadratic in delay complexity. A brief overview of our ongoing work with fully digital multi-beam beamformers that use the state-of-the-art (SOTA) chiplets from Intel Altera was provided. No real-world realization has been attempted thus far due to lack of resources. However, the authors are working towards an experimental realization.

References

[1] S. M. Perera, L. Lingsch, A. Madanayake, S. Mandal, and N. Mastronardi, "A fast dvm algorithm for wideband time-delay multi-beam beamformers," *IEEE Transactions on Signal Processing*, vol. 70, pp. 5913–5925, 2022.

[2] A. Madanayake, K. Lawrance, B. U. Kumarasiri, S. Sivasankar, T. Gunaratne, C. U. S. Edussooriya, and R. J. Cintra, "Design of multichannel spectrum intelligence systems using approximate discrete fourier transform algorithm for antenna array-based spectrum perception applications," *Algorithms*, vol. 17, no. 8, 2024. [Online]. Available: https://www.mdpi.com/1999-4893/17/8/338

[3] A. Madanayake, R. J. Cintra, N. Akram, V. Ariyarathna, S. Mandal, V. A. Coutinho, F. M. Bayer, D. Coelho, and T. S. Rappaport, "Fast radix-32 approximate dfts for 1024-beam digital rf beamforming," *IEEE Access*, vol. 8, pp. 96 613–96 627, 2020.

[4] A. Madanayake, V. Ariyarathna, S. Madishetty, S. Pulipati, R. J. Cintra, D. Coelho, R. Oliviera, F. M. Bayer, L. Belostotski, S. Mandal, and T. S. Rappaport, "Towards a low-swap 1024-beam digital array: A 32-beam subsystem at 5.8 ghz," *IEEE Transactions on Antennas and Propagation*, vol. 68, no. 2, pp. 900–912, 2020.

[5] S. M. Perera, V. Ariyarathna, N. Udayanga, A. Madanayake, G. Wu, L. Belostotski, R. Cintra, and T. Rappaport, "Wideband n-beam arrays with low-complexity algorithms and mixed-signal integrated circuits," *IEEE Journal of Selected Topics in Signal Processing*, vol. 12, no. 2, pp. 368–382, 2018.

[6] S. M. Perera, A. Madanayake, and R. Cintra, "Efficient and self-recursive delay vandermonde algorithm for multi-beam antenna arrays," *IEEE Open Journal of Signal Processing*, vol. 1, no. 1, pp. 64–76, 2020.

[7] ——, "Radix-2 self-recursive algorithms for vandermonde-type matrices and true-time-delay multi-beam antenna arrays," *IEEE Access*, vol. 8, pp. 25 498–25 508, 2020.

[8] J. W. Cooley and J. W. Tukey, "An algorithm for the machine calculation of complex fourier series," *Math. Comp.*, vol. 19, pp. 297–301, 1965.

[9] R. Yavne, "An economical method for calculating the discrete fourier transform," in *in Proc. AFIPS Fall Joint Computer Conf. 33*, 1968, pp. 115–125.

[10] G. Strang, *Introduction to Applied Mathematics*. USA: Wesley-Cambridge Press, 1986.

[11] C. V. Loan, *Computational Frameworks for the Fast Fourier Transform*. Philadelphia, USA: SIAM Publications, 1992.

[12] S. G. Johnson and F. M., "A modified split-radix fft with fewer arithmetic operations," *IEEE Trans.*, vol. 55, no. 1, p. 111–119, 2007.

[13] K. R. Rao, D. Kim, and J. J. Hwang, *Fast Fourier Transform: Algorithm and Applications*. New York, USA: Springer, 2010.

[14] R. E. Blahut, *Fast Algorithms for Signal Processing*. Cambridge University Press, 2010. [Online]. Available: https://api.semanticscholar.org/CorpusID:53846853

[15] V. Ariyarathna, D. F. G. Coelho, S. Pulipati, R. J. Cintra, F. M. Bayer, V. S. Dimitrov, and A. Madanayake, "Multibeam digital array receiver using a 16-point multiplierless dft approximation," *IEEE Transactions on Antennas and Propagation*, vol. 67, no. 2, pp. 925–933, 2019.

[16] A. Madanayake, S. Mandal, T. T. S. Rappaport, V. Ariyarathna, S. Madishetty, S. K. Pulipati, R. J. Cintra, D. F. G. Coelho, R. Oliviera, F. M. Bayer, and L. Belostotski, "Towards a low-swap 1024-beam digital array: A 32-beam subsystem at 5.8 ghz," *IEEE Transactions on Antennas and Propagation*, vol. 68, pp. 900–912, 2020. [Online]. Available: https://api.semanticscholar.org/CorpusID:203035738

[17] S. M. Perera, L. Lingsch, A. Tuztas, and A. Madanayake, "Linear order approximate-dvm algorithm for true time-delay multi-beam beamforming," *in review, IEEE Transactions on Signal Processing*, 2024.