Algorithmic Design and Optimization of On-Chip Multilayered Pixelated Passive Networks

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***Abstract*—Various methods of applying algorithmic design techniques to on-chip RF and mm-Wave passive structures are shown. Multiple metal and via layers are considered to explore an expanded design space compared to single-layer structures to achieve a superior performance within smaller area footprints. Furthermore, the inherent stochasticity of metaheuristic algorithms combined with the highly nonconvex optimization landscape is exploited to diversify designs and generate multiple layouts with near-identical performance, with potential applications involving hardware obfuscation and design diversification. Finally, a method is introduced to apply algorithmic techniques to shrink the physical sizes of pixelated layouts with minimal loss in performance, adding another dimension to the hardware diversification capabilities of algorithmic design techniques.**

***Index Terms*—Algorithmic passive design, design diversification, layout shrinking algorithms, on-chip power combiners, passive bandpass filters (BPFs), pixelated passive devices.**

I. Introduction

PASSIVE networks play a critical role in radio frequency integrated circuits (RFICs) by enabling transistors to operate at high frequencies, facilitating the design of wireless transceivers for various communication and sensing applications. Traditional on-chip passive network design, shown in Fig. 1(a), typically starts with a well-known parameterized template (e.g., a circuit topology) from literature or a custom topology derived from the designer's expertise. At RF and mm-wave frequencies, component coupling and unavoidable layout parasitics, such as those from pads and interconnects, necessitate full-layout electromagnetic (EM) simulations for both design and optimization. Multiple simulations are usually required to tune performance within the design space. If target specifications remain unmet, the designer must adopt a revised or entirely new topology. This process is labor-intensive and heavily reliant on experience, intuition, and domain knowledge.

With widespread availability of modern computational resources and advances in computational algorithms, algorithmic design techniques [Fig. 1(b)] have gained significant traction. In such approaches, an optimization algorithm autonomously constructs the metal and dielectric geometries of an EM structure to meet target specifications, removing human designers from the design loop. By formulating the problem generally, algorithmic design techniques uncover nonintuitive, high-performance layouts that traditional methods cannot produce. Algorithmic design approaches have shown significant success in optimizing microwave devices [2], [3], [4] and

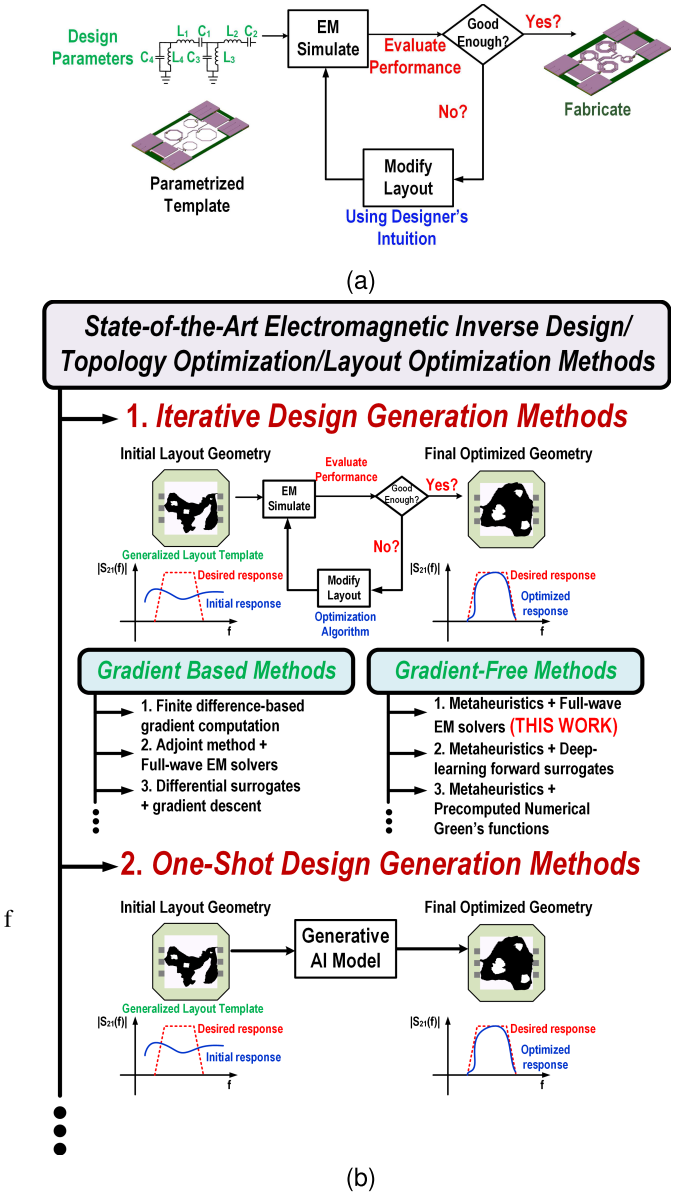

Fig. 1. (a) Traditional passive network design procedure. (b) State-of-the-art algorithmic and inverse design methodologies of passive networks.

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photonic devices [5] over the past three decades. More recently, they have gained traction in RF applications, including on-PCB RF filters [6] and multiport on-chip passive networks [7]. However, prior efforts have been limited to single-layer structures, failing to leverage the multiple metal and via layers available in standard IC fabrication, thus missing opportunities for improved performance and reduced area. This work, an extension of [1], addresses that gap by demonstrating an on-chip multilayer pixelated passive design.

While most recent efforts have focused on accelerating convergence either through improved computational techniques [8], [9], [10] or machine learning (ML) assistance [7], [11], little attention has been given to exploring other potential applications of algorithmic design. This work also explores new use cases of algorithmic design, including design diversification for intellectual property (IP) protection and shrinking layouts.

Section II outlines the challenges associated with multilayered algorithmic design, while Section III summarizes the optimization algorithms used in this work. Section IV presents a case study of a multilayer algorithmically designed passive network: wideband mm-wave power combiners with built-in impedance transformation. Section V demonstrates the design diversification capabilities of algorithmic design using measured examples of bandpass filters (BPFs). Section VI concludes the article.

II. Algorithmic Design of Multilayer Passives

The generalized layout templates used in algorithmic design techniques [Fig. 1(b)] can take several forms. For example, the design region may allow unrestricted structural flexibility, enabling arbitrary distributions of topological features such as islands and holes with varying shapes and sizes. These approaches often use gradient-based optimization to evolve continuously varying parameters, such as material properties (e.g., conductivity and dielectric constant), through methods like density-based topology optimization [3] or higher-dimensional level-set techniques that implicitly shift device boundaries [12]. Efficient gradient computation typically relies on adjoint sensitivity analysis, which requires access to the internal system matrices of EM solvers, which are not generally available to the users in standard electronic design automation (EDA) tools used for chip design. Moreover, despite offering maximum structural freedom, these methods often converge to solutions that violate foundry design rule checks (DRCs), making them unsuitable for fabrication. This issue becomes even more severe in multilayer designs, where vias are subject to strict dimensional constraints and must be placed only where metals exist directly above and below.

A more practical alternative is to use pixelated layout templates, where metal/dielectric layers are discretized into grids of pixel windows [2], [4], [6], [7], [8]. These layouts can be implicitly represented using binary matrices, with design variables taking binary values to indicate materials such as metal (1) or dielectric (0) at each location in the device volume. This discretization simplifies DRC compliance and enables the use of gradient-free optimization algorithms,

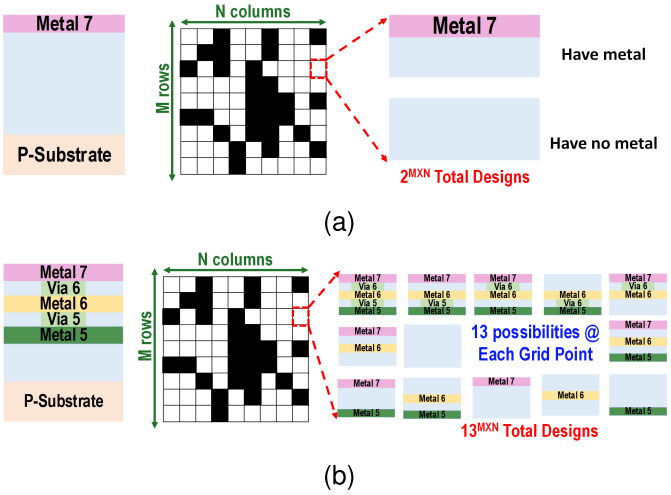

Fig. 2. Design space for pixelated passive networks. (a) Single-layer passives. (b) Multilayered passives with three metal + two via layers.

which do not require access to the internals of EM solvers. Therefore, pixel-based methods are easier to implement while still offering a significantly larger design space and greater generality than traditional passive structures.

All prior pixelated algorithmic design efforts have been limited to single-layer structures and have not explored the use of multiple metal and via layers available in IC technologies. Extending algorithmic design techniques to multilayer layouts presents additional challenges due to the curse of dimensionality: the design space expands exponentially, and EM simulation times increase significantly because of the larger number of unknowns in the solver's system matrix.

A. Expansion of Design Space

For a single-layer pixelated layout with M rows and N columns, the design space has size $2^{M\times N}$ [Fig. 2(a)], as each pixel can represent either metal or dielectric. In contrast, using three metal and two via layers expands the design space to $13^{M\times N}$, since there are 13 distinct valid configurations in which the three metal and two via layers can be filled at any given location [Fig. 2(b)]. This exponential growth in design space is both advantageous and challenging. On the one hand, multiple layers enable a broader design space that can yield significantly higher-performing layouts compared to single-layer structures. On the other hand, the size of the space reduces the likelihood of converging to a good solution due to the increased number of suboptimal local optima. To balance these competing considerations, a configuration with the top three metals and two via layers was found to offer the best tradeoff between convergence time and solution quality.

B. Increased EM Simulation Times

The solution time for any EM solver typically grows with the number of unknowns in the solution volume. For instance, the computation time for N unknowns in a classical finite element method (FEM) simulator scales as $\mathcal{O}(N^2)$ [13], while that of a classical method of moments (MoM) simulator scales as $\mathcal{O}(N^3)$ [14]. Therefore, increasing the number of metal

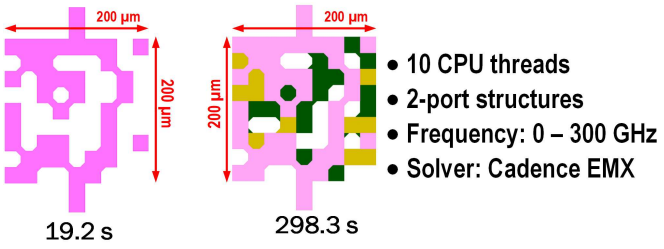

Fig. 3. EM simulation times of single-layer and multilayered layouts.

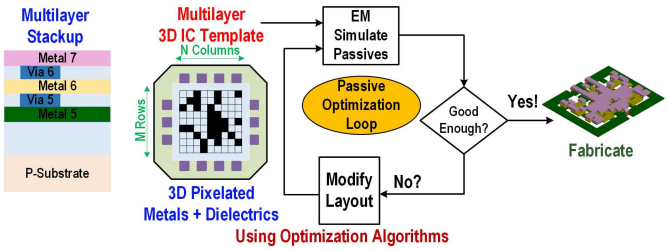

Fig. 4. Proposed algorithmic design of on-chip multilayered pixelated passives.

layers raises EM simulation times, thereby lengthening each optimization iteration. For example, in the layouts shown in Fig. 3, the multilayered case takes 10–20 times longer to simulate than its single-layer counterpart, despite occupying the same chip area.

This combination of increased EM simulation time and exponentially larger design spaces makes it infeasible to generate training datasets for ML-based surrogates [7], [11] and significantly lengthens the overall algorithmic design cycle. To address this, this work proposes optimization loops operating on 3-D pixelated layout templates using explicit EM simulators, combined with carefully selected optimization algorithms (Fig. 4), to achieve acceptable convergence times despite the use of full-wave solvers in the loop.

III. Optimization of 3-D Pixelated Passives

Gradient-free metaheuristic optimization algorithms [15], which naturally handle binary optimization variables, are used in this work. These algorithms rely on randomness to explore the solution space as a more efficient alternative to brute-force search. The discrete 0–1 nature of pixelated templates renders the optimization problem NP-hard, meaning no known algorithm, besides brute-force search, can guarantee a globally optimal solution [16]. It has also been shown that, averaged over all possible algorithms, no class of combinatorial optimization problems is intrinsically harder than others [17]. Furthermore, the no free lunch (NFL) theorems [18] state that if an algorithm A outperforms algorithm B on a problem x, there must exist another problem y where B outperforms A.

These factors, combined with the computational demands of multilayered algorithmic design, make it infeasible to perform extensive comparisons across algorithms to identify an optimal one for a given objective function. It is also infeasible to run any single algorithm enough times to establish statistically meaningful success rates. Addressing these challenges would require significant advances in EM simulation techniques or computational hardware, which are beyond the scope of this work. As with any nonconvex optimization problem, the quality of the solution depends on the appropriate combination of optimization algorithm, hyperparameters, and initial conditions, which are typically determined through ad hoc, problem-specific, on-the-fly adjustments.

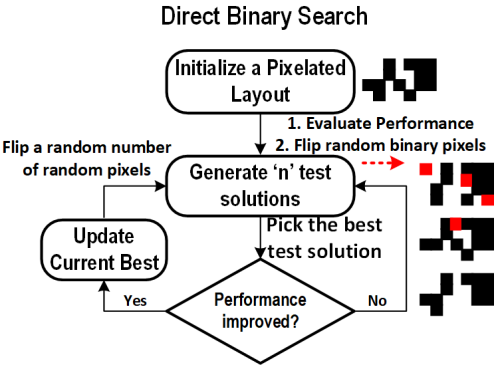

Fig. 5. DBS.

Of the many metaheuristic algorithms available in the literature [15], this work uses two: binary particle swarm optimization (BPSO) and direct binary search (DBS). Due to limitations on available CPU threads (<100), the swarm sizes in BPSO were restricted to fewer than 15 particles. Although DBS and BPSO performed well for the problems addressed in this work, the NFL theorems do not guarantee that they are the most suitable algorithms for these problems, nor do they guarantee effectiveness for the algorithmic design of all possible microwave structures with objective functions different from those used in this work.

BPSO and DBS offer complementary strengths due to their algorithmic distinctions. BPSO is exploratory, capable of efficiently searching a broad region of the solution space, though often with limited resolution. In contrast, DBS is exploitative, well-suited for refining existing solutions through incremental changes, but less effective at exploring globally. To balance these tradeoffs, BPSO may first be used to generate high-quality initial solutions, which can then be fine-tuned using DBS to maximize performance through local exploitation.

A. Direct Binary Search

In its basic form, DBS involves initializing the pixelated grid with the initial seed. In each iteration, a random pixel is flipped, and the change is retained if performance improves; otherwise, the flip is reverted, and an alternative pixel is considered. This process continues until either the allotted time expires or the target specification is achieved. In the context of EM problems, a single flip may not induce a substantial change to evaluate performance improvements in each iteration. Additionally, the speed of EM simulations increases sublinearly with the number of CPU cores. Therefore, a slightly modified DBS version is utilized (Fig. 5), testing multiple (4–12) mutations of the current-best solution simultaneously in every iteration and picking the best out of them. Each test solution is generated by randomly flipping

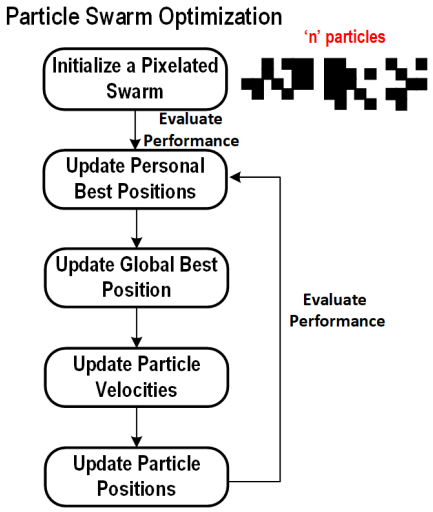

Fig. 6. Typical particle swarm optimization flow.

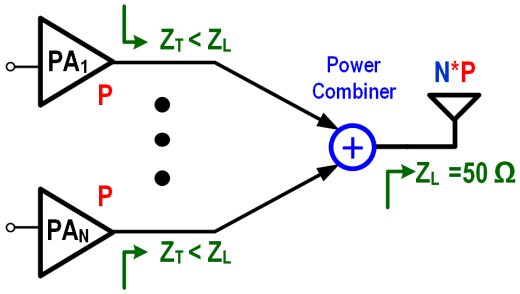

Fig. 7. Power combining in RF PAs.

up to ten pixels in the current-best solution, enhancing search throughput and exploration capability without compromising exploitation.

B. Binary Particle Swarm Optimization

Particle swarm optimization (Fig. 6) treats each test solution as a particle navigating the solution space with varying velocities. In the binary variant of PSO, each test solution (particle) is characterized by a 3-D binary array (the position array) representing pixels in the EM structure, and a corresponding 3-D real-valued array (the velocity array) denoting the probabilities of flipping the pixels in the next iteration. The particles' positions and velocities are updated in each iteration based on the individual and the global best-known positions. Optimization concludes when all particles converge to the same position. At this point, BPSO reduces to inefficient exploitation, making the transition to DBS meaningful. Among various BPSO variants available in the literature (see [19], [20], [21], [22], etc.), this work adopts the approach in [19] to generate high-quality initial seeds for subsequent optimization using DBS.

IV. Impedance-Transforming Wideband Multilayered mm-Wave Power Combiners

Power combining (Fig. 7) is widely used in power amplifiers (PAs) to increase total transmitted RF power by summing the outputs of individual PA cells. To maintain high PA efficiency, power combiners must exhibit low insertion loss (IL). Additionally, to extract maximum power from each PA cell without exceeding transistor breakdown limits, the combiner must transform the 50 Ω antenna impedance to a lower value.

Wideband PAs have gained significant interest, with both algorithmic design approaches [23] and traditional methods [24] used to achieve broad bandwidths. However, existing wideband solutions typically occupy large chip areas and exhibit insertion losses exceeding 1 dB. These factors motivate the exploration of multilayered algorithmic design techniques to realize compact, wideband power combiners with built-in impedance transformation and low loss.

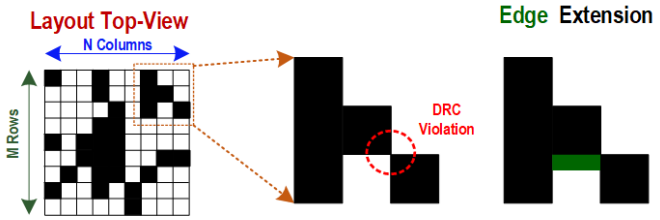

Fig. 8. Dealing with single-point connections in on-chip pixelated layouts.

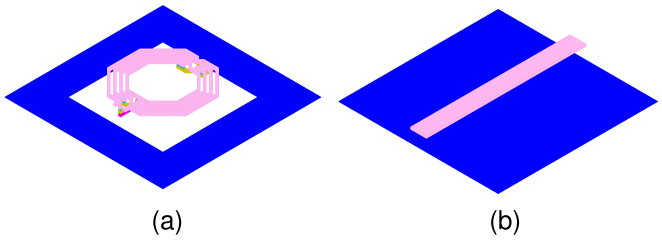

Fig. 9. Ground shielding in traditional on-chip passives. (a) Spirals. (b) Transmission lines.

A. On-Chip Algorithmic Design Considerations

Several factors, such as DRC compliance and ground plane formation, must be addressed to make on-chip pixelated passive design feasible.

1) Single-Point Connection DRC Violations: Single-point connections (Fig. 8) commonly occur in pixelated layouts when two neighboring pixels touch only at a single corner. These connections are undesirable, as they violate foundry DRC rules and thus prevent fabrication. Moreover, they introduce singularities in EM simulations, often leading to nonconvergent solver behavior.

A simple solution is to extend one of the pixel edges at the corner to create a slight overlap. In this work, the overlap amount is set to the minimum allowed by the DRC, which is smaller than the typical pixel dimensions used. These edge extensions are included in the EM simulations of the layouts corresponding to each binary pattern, ensuring accuracy during every optimization iteration.

2) Ground Shield: In certain traditional on-chip passive structures, such as spiral inductors, baluns, and transformers [Fig. 9(a)], a solid ground shield is typically avoided beneath the spiral patterns, as it induces eddy currents that degrade

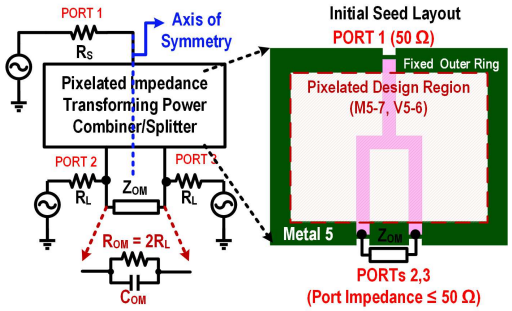

Fig. 10. Multilayered pixelated power combiner design optimization template.

the quality factor due to increased loss. In contrast, for other passive components like microstrip transmission lines [Fig. 9(b)], the return path is deliberately designed as a solid, low-impedance ground plane to minimize loss per unit length.

These examples illustrate that traditional design practices offer no consistent guidelines regarding the necessity of ground shielding. Therefore, to maintain generality in the design process, it is essential to formulate the algorithmic design problem such that ground shields, if beneficial, are automatically synthesized by the optimization algorithm.

B. Power Combiner Design Problem Setup

The optimization template for the 2-to-1 power combiner design is shown in Fig. 10. The design utilizes the top three aluminum metal layers and the two corresponding tungsten via layers available in Tower Semiconductor's SBC18 180-nm SiGe BiCMOS technology.

1) Optimization Layout Template: The template features a multilayer pixelated design region at the center, surrounded by a fixed 10-μm-wide metal five outer ring, relative to which the three EM ports are referenced. While using EM ports referenced to global grounded planes remains the predominant paradigm in RFIC design, this convention is primarily driven by convenience rather than fundamental necessity. As demonstrated in [25], transistor cells can be laid out to interface with EM structures that use locally referenced ports. By fixing the outer metal five-ring and pixelating only the inner region, the algorithm is implicitly given the freedom to construct its own ground planes, preserving generality in the optimization problem. Port 1 is always assumed to be driven with a 50-Ω source impedance, while ports 2 and 3 may present lower impedances depending on the desired impedance transformation ratio. The initial seed, shown in Fig. 10, is a simple dc short implemented in metal 7, which initially connects all ports. A vertical axis of symmetry is used to ensure a truly symmetric structure, eliminating any systemically introduced amplitude and phase imbalance at ports 2 and 3.

2) Optimization Objective Function: The goal of the optimization problem is to find the optimal 3-D binary matrix $\mathbf{B}$ that maximizes the $|S_{21}|$ over the 20–120-GHz range. One possible objective is the maximin function, defined in (1), which seeks to maximize the minimum value of $|S_{21}|$ across the band. EM simulations are carried out over this range using an adaptive sweep, ultimately producing S-parameters with a 100-MHz frequency step

$$\mathbf{B}^* = \arg \max_{\mathbf{B}\in\{0,1\}^{n_x\times n_y\times n_z}} \left(\min_{f\in[20,\,120]\,\mathrm{GHz}} |S_{21}(f;\mathbf{B})| \right). \quad (1)$$

An alternative is to maximize the harmonic mean of $|S_{21}|$ across all frequency points, as shown in the following equation:

$$\mathbf{B}^* = \arg \max_{\mathbf{B}\in\{0,1\}^{n_x\times n_y\times n_z}} \left(\frac{1}{N} \sum_{\substack{i=1,\ldots,N \\ f_i\in[20,\,120]\,\mathrm{GHz}}} \frac{1}{|S_{21}(f_i;\mathbf{B})|} \right)^{-1}. \quad (2)$$

A common feature of both objective functions is their emphasis on worst case performance. By prioritizing low values of $|S_{21}|$, these formulations ensure performance is optimized uniformly across the entire frequency band. In the context of the power combiner problem, both approaches were found to yield solutions of comparable quality; however, the maximin formulation was ultimately adopted for the synthesized devices. Both objective functions also implicitly minimize $|S_{11}|$ within the desired frequency range, since maximizing transmission from port 1 to ports 2 and 3 inherently minimizes the power reflected back from port 1.

3) Optimizing $|S_{22}|$, $|S_{33}|$, and $|S_{23}|$: Three-port passive networks cannot be lossless, reciprocal, and matched simultaneously [26]. Therefore, loss is intentionally introduced via an impedance Z_{OM} (Fig. 10) across ports 2 and 3, to achieve matching. While traditional power combiners such as Wilkinson combiners use a purely resistive Z_{OM}, simulations revealed that incorporating a capacitive component improves matching bandwidth in these nonintuitive structures.

Since Z_{OM} only influences the odd-mode behavior of the network, it ideally has no impact on S_{11}, S_{21}, or S_{31}, which are determined primarily by even-mode behavior. Consequently, Z_{OM} was determined postoptimization. However, adding a capacitive element to Z_{OM} does not guarantee high isolation between ports 2 and 3 seen in traditional Wilkinson combiners, potentially resulting in suboptimal $|S_{23}|$. Although $|S_{23}|$ was not considered in this work, future designs could incorporate it into the optimization loop. It is important to note that a suboptimal $|S_{23}|$ does not render the device unusable, as in many circuits, such as symmetrically power-combined PAs (see [25]), $|S_{23}|$ is irrelevant due to the circuit operating exclusively in even mode.

4) Hyperparameters and Impact on Scalability: Hyperparameters are inputs to an optimization algorithm that indirectly influence the quality of the solution and the number of iterations required to converge at the final optimized design. In an algorithmic multilayered pixelated passive design, these include the number of metal layers, pixel size, layout dimensions, and the number of rows and columns. Identifying the optimal combination of hyperparameters is nontrivial, as it would require an additional optimization loop outside the algorithmic design loop, one that explores a highly nonconvex hyperparameter space by repeatedly running the already expensive algorithmic design process. Therefore, hyperparameter tuning remains an active research area [27].

State-of-the-art methods, such as evolutionary algorithms and Bayesian optimization, often struggle with convergence when the inner loop (the algorithmic design loop) is itself computationally intensive and highly nonconvex [27].

The total design time equals the EM simulation time of a given structure multiplied by the number of iterations required. While the exact EM simulation time for any structure cannot be predicted in advance [14], it is known to scale with polynomial complexity as the layout size increases in terms of area and number of layers [13], [14]. This scaling is largely independent of pixel resolution; to first order, only the area and number of layers determine EM simulation time.

On the other hand, the NP-hard nature of these 0–1 problems, combined with exponentially large design spaces, makes it infeasible to predict the number of iterations required to converge. This uncertainty stems from the dependence on hyperparameters, which strongly influence convergence behavior, yet cannot be determined beforehand.

Consequently, it is not possible to predict either the total convergence time or how computational requirements scale with problem size and objective function. As illustrated by the examples in this work, even when design space sizes differ by hundreds of orders of magnitude, the observed convergence times increase only by a factor of 4–5. This highlights the dominant influence of hyperparameters and optimization choices. However, because the optimal combination of hyperparameters, optimization algorithm, and initial conditions cannot be known in advance, the computational cost itself cannot be predicted a priori.

This work adopts a strategy of minimizing layout area and pixel count to accelerate convergence. The area or pixel count is increased only if the initial configuration fails to yield satisfactory results within a reasonable time. Using this approach, a pixelated grid with 11 rows and 15 columns was found to be effective. Owing to the enforced symmetry axis, the effective number of columns is further reduced to 8.

5) Robustness and Tolerance to Fabrication Deviations: The robustness of the proposed pixelated passives to process variations is comparable to that of traditionally designed passives. This is because the discretized metal pixels used here have lateral dimensions on the order of several micrometers, which are much larger than typical lithographic deviations in advanced silicon technologies (tens of nanometers). As a result, any in-plane disturbances are unlikely to produce meaningful electrical perturbations. Variations in vertical dimensions, such as metal thickness or interlayer dielectric spacing, can be evaluated using conventional back-end-of-line (BEOL) process corner simulations. While these effects were not explicitly incorporated into the optimization flow of Fig. 1(b), they can, in principle, be integrated into the loop without altering the methodology.

At present, commercially available EDA tools do not expose the internal system matrices needed to carry out tolerance analysis of pixelated layouts directly. Therefore, statistical robustness studies would either require large-scale measurements of thousands of fabricated devices or custom adjoint implementations within full-wave solvers, both of which are beyond the scope of this work.

Importantly, several multilayer structures with pixel dimensions ranging from $6.5\times6.5\ \mu\text{m}^2$ to $10\times10\ \mu\text{m}^2$ are fabricated and measured in this article. The measured results closely tracked EM simulations, and the foundry raised no concerns during mask preparation and optical proximity correction (OPC). This empirical evidence underscores the manufacturability and practical robustness of the proposed methodology.

6) Optimization Algorithm and Computational Requirements: DBS was used to synthesize various power combiners starting from the initial seed shown in Fig. 10. In each iteration, DBS evaluated six test solutions (Fig. 5), generated by flipping up to nine random pixels in the current-best solution. Depending on the desired impedance transformation ratio, each design took 6–10 h to complete. With each iteration requiring ~8 min on 72 threads of an Intel[1] Xeon E5-2695 v4 CPU, the total number of EM simulations per design ranged from 250 to 500, despite operating within design spaces as large as $13^{88}\approx10^{98}$.

C. Example Algorithmically Designed Power Combiners

Fig. 11 shows the synthesized layouts of three power combiners designed for impedance transformation ratios of 50 Ω–50 Ω, 50 Ω–25 Ω, and 50 Ω–12.5 Ω. Simulated results confirm their wideband operation and low IL. All three designs are well matched at all ports. The 10-dB isolation bandwidth does not fully span the operational frequency range since $|S_{23}|$ was not explicitly optimized. Table I compares these combiners with prior state-of-the-art on-chip wideband power combiners, both traditionally designed and algorithmically designed, most of which only support 50 Ω–50 Ω transformation.

The proposed combiners demonstrate superior performance across all key metrics, including loss, bandwidth, and area, while ensuring excellent port matching and introducing no systemic amplitude or phase imbalances, owing to their truly symmetric layout. These results clearly demonstrate the superiority of the algorithmic multilayer pixelated passive design approach over both conventional and single-layer inverse design techniques.

Future efforts will focus on incorporating isolation ($|S_{23}|$) into the optimization objective, as well as developing more efficient computational techniques and optimization algorithms to achieve faster convergence.

V. Design Diversification Using Algorithmic Design Techniques

IP theft and counterfeit products are major challenges in the semiconductor industry, resulting in billions of dollars in annual losses and the elimination of thousands of jobs [30]. Moreover, unreliable counterfeit components pose serious risks to public health, safety, and national security when used in critical systems such as medical devices, power grids, communication networks, automotive safety systems, and military or aerospace applications [31]. These concerns have led both governments and industry stakeholders to pursue strategies aimed at mitigating the growing threat of counterfeits [32], [33]. Such efforts become even more crucial during

[1]Registered trademark.

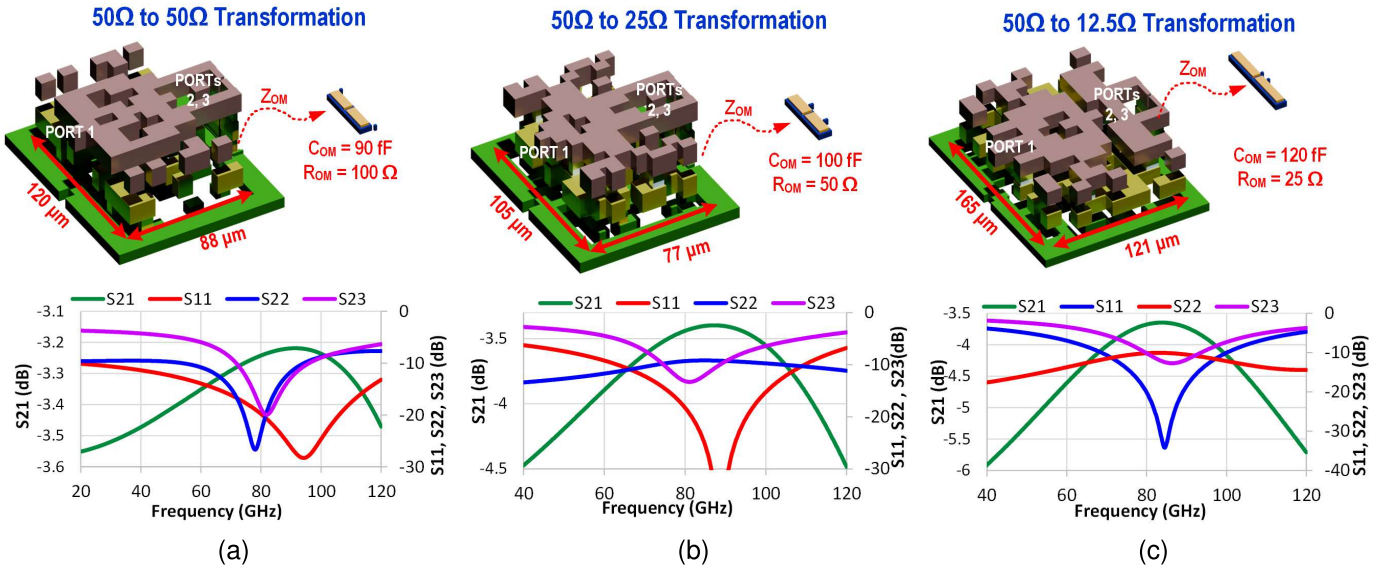

Fig. 11. Combiners with 50 Ω (port 1) to (a) 50 Ω (ports 2 and 3), (b) 25 Ω (ports 2 and 3), and (c) 12.5 Ω (ports 2 and 3) impedance transformation ratios.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART ON-CHIP WIDEBAND POWER COMBINERS

	Freq. Range (GHz)[a]	Impedance Transformation Ratio	Topology	IL (dB)	S11 (dB)	S22 (dB)	ΔAmp. (dB)	ΔPhase (°)	Area (mm²)	Normalized Size (λ^2 @ f_{center})
[28] - IMS 2024[b]	25-79	50 Ω to 50 Ω	Singlelayer Inverse Design	0.8 to 1.5	N/R	N/R	≈ 0	0.75 to 2.3	0.16	0.0064
[29] - IMS 2019[c]	15 - 55	50 Ω to 50 Ω	Folded Inductor	0.5 - 1.17	< −10	< −15	< 0.2	< 3	0.0361	0.00049
This work - Fig. 11(a)	**20 - 100**	**50 Ω to 50 Ω**	**Multilayer Algorithmic Design**	**0.2 to 0.6**	**< -10**	**< - 9.5**	**0**	**0**	**0.0106**	**0.00042**
This work - Fig. 11(b)	**60 - 110**	**50 Ω to 25 Ω**		**0.4 to 0.9**	**< -10**	**< - 9.5**	**0**	**0**	**0.0081**	**0.00065**
This work - Fig. 11(c)	**68 - 100**	**50 Ω to 12.5 Ω**		**0.66 to 1.1**	**< -10**	**< - 10**	**0**	**0**	**0.02**	**0.0015**

[a] - defined as the frequencies over which S11 < -10 dB for structures in this work, [b] - estimated from figures 3(d)-(f) of the reference, [c] - measured results

periods of supply chain shortages, which further incentivize counterfeiting activity [34].

As discussed in [34], counterfeit chips infiltrate supply chains in three primary forms: gray-market recycled chips, fraudulent clones, and overproduced or failed parts. Mitigating these threats requires chip design strategies tailored to these counterfeiting mechanisms, without compromising chip performance. Toward this end, this work leverages algorithmic design techniques as a mechanism for IP protection. The stochastic nature of metaheuristic algorithms, combined with the highly nonconvex landscape of algorithmic design problems, enables the generation of multiple device layouts with near-identical performance. RFIC vendors can exploit this property to distribute visually distinct variants of a given component to different clients (Fig. 12). This enables traceability of IP leaks and improves accountability to the law. This, in turn, serves as a deterrent to IP theft and counterfeiting. Moreover, since algorithmically designed layouts are highly nonintuitive, their operating principles cannot easily be comprehended. This adds an additional layer of protection against fraudulent cloning, as an IP thief would be unable to alter the clone's appearance in an attempt to disguise the theft.

This work proposes two mechanisms for layout diversification as follows.

1) *Stochastic Variation:* The inherent randomness of metaheuristic design is leveraged to generate multiple layouts with identical performance by running the optimization algorithm multiple times with the same objective function.
2) *Adiabatic Pixel Shrinking:* This technique modifies the layout appearance while preserving electrical performance by gradually shrinking pixels. It not only diversifies the design but also reduces the layout area, saving valuable chip real estate.

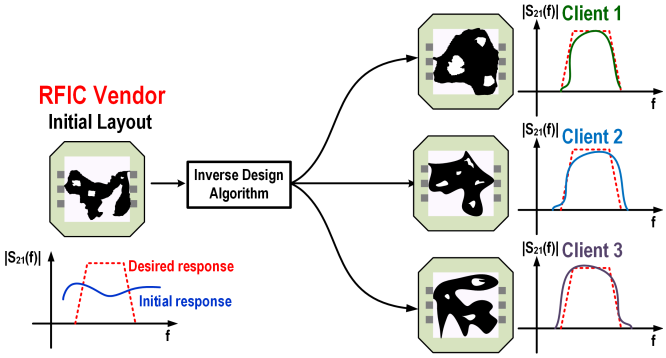

Fig. 12. Using algorithmic design for diversifying designs.

mm-Wave BPFs are synthesized to experimentally demonstrate the design diversification capabilities of algorithmic design techniques. *It is emphasized that the primary purpose of these BPFs was to validate diversification, not to achieve maximum performance. As such, the filters were not necessarily fully optimized for peak achievable performance.* The BPFs were all implemented in Tower Semiconductor's SBC18 180-

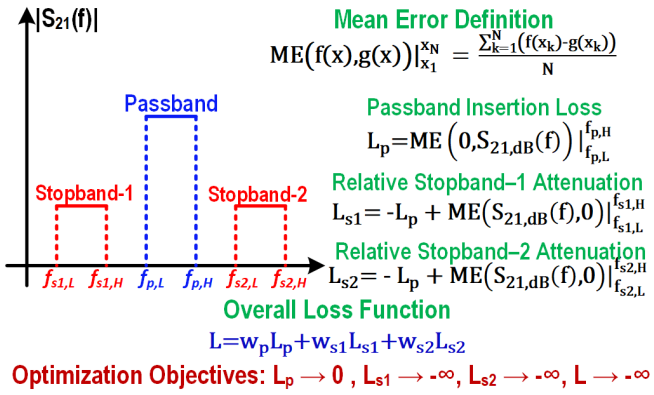

Fig. 13. Loss function definition for BPF design.

nm SiGe BiCMOS technology using the top 3 aluminum metal layers and the 2 corresponding tungsten via layers.

A. Optimization Loss Function Definition

The loss function used for BPF design, denoted as L and illustrated in Fig. 13, aims to maximize $|S_{21}(f)|$ within the passband and minimize it in the two stopbands. It consists of three terms: L_p for passband IL, and L_{s1} and L_{s2} for stopband attenuation relative to the passband. Similar to the power combiner optimization in Section IV, minimizing $|S_{11}(f)|$ in the passband is not explicitly enforced. For low-loss passive networks, energy conservation implies $|S_{21}|^2 + |S_{11}|^2 \approx 1$, making an explicit S_{11} term unnecessary. However, since some fabricated BPFs exhibited nonnegligible loss, suboptimal in-band $|S_{11}(f)|$ was observed.

Although performance maximization was not the primary goal of these BPFs, this issue can be addressed in future work by adding an explicit S_{11} term to the objective function, as demonstrated in prior work [6]. Alternatively, return loss can be incorporated nonlinearly with the S_{21} terms [35].

All terms in the loss function use $|S_{21}|$ in the dB scale. The weights w_p, w_{s1}, and w_{s2} influence the optimization outcome: higher w_p reduces IL but degrades selectivity, while lower w_p improves selectivity at the cost of higher IL. Initial values are set to $w_p = 2$ and $w_{s1,2} = 1$, and manually adjusted during optimization to balance the terms and avoid undesirable filter shapes. The passband is defined by frequencies $f_{p,L}$ and $f_{p,H}$, while $f_{si,L}$ and $f_{si,H}$ define the stopbands, automatically determining the transition bandwidth. The optimization seeks to drive L toward $-\infty$ for best performance.

B. Approach 1: Stochastic Variation

The vast design space available for multilayered passives (Section II), combined with the highly nonconvex optimization landscape, enables the generation of multiple layouts with near-identical functionality. The stochastic nature of meta-heuristic optimization algorithms (Section III) facilitates the discovery of such diverse solutions.

To demonstrate this capability, two nonintuitive initial designs were first generated from 14 standard first-order LC filters using 250 iterations of BPSO followed by approximately

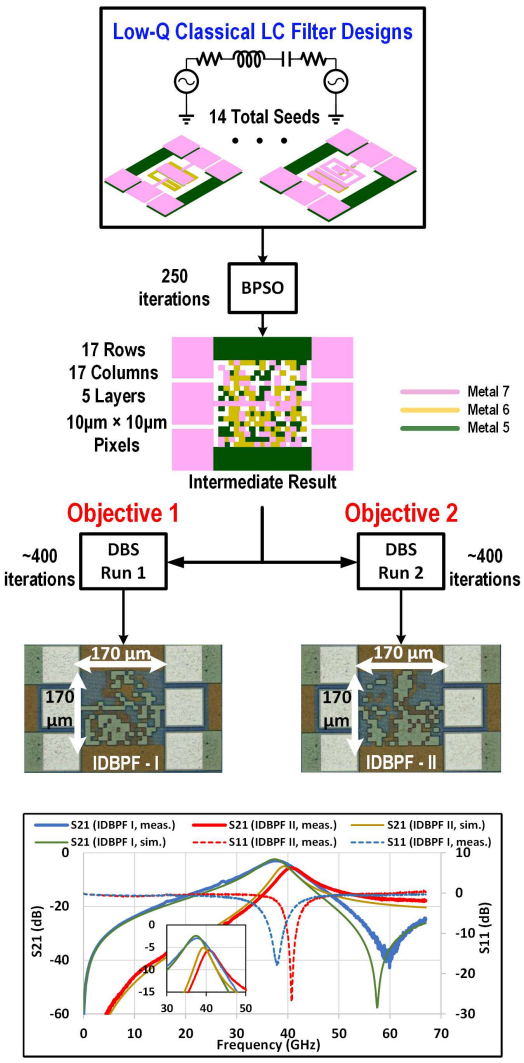

Fig. 14. Generation of initial pixelated designs by obfuscating classical LC filters.

400 iterations of DBS (14 test solutions in each iteration), and a distinct objective function (Fig. 14). Each iteration took about 4 min using 72 threads on an Intel[1] Xeon E5-2695 v4 CPU, resulting in a total design time of approximately 43 h per filter. These designs served as initial seeds for subsequent optimization and diversification.

All the designs occupied 170 × 170 μm (excluding pads). A pixel size of 10 × 10 μm (17 rows, 17 columns) was selected. The two initially algorithmically designed BPFs (IDBPFs I and II) were intentionally designed to have different center frequencies. The layout area and grid resolution were chosen to be the minimum required to accommodate the initial seeds within the 30–40-GHz frequency range. Since these filters were intended to be starting points for further design exploration and diversification, maximizing performance was not the primary objective.

The pixelated patterns of IDBPFs I and II were cascaded to form a seed for designing higher-order filters (Fig. 15). The underlying intuition is that cascading two frequency-shifted lower-order filters can result in a higher-order filter with a broader bandwidth. DBS was then run twice using the same

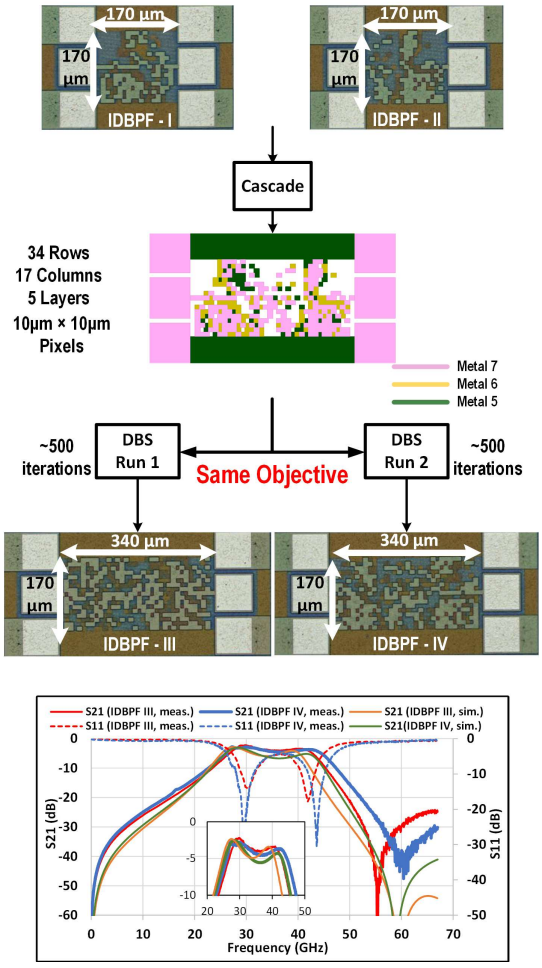

Fig. 15. Design diversification using stochastic variation.

objective function, producing two designs—IDBPF-III and IDBPF-IV.

Starting from the intermediate cascaded layout, each design was optimized using approximately 500 iterations of DBS with eight test solutions per iteration. Using 96 threads on an Intel Xeon Gold 5118 CPU, each iteration took about 3 min, allowing the complete designs to be generated within a day. Both filters exhibit nearly identical measured IL, bandwidth, and transition band characteristics (Fig. 15).

This example demonstrates the ability of algorithmic design techniques to generate multiple, functionally equivalent layouts through stochastic variation, highlighting its potential for design diversification.

C. Approach 2: Adiabatic Pixel Shrinking

Passives occupy the largest area in RFICs, making it desirable to explore algorithmic design techniques not only for performance-preserving visual diversification but also for reducing layout area without compromising performance. To this end, a pixel shrinking algorithm [Fig. 16(a)] was developed. The approach begins with a high-performance initial seed and gradually reduces the pixel size. Each reduction causes a slight performance drop, which is then recovered by running DBS for a sufficient number of iterations. Once performance is restored, the pixel size is further reduced,

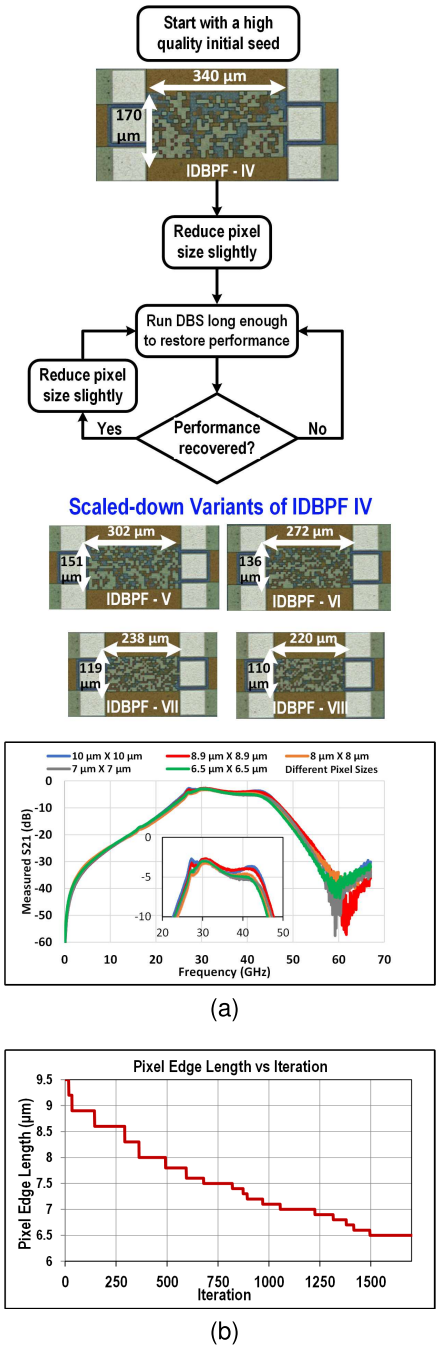

Fig. 16. Adiabatic pixel shrinking using algorithmic design techniques. (a) Pixel shrinking algorithm. (b) Pixel size versus iteration.

and the process repeats. Using this method, multiple layouts with virtually identical measured performance but significantly different sizes were generated.

Fig. 16(b) shows the progression of the algorithm over time. At any given pixel size, once the performance is recovered, the pixel edge length is reduced in steps of 0.1 μm until a predefined error threshold is reached, which then defines the next pixel size. Starting from an initial size of 10 $\times$ 10 μm, IDBPF-IV was successfully shrunk to 6.5 $\times$ 6.5 μm over 1700 iterations (approximately three days), without degrading performance. As shown in Fig. 16, this process not only reduces area but also results in a visually different layout.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	Center Freq. (GHz)	BW-3dB (GHz)	IL @ Peak (dB)	Area (mm^2)
IDBPF I	**37.7**	**8**	**3**	**0.029**
[36]	33	11.9	2.6	0.038
[37]	31	14	2.4	0.024
[38]	35	15.3	1.7	0.039
[39]	30	14	1.66	0.009
IDBPF III	**35**	**17**	**2.1**	**0.058**
IDBPF IV	**36**	**19.5**	**2.7**	**0.058**
IDBPF VIII	**34.5**	**17.3**	**2.9**	**0.024**
[40]	35	26	5	0.124
[41]	33	22	1.5	0.07
[42]	34.5	42	1.6	0.033

Thus, pixel shrinking adds another dimension to the design diversification capability of algorithmic design techniques by introducing variation in both appearance and physical footprint.

D. Performance Summary

The performance summary of IDBPFs I, III, IV, and VIII (the worst case among the scaled-down filters) is provided in Table II. While these IDBPFs were not optimized for peak performance, they still demonstrate performance comparable to or better than many of the state-of-the-art BPFs. For example, IDBPF-I shows comparable IL and bandwidth to filters with similar center frequencies. Similarly, IDBPFs III, IV, and VIII achieve performance on par with several state-of-the-art designs, despite occupying smaller or similar areas.

The inability of the fabricated IDBPFs to outperform some of the best traditionally designed filters is not a limitation of the algorithmic design methodologies themselves. Performance can be further improved through better optimization strategies. For instance, enhancements in the loss function, such as incorporating terms to promote transmission zeros, could improve selectivity without increasing IL. Likewise, using better initial seeds can lead to improved outcomes. Future research could explore seeding design algorithms with the best-known high-performance traditional filter layouts to push performance further.

Moreover, the successful experimental validation of adiabatic layout scaling suggests the presence of untapped design space for realizing compact, high-performance filters. These observations reinforce the highly nonconvex nature of the multilayered algorithmic design landscape and highlight opportunities for further exploration using refined strategies.

VI. CONCLUSION AND FUTURE WORK

This work has addressed the key challenges associated with the algorithmic design of multilayered pixelated passives and presented several optimization strategies to overcome them. The advantages of multilayered algorithmic design techniques over both single-layer and traditional approaches were demonstrated through the example of wideband impedance-transforming power combiners.

Additionally, a novel application of algorithmic design techniques for layout diversification, aimed at IP protection and counterfeit prevention, was proposed and validated using BPF examples. The pixel shrinking algorithm further illustrated that layouts can retain performance even as their area is reduced, an outcome not achievable through traditional design methods.

Future work will explore algorithmic design techniques for other passive network topologies and develop computational techniques to significantly accelerate the optimization process.

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