SHORT-PAPER

Hardware Implementation of an Underwater Acoustic Massive MIMO Transmitter

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Abstract

This paper presents the hardware implementation of a massive Multiple-Input Multiple-Output (MIMO) transmitter for underwater acoustic (UWA) communication capable of incorporating precoding or beamforming. The transmitter consists of baseband and passband processing modules implemented on an AMD-Xilinx All Programmable System-on-Chip (AP-SoC) architecture, front-end power amplifiers, and high-frequency transducers. While the number of channels can be easily scaled, the current hardware demonstrates a 16-channel transmitter at a carrier frequency of 115 kHz. Experiments in the lab and field show that passband beamforming and precoding are successfully transmitted through the 16 transducers. The receiver signal strengths, however, deviate largely from the free-space simulation of the beam patterns due to rich multipath reflections and imperfection in element spacing and omni-directionality of the transducers.

Keywords

Underwater acoustic communication, Massive MIMO, Beamforming, Precoding

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1 Introduction

In recent years, Multiple-Input Multiple-Output (MIMO) and massive MIMO technologies have attracted strong interest in underwater acoustic (UWA) communication and networking thanks to their potential to address the need for high data-rate multi-user underwater wireless networking [2, 3, 10]. Underwater acoustic channels are limited to frequency bands between 2 kHz and 200 kHz for medium and short distances. This bandwidth constraint along with the channel impairments, such as strong signal attenuation, Doppler spread, and multipath fading, makes managing spectrum and energy resources extremely challenging, especially for underwater Internet of Things (IoT) networks. Massive MIMO technology, combined with advanced precoding techniques, provides a promising solution by optimizing both spatial diversity and spectrum efficiency, thereby enhancing overall communication network performance [8].

However, the current state of the art in massive MIMO acoustic communication systems often rely on theoretical analysis and simulations [3, 10], primarily focusing on receiver beamforming rather than transmitter beamforming [12]. This highlights a significant gap in the practical application of massive MIMO technologies for underwater acoustics. In a recent work, a hardware implementation of massive MIMO is presented in [7], where baseband digital precoder and passband analog precoder have been implemented successfully on a Field Programmable Gate Array (FPGA). Other FPGA-based modems have been described in [4, 5]with limited details on the specific implementation and how they can be expanded to massive MIMO. In addition, no complete massive MIMO system has been demonstrated so far, especially massive MIMO transmitter, due to high cost and large sizes of wide-band transducers and large power consumption of power amplifiers.

This paper demonstrates a complete massive MIMO transmitter system and the lab and field experimental test results. The massive MIMO transmitter is implemented on the AMD-Xilinx Zybo Z7-20 development board for its baseband and passband modules, which leverages the ARM-based processing system (PS) and programmable logic (PL) on a single chip of Zynq XC7Z020-1CLG400C AP-SoC [11]. The output Pulse Width Modulation (PWM) with switching rate of 920 kHz are sent to transmitter power amplifiers, which are custom designed class-D amplifier board for 115 kHz. The transducers are BTech BT-120 with a transmit frequency band of 15 kHz centered around 115 kHz.

Lab and field experiments are performed to evaluate the massive MIMO beamformer performance, power efficiency, and flexibility of the proposed 16-channel UWA transmitter with different beam steering. Our results demonstrate that multipath propagation and variation of the underwater environment significantly impact signal strengths, often rendering the directional gain of beamforming ineffective, especially in the far field of the transmitter array.

2 Hardware Implementation

2.1 AP-SoC Implementation

The structure of the proposed massive MIMO implementation is shown in Fig. 1. The implementation employs Xilinx Low-Density Parity-Check (LDPC) encoder Intellectual Property (IP) as the Forward Error Correction (FEC) encoder. LDPC encoding, PWM generation and passband precoder are carried out on the PL. The remaining processing tasks—such as the block interleaver, bit-to-symbol mapper, pulse shaping filter, and carrier modulation—are carried

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out on the PS. The high-performance Advanced eXtensible Interface (AXI) port provides high-throughput data transfer between the PL and the PS. This configuration leverages the PL's parallel processing capabilities to efficiently handle the LDPC encoding, which enhances error correction and improves overall transmission reliability. By strategically distributing the processing workload, the design achieves a balance between computational efficiency and flexibility, facilitating effective multi-channel underwater acoustic communication.

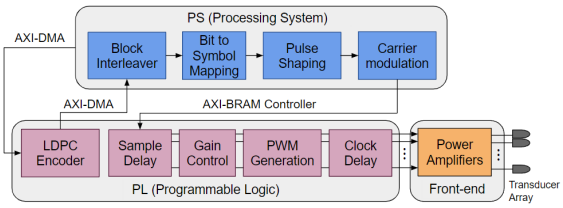


Figure 1: Implementation of multi-channel transmitter

In the implementation, the raw information bits initially stored in Double Data Rate (DDR) memory at the start of the program are passed to the Xilinx LDPC IP on PL through AXI Direct Memory Access (DMA). The LDPC IP implement the forward error FEC encoding, with the configuration of a LDPC code rate $\frac{1}{2}$ and a codeword length of 648, following the IEEE 802.11ac WiFi standard [6] to fit the common use case. The LDPC encoder processes 12 codewords per transmission packet. This approach enhances error correction and ensures reliable transmission.

After LDPC encoding, the encoded data then passes through the block interleaver, which reorganizes the encoded data by reading it column-wise and outputting it row-wise. In the implemented transmitter design, a block interleaver with 72 rows and 108 columns is utilized. The block interleaver helps mitigate burst errors, enhancing the robustness of the transmitted signal.

After interleaver, data is sent to the bit-to-symbol mapping module, where bits are grouped into complex symbols for M-ary gray-coded PSK. For the implemented design, the transmission packet consist of a pilot block and payload blocks, separated from each other by a guard interval, as shown in Fig. 2. PSK order of $M = 4$ is applied for mapping the interleaved bits into $N_{payload} = 3888$ payload symbols, while $M = 2$ is used for the 255-bit PN sequence serving as $N_{pilot} = 255$ pilots symbols. A symbol duration of $N_{gap} = 50$ gap interval is inserted between the pilots and payload, resulting symbol vector fed to next processing block.

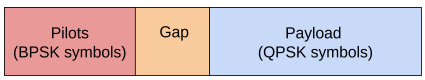


Figure 2: Structure of a typical transmission packet

Next, the pulse shaping module upsamples the signal and applies a square-root-raised-cosine (SRRC) filter to the symbol stream $s[l]$ to limit bandwidth and reduce inter-symbol interference (ISI). This module upsamples the signal by R_{sym}, which is calculated as:

$$R_{\text{sym}} = (\frac{f_c}{f_b}) \times N_{spc} \tag{1}$$

where f_c is the carrier frequency, f_b is the signal bandwidth, and N_{spc} is the number of PWM cycles per carrier period. In this implementation, the carrier frequency $f_c = 115kHz$ is used, while the bandwidth is set to $f_b = 14.375$kHz and $N_{spc} = 8$. The filter coefficients are loaded from a binary file into the PS memory and scaled to 8-bits to avoid floating-point operations, converting them to fixed-point for all subsequent data processing steps. The convolution of the baseband signal with filter coefficients is performed. The selected SRRC filter is designed with a roll-off factor of 0.35 and the symbol span is limited to $-3T_s$ to $3T_s$, where T_s is the symbol period. After pulse-shaping, the resulting signal $x_p[t]$ is carrier modulated to generate the signal $x_c[t]$.

Finally, the passband signal $x_c[t]$ is scaled to 8 bits and stored in block random access memory (BRAM) in the PL through the AXI BRAM controller. In contrast to the design in [7], which implemented the phase control by delaying the signal after PWM, our approach introduces an initial sample delay. This ensures convenience in buffering each sample is 8 bits width, whereas delaying after PWM would require buffering 128 bits for each sample, consuming significantly more resources.

After the sample delay, the signal passes through a gain control module to adjust the signal gain as needed, with amplitude gain control operating having an 8-bit resolution. The PWM generation principle uses a comparator with a resolution of 128 steps to generate the PWM signal and corresponding transmission enable signals. Following this, the generated PWM signal is delayed again at the PWM clock level to achieve high-precision phase control before being directed to 16 GPIO pins.

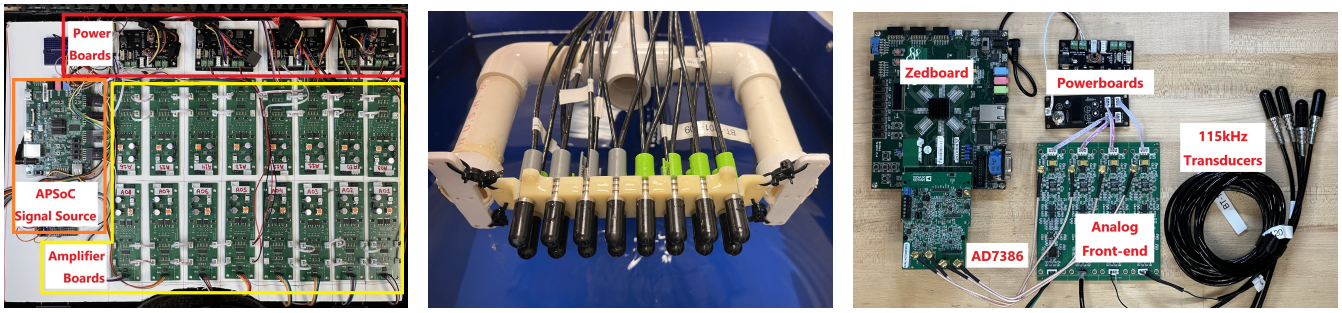
2.2 Front-end Hardware

Expanding upon this signal generation process, a complete prototype of massive mimo system is designed, utilizing a 2×8 115kHz transducer uniform rectangular array with approximately 19.8mm spacing, which is is shown in Fig. 3, the APSoC platform serving as the signal source, sixteen Class-D amplifier boards [9], and the corresponding power supply boards.

The receiver side data acquisition system, as shown in Fig. 3(c), includes a multi-channel external ADC, the EVAL-AD7386FMCZ, and a Xilinx Zedboard platform. The ADC features a 16-bit successive approximation register (SAR) ADC with four channels and supports a maximum sampling rate of 2 Msps [13]. In this design, a sampling rate of 800 ksps is chosen to capture the 115 kHz signal. The Xilinx Zedboard uses the SPI protocol implemented on the PL and the ethernet protocol on the PS. The multi-channel passband signals are amplified and filtered by the analog front-end board before being captured by the external ADC. The sampled data is transferred from the PL to the PS via the AXI-DMA bus, where it is buffered in DDR memory. The buffered samples are then sent to a laptop using the Ethernet protocol for post-processing. With the LwIP protocol supporting up to 340 Mbps, the system efficiently transfers all four-channel data without loss.

3 Performance Evaluation

This section assesses the performance of the implemented multi-channel transmitter design, addressing critical factors such as the



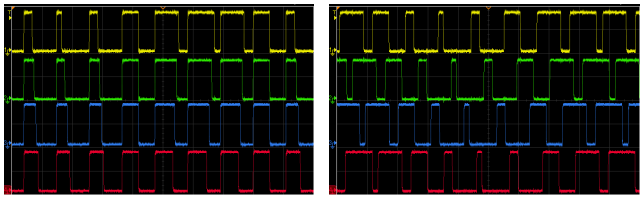
(a) Signal source and driving circuit (b) 115 kHz 2 × 8 transducer array (c) The 4-channel acoustic receiver

Figure 3: The prototyped 16-channel acoustic transmitter and receiver hardware

precision of delay and amplitude control, expandability, Error Vector Magnitude (EVM), and power consumption.

3.1 Amplitude gain and phase control

The implemented design features 8-bit amplitude gain control and 14-bit phase shift control. High order control is crucial by noticing the difficulty of practical the half-wavelength spacing in acoustic transducer arrays. An oscilloscope is used to capture four PWM outputs from the APSoC signal source to validate the functionality of the amplitude and phase control. Fig. 4(a) shows the oscilloscope capture of four output signals with no phase shift and different amplitude gains of 1, 0.75, 0.5 and 0.25, respectively. Fig. 4(b) illustrates the four channels have amplitude gain of 1, and the phases set to 0°, 9°, 18°, and 27°. The phase shifts were achieved with the precision of the PWM generation clock. While the testing setup have 8 PWM cycle representing one carrier, and the phase shift after PWM is achieved with resolution of 7 bits, the phase control achieves the precision of 0.36°.



(a) Amplitude control evaluation (b) Phase shift evaluation

Figure 4: PWM outputs of APSoC signal source

3.2 Resource utilization and expandability

For massive MIMO systems, the number of transmission elements can vary based on the specific deployment, which can be influenced by multiple factors, including the need for diversity or multiplexing gains, application-specific requirements, and environmental conditions. Some advanced systems can scale up to even larger arrays, leading to increased resource requirements. Thus, flexibility, portability, and expandability are essential considerations for hardware selection. These factors facilitate early prototyping, design iteration, and configuration adjustments.

FPGA-based transmitters offer outstanding flexibility by allowing parameterization of each functional block and utilizing a pool of generic hardware resources. This enables straightforward adjustments to various parameters, including modulation order, interleaver size and shape, guard intervals, and more. Additionally, the FPGA can accommodate as many transmit branches as its resources permit, and the number of branches can be easily adjusted to meet specific requirements.

Resource	Utilization	Available	Utilization (%)
LUT	12704	53200	23.8797
LUTRAM	191	17400	1.10
FF	9562	106400	8.99
BRAM	128	140	91.43
DSP	16	220	7.27
IO	41	125	32.8
BUFG	3	32	9.38
MMCM	1	4	25.0

Table 1: Resource Utilization Summary

The implemented FPGA-based transmitter efficiently utilizes chip resources, as illustrated in Table 1. As can be seen, this implementation of a 16-channel transmitter consumes less than 32% of the overall resources available on the utilized XC7Z020-1CLG400C SoC platform. This highlights the significant potential for future expandability to additional channels.

3.3 Error Vector Magnitude

The Error Vector Magnitude (EVM) is a figure of merit for determining the accuracy with which a transmitter produces the symbols in a constellation. To evaluate EVM, a Cypress FX2-based logic analyzer is used to records the PWM waveform from each output pin at a rate of 16 MSps. After carrier demodulation and matched filtering, this signal can be processed as data frames received via hydrophone, but with approximately no signal distortion or noise. The constellation obtained by this method is used to evaluate the

EVM of the FPGA output.
The equation used to evaluate the EVM is taken from [1] and uses the room-mean square value of the euclidean distance of the transmitted constellation points to the ideal symbols:

$$\mathrm{EVM_{dB}} = 20\log_{10}\left(\frac{\sqrt{(s_{i,k} - r_{i,k})^2}}{N_{payload}}\right) \quad (2)$$

where $r_{i,k}$ is the captured symbol corresponding to $s_{i,k}$. The designed implementation has an EVM of −33.087 dB, which denotes the outputs are close to the ideal signal. The implemented method does not negatively affect the phase and amplitude modulation of massive MIMO communication. The received constellations used to compute EVM is shown in Figure 5.

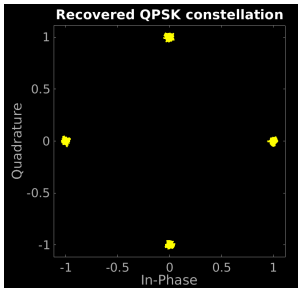
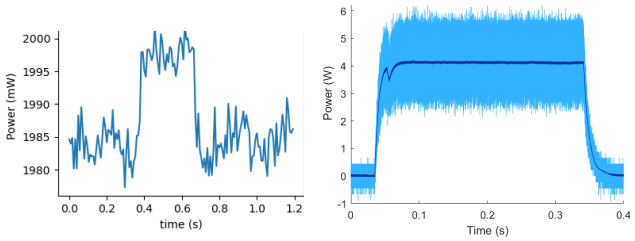


Figure 5: Recovered QPSK constellations for EVM calculation

3.4 Power Consumption

In resource-constrained underwater environments, optimizing power consumption is crucial, and power consumption should be evaluated and minimized for any underwater acoustic modem.

The power consumption for all components of transmission side is shown in Figure 6(a) The raised areas show the active transmission and other areas show the idle condition. The power consumption for the APSoC peaked at 2.0W and averaged 1.9W in the active region.



(a) APSoC (b) Power Amplifier

Figure 6: Instantaneous power consumption

The implemented transmitter outputs PWM waveform for multiple channels, which are fed to separate power amplifier responsible for driving an acoustic transducer that converts the electrical signal into acoustic signal. As shown in Figure 6(b), each amplifier device consumes 4.12W while active, and when considering the design of the system with 16 channels, the combined power consumption from the power amplifiers escalates to 65.92W, indicating that they dominate the overall power budget. The total power consumption with the FPGA solution included reaches 67.92W, of which the FPGA contributes only 2.9%. This highlights that while FPGAs are often considered to consume more power than Digital Signal Processors (DSPs) in UWA modems, the bulk of the power budget is actually consumed by the front-ends driving the acoustic transducers, underscoring the importance of efficient power management in the hardware platform used.

4 Experimental results

An experiment was conducted at the marina area of Lake Nockamixon State Park in Bucks County, southeastern Pennsylvania. The GPS-logged locations of the transmitter and receiver are illustrated in Fig. 7. Both the transmitter and receiver systems were anchored in fixed positions on a boat using a drogue anchor, maintaining a distance of up to 200 meters. The transducers were placed at a depth of approximately 0.5 meters to optimize signal transmission and reception.

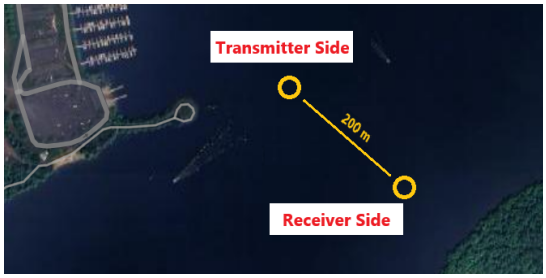


Figure 7: Experiment map

Two types of experiments were conducted: the first aimed to compare signal strength between a 1-channel and a 16-channel configuration using broadside beamforming. The second experiment examined the variation in signal strength at different steering angles.

4.1 Evaluation of signal power

The transducer array, mounted on the boat and facing towards the broadside, alternates between one-channel and 16-channel, with no gain adjustments and phase change. As shown in the result, the received signal strength from the 16-channel transmission is significantly higher than that from the single-channel transmission. The root mean square (RMS) of the 16-channel signal is approximately 7.4 times greater than the single-channel signal. This is less than the 16-fold increase, due to underwater environmental factors affecting signal propagation and limiting a linear strength increase.

Fig. 8 displays the results of 15 trials of comparing signal, each trial lasting about 2.5 seconds and including one packet of single-channel and one packet of 16-channel transmission. The variation in signal strength is more pronounced for the 16-channel transmission, as the signals from different channels lead to constructive and destructive interference at the receiver, resulting in a more dynamic communication channel.

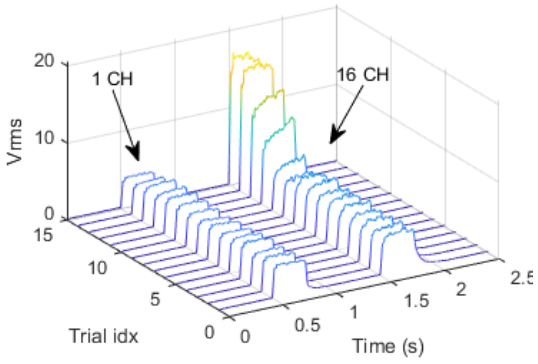


Figure 8: Signal Strength Comparison: Single-Channel vs. 16-Channel Transmission

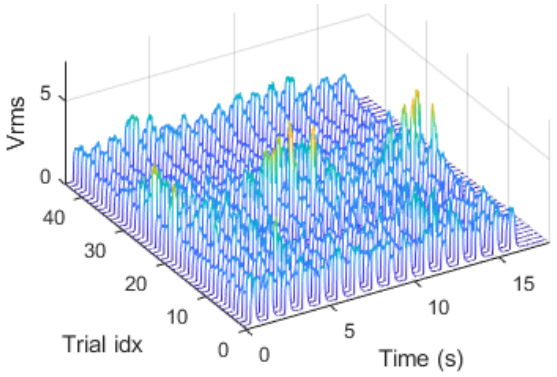


Figure 9: Effect of Beam Steering on Signal Strength

4.2 Beam steering test

Another experiment was conducted to investigate the impact of phase control on signal strength through an angular beam steering approach. In each round, the transmitter sequentially sent 16 signal packets, applying varying phase delays to the transducer array. For each transmission packet, the phase delays were incrementally adjusted in the row direction of the array, with the eight transducers applying phase delays of $0, \varphi, 2\varphi, ...7\varphi$ respectively, while the two transducers in the same column keep the same phase. This configuration facilitates constructive interference in a specific direction, which is determined by the applied phase delay φ. To achieve targeted beam steering, the phase delay φ was incrementally increased from 0, with each step corresponding to approximately 0.13 wavelength, resulting in a beam angle sweep with increments of about 5°, allowing for a comprehensive assessment of signal strength across these steering angles.

Fig 9 shows the results of 44 trials of testing, each lasting approximately 18 seconds, indicating that the signal strength changes more significantly over time than the applied phase delay. While the phase delay aims to facilitate constructive interference in specific directions, its effectiveness is limited by the dynamic nature of the underwater acoustic communication channel. This variability highlights the challenges posed by environmental factors that can disrupt coherent signal summation and affect overall communication performance.

5 Conclusion

This paper has presented the implementation of a complete massive mimo UWA system. The design effectively utilizes both the processing system (PS) and programmable logic (PL) for baseband and passband modules, optimizing performance and resource usage. Field experiments in a lake evaluated the performance of the 16-channel massive MIMO beamformer, revealing that multipath propagation and variations in the underwater environment significantly affect signal strength, often diminishing the effectiveness of directional beamforming, particularly in the far field. Despite these challenges, the reliable operation of the transmitter and its flexible hardware design, which allows for customization and future scalability, lay a strong foundation for advancements in underwater communication technologies.

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