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$PdSe_2/WSe_2$ Nanosheet-Based Heterostructures for n-Type Field-Effect Transistors with Enhanced Performance

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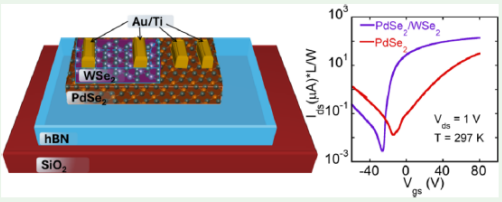
ABSTRACT: Two-dimensional (2D) semiconductors are promising candidates for next-generation flexible electronics, but their performance is often limited by low electron mobility and substantial Schottky barriers (SBs) at metal contacts. Here, we demonstrate that $PdSe_2/WSe_2$ nanosheet-based van der Waals heterostructures outperform $PdSe_2$ or WSe_2 nanosheets alone as channel materials for n-type field-effect transistors. Here, the WSe_2 nanosheet serves as a buffer layer, mitigating Fermi-level pinning and reducing SBs between Ti metal and $PdSe_2$ nanosheets. These heterostructures achieve two-terminal effective mobility exceeding 200 $cm^2\ V^{-1}\ s^{-1}$ at room temperature and nearing 680 $cm^2\ V^{-1}\ s^{-1}$ at 77 K. Additionally, the increased bandgap in thinner $PdSe_2$ nanosheets enables high on/off ratios ($\sim 10^7$) in $PdSe_2/WSe_2$. These results underscore the potential of $PdSe_2/WSe_2$ nanosheet-based heterostructures and the importance of interfacial engineering in advancing 2D electronic devices.



KEYWORDS: *$PdSe_2$, WSe_2, heterostructure, field-effect transistor, Schottky barrier, contact resistance*

1. INTRODUCTION

Atomically thin and uniform two-dimensional (2D) semiconductors, offering exceptional mechanical strength and flexibility, are promising channel materials for next-generation flexible electronics and optoelectronics, enabling performance beyond the scaling limits of Si-based metal-oxide-semiconductor field-effect transistors (MOSFETs).[1−15] Among 2D semiconductors, group 6 transition metal dichalcogenides (TMDs), such as MoS_2, $MoSe_2$, and WSe_2, have been extensively studied. While high hole mobility exceeding 1000 cm^2/V s at room temperature has been reported in WSe_2,[16] its relatively low electron mobility at room temperature restricts its potential for complementary electronic applications.[17,18] Furthermore, group 6 TMDs often form significant energy barriers with commonly used metals for electrical contacts, further hindering their performance in electronic and optoelectronic devices.[19−23]

Recently, group 10 TMDs such as $PtSe_2$ and $PdSe_2$ have emerged as high-mobility 2D electronic materials with a theoretically predicted high electron mobility exceeding 1000 $cm^2\ V^{-1}\ s^{-1}$ at room temperature,[24,25] significantly higher than those of group 6 TMDs like MoS_2 and WSe_2. Experimentally, a four-terminal field-effect mobility as high as ~700 cm^2/V s at room temperature, excluding contact resistance, has been observed in hBN-encapsulated few-layer $PdSe_2$ field-effect transistors with gated graphene contacts. This mobility increases to ~10,000 cm^2/V s at cryogenic temperatures.[26] Moreover, group 10 TMDs exhibit greater chemical stability compared to other high-mobility 2D semiconductors, such as black phosphorus and indium selenide (InSe).[27−29] Furthermore, electronic properties of some group 10 TMDs are predicted to change qualitatively with the layer number, which may open up novel applications in nanoelectronics and optoelectronics.[30] However, the experimentally observed two-terminal field-effect mobility of group 10 TMDs, which is pertinent to practical electronic device applications, is significantly lower, particularly in thinner samples. This discrepancy may be partially attributed to the presence of a non-negligible Schottky barrier (SB) at the drain and source contacts.[27,31]

In this article, we demonstrate that $PdSe_2/WSe_2$ nanosheet-based van der Waals heterostructures exhibit superior performance as channel materials for n-type field-effect transistors (FETs) compared to $PdSe_2$ or WSe_2 alone. In these heterostructures, the WSe_2 nanosheet functions both as a passivation layer, protecting the underlying $PdSe_2$ nanosheet from contamination and damage during fabrication, and as a buffer layer between $PdSe_2$ and Ti metal at the source and drain contacts, mitigating the Fermi-level pinning effect and

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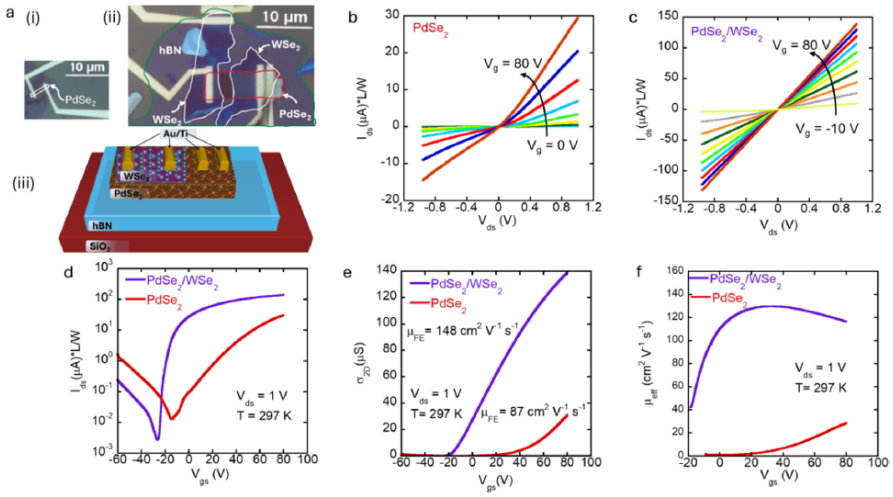

Figure 1. (a) Device structure of WSe_2 and $PdSe_2/WSe_2$ FETs. Optical micrograph of FETs consisting of (i) an ∼4.0 nm-thick $PdSe_2$ channel with a channel length L = 2.3 μm and channel width W = 0.4 μm, (ii) a $PdSe_2/WSe_2$ heterostructure channel of an ∼4.0 nm-thick $PdSe_2$ and an ∼2 nm-thick WSe_2 with a channel length L = 10.7 μm and channel width W = 5.8 μm, and (iii) schematic of the $PdSe_2$ and $PdSe_2/WSe_2$ devices. (b, c) Output characteristics of (b) the $PdSe_2$ and (c) the $PdSe_2$/ WSe_2 FET. (d) Transfer characteristics of the $PdSe_2$ and $PdSe_2/WSe_2$ FETs plotted on a semilog scale. (e) Two-terminal 2D conductivity of the $PdSe_2$ and $PdSe_2/WSe_2$ FETs as a function of gate voltage plotted on a linear scale. Field-effect mobility (μ_{FE}) is calculated from the average slope in the linear region of the 2D conductivity versus gate voltage curves. (f) Effective mobility of the $PdSe_2$ and $PdSe_2/WSe_2$ FETs as a function of gate voltage. All the data are taken at room temperature. The equivalent capacitance (C_{gs}) is 11.8 nF/cm^2 for both devices, based on the dielectric stack of 10 nm hBN and 280 nm SiO_2.

significantly reduces the Schottky barrier height (SBH) between Ti metal and $PdSe_2$.

As a result, our FETs based on $WSe_2/PdSe_2$ heterostructures, composed of a few-nanometer-thick $PdSe_2$ nanosheet and a bilayer or trilayer WSe_2, demonstrate high two-terminal effective electron mobility. Specifically, these devices achieve electron mobility values exceeding 200 cm^2 V^{-1} s^{-1} at room temperature and nearing 680 cm^2 V^{-1} s^{-1} at 77 K, consistent with phonon-limited electron transport mechanisms.

In contrast, FETs based solely on few-layer $PdSe_2$ (without the inclusion of WSe_2) exhibit substantially lower two-terminal effective mobility. Moreover, the electron mobility achieved in FETs based on $PdSe_2/WSe_2$ heterostructures significantly surpasses that of WSe_2 alone.[18,32,33] These findings suggest that electron transport in these $PdSe_2$ devices is primarily hindered by the Ti/$PdSe_2$ contacts, emphasizing the critical role of contact engineering, the importance of material selection, and the synergistic benefits of heterostructure and interfacial engineering in optimizing next-generation 2D electronic device performance.

Furthermore, the increase in bandgap with decreasing $PdSe_2$ thickness results in a higher on/off ratio for FETs based on $PdSe_2/WSe_2$ heterostructures with thinner $PdSe_2$ nanosheets. Specifically, our $PdSe_2/WSe_2$ heterostructure-based FET, comprising an ∼2 nm (∼3 layers) $PdSe_2$ nanosheet and a 2-to-3-layer WSe_2 nanosheet, achieves an impressive on/off ratio of ∼10^7 while simultaneously demonstrating significantly higher two-terminal electron mobility compared to FETs based solely on the constituent $PdSe_2$ or WSe_2.

2. EXPERIMENTAL SECTION

To fabricate $PdSe_2/WSe_2$ FETs, 10−30 nm-thick hBN flakes were first exfoliated on degenerately doped Si with 280 nm of thermal oxide by a mechanical exfoliation method. Next, trilayer to few-layer $PdSe_2$ and bilayer/trilayer WSe_2 nanosheets were also mechanically exfoliated on SiO_2/Si substrates and then sequentially picked up from SiO_2/Si substrates and placed on the hBN substrates by a dry transfer method using a polycarbonate (PC)/polydimethylsiloxane (PDMS) stamp on a glass microscope slide. Finally, metal electrodes, consisting of 10 nm Ti and 40 nm Au, were fabricated on top of the drain/source regions of the $PdSe_2/WSe_2$ heterostructure by electron beam lithography and electron beam-assisted metal deposition. For comparison, $PdSe_2$ FETs were also fabricated by dry transfer of mechanically exfoliated $PdSe_2$ onto hBN substrates, followed by e-beam lithography and metal deposition of 10 nm Ti and 40 nm Au.

Optical microscopy and Park-Systems XE-70 noncontact mode atomic microscopy (AFM) were used to identify and characterize thin $PdSe_2$ and WSe_2 flakes. Electrical properties of the devices were measured by a Keithley 4200 semiconductor parameter analyzer in a Lakeshore Cryogenic probe station under high vacuum (1×10^{-6} Torr).

3. RESULTS AND DISCUSSION

Figure 1a presents optical micrographs (panels i and ii) and a schematic (panel iii) of two FET devices, one with a $PdSe_2$ nanosheet as the channel material (panel i) and the other with a $PdSe_2/WSe_2$ nanosheet-based heterostructure as the channel material (panel ii). The $PdSe_2$ in both devices is approximately 4 nm thick, while the WSe_2 nanosheet in the $PdSe_2/WSe_2$ heterostructure is about 3 layers. To fabricate the FET devices, hBN flakes exfoliated onto degenerately doped Si with 280 nm of thermal oxide were used as ultraflat, smooth substrates to minimize dangling bonds and charge traps. Next, ultrathin WSe_2 nanosheets were stacked on top of the $PdSe_2$ nanosheets

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exfoliated onto Si wafers with 280 nm of SiO_2 using a dry transfer method to form the $PdSe_2/WSe_2$ heterostructure, which was then picked up and transferred onto the hBN substrates.[7,33,34] Finally, metal electrodes consisting of 10 nm Ti and 40 nm Au were fabricated on the drain/source regions of the $PdSe_2$ or $PdSe_2/WSe_2$ heterostructure devices using electron beam lithography followed by electron beam-assisted metal deposition.

To measure the electrical properties of the FET devices, back-gate biases were applied through the SiO_2/hBN dielectric stack to modulate the carrier density in the channel. To allow for a fair and quantitative comparison between devices with different channel widths and lengths, the currents plotted in Figure 1b−d are normalized by the respective channel dimensions. Figure 1b,c displays the output characteristics of the two devices shown in Figure 1a. The $PdSe_2/WSe_2$ device exhibits highly symmetric and linear $I-V$ characteristics (Figure 1c), whereas the $I-V$ curves of the $PdSe_2$ device, with nominally identical Ti/Au contacts (Figure 1b), are significantly more nonlinear and asymmetric. This suggests a more substantial SB in the $PdSe_2$ device compared to the $WSe_2/PdSe_2$ heterostructure.

Figure 1d shows semilogarithmic plots of the room-temperature transfer characteristics of the two FETs at a drain/source voltage of V_{ds} = 1 V. Both the on/off ratio and normalized on-current of the $PdSe_2/WSe_2$ device are significantly higher than those of the $PdSe_2$ device, which can be partially attributed to the enhanced on-current enabled by lower contact resistance.[33] Additionally, the subthreshold swing of the $PdSe_2/WSe_2$ device is much smaller (steeper) than that of the $PdSe_2$ device. However, the reduced switching steepness of the $PdSe_2$ device compared to the $PdSe_2/WSe_2$ device cannot be attributed to charge traps at the channel/gate-dielectric interface, as both devices are fabricated on the same hBN substrate and have nominally identical gate capacitance and gate-dielectric/channel (hBN/$PdSe_2$) interface.[35] This suggests that the difference is likely a contact effect, arising from thermally assisted tunneling through a SB at the Ti/$PdSe_2$ contacts.[36] In contrast, the near absence of such a thermally assisted tunneling region in the $PdSe_2/WSe_2$ device strongly suggests a significantly reduced SB height (SBH).

Figure 1e shows the linear plots of the two-terminal 2D conductivity (defined as $\sigma_{2D} = \frac{L}{W}\frac{I_{ds}}{V_{ds}}$, where L and W are the channel length and width, respectively) versus gate voltage to quantitatively compare the transfer characteristics of the two devices. While both devices exhibit n-type behavior, the threshold voltage of the $PdSe_2$ device is approximately 40 V higher (more positive) than that of the $PdSe_2/WSe_2$ device. This difference in threshold voltage suggests that the current in the $PdSe_2$ device is strongly suppressed by a substantial SB in the low-carrier-density region ($-20 < V_{gs} < 20$ V), in contrast to the $PdSe_2/WSe_2$ device. The region of suppressed drain current on the linear plot coincides with the broadened subthreshold region (thermally assisted tunneling region) on the semilog plot shown in Figure 1d, providing further evidence of a significant SBH at the Ti/$PdSe_2$ contacts. The WSe_2 layer between the Ti metal and $PdSe_2$ in the $PdSe_2/WSe_2$ device plays a key role in significantly reducing the SBH.

Interestingly, while the 2D conductivity of the $PdSe_2/WSe_2$ device is approximately four times higher than that of the $PdSe_2$ device at a back-gate voltage of 80 V, the field-effect mobility in the linear region of transfer characteristics for the former (148 $cm^2\ V^{-1}\ s^{-1}$) is less than twice that of the latter (87 $cm^2\ V^{-1}\ s^{-1}$). Here, the field-effect mobility is defined as

$$\mu_{FE} = \frac{1}{C_{gs}}\frac{d\sigma_{2D}}{dV_{gs}} \tag{1}$$

where C_{gs} is gate capacitance and σ_{2D} is the 2D conductivity. Here, C_{gs} is calculated as the equivalent series capacitance of the SiO_2/hBN dielectric stack, using the parallel-plate capacitor model and a dielectric constant of 3.5 for hBN.[33] The strong discrepancy between the differences in 2D conductivity and field-effect mobility of the two devices can also be attributed to the presence of a pronounced gate voltage-tunable SB at the contacts of the $PdSe_2$ device.[37] The drain current in the $PdSe_2$ device is significantly suppressed by a large SBH at low gate voltages (carrier densities). However, at higher V_{gs}, the current increases rapidly as the SB width is reduced by the gate voltage, resulting in an artificially enhanced slope in its transfer characteristics and, consequently, an overestimation of the two-terminal field-effect mobility.[38] Another potential artifact in extracting field-effect mobility may arise from the carrier density dependence of the intrinsic mobility (Drude mobility) of channel material. If the intrinsic mobility increases (or decreases) with carrier density, then the extracted field-effect mobility will contain an additional positive (or negative) term proportional to the first derivative of mobility with respect to gate voltage (or carrier density).[39] However, this is unlikely to contribute to the artificially enhanced field-effect mobility in our $PdSe_2$ devices, as their actual mobility slightly decreases with increasing carrier density (as discussed in detail below). On the contrary, this results in a small additional negative term in the extracted field-effect mobility at high gate voltages.

In addition to field-effect mobility, we also extracted the effective mobility of the two devices. According to the Drude model, the effective mobility is defined as the ratio of 2D conductivity to carrier density:

$$\mu_{eff} = \frac{\sigma_{2D}}{n} \tag{2}$$

Here, the carrier density is defined as

$$n = C_{gs}(V_{gs} - V_{th}) \tag{3}$$

where V_{th} is the threshold voltage. To accurately derive effective mobility, it is crucial to precisely determine the threshold voltage (V_{th}) corresponding to zero carrier density. In ideal transistors with low-resistance ohmic contacts, the effective mobility should match the actual mobility. However, the presence of a significant SB not only shifts the threshold voltage but also reduces the two-terminal 2D conductivity. As a result, effective mobility may deviate substantially from the actual channel mobility. Therefore, it is essential to extract and compare both field-effect and effective mobilities. In devices with low-resistance ohmic contacts and nearly carrier-density (gate voltage)-independent channel mobility, these values should be consistent. A discrepancy between the field-effect and effective mobility values from the same device indicates the presence of a non-negligible SB and/or carrier-density-dependent channel mobility.

The threshold voltage is influenced not only by the carrier density but also by the SBH at the source and drain contacts. In devices with ohmic contacts, the threshold voltage corresponds to the condition where the density of mobile

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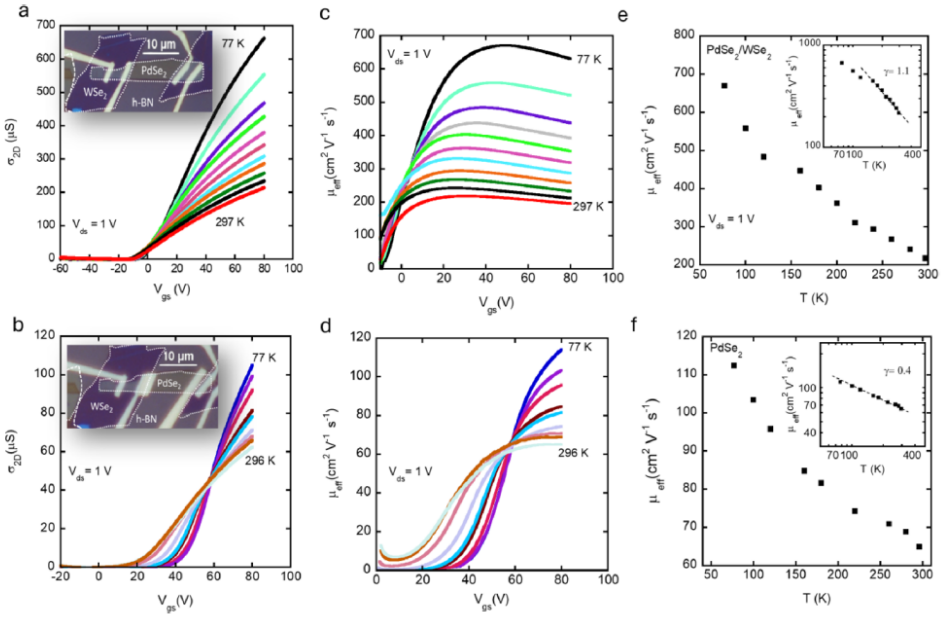

Figure 2. Temperature-dependent transfer characteristics and mobility comparison for two FETs with Au/Ti/WSe_2/$PdSe_2$ (a, c, and e) and Au/Ti/$PdSe_2$ contacts (b, d, and f). Both devices consist of an ∼6.7 nm-thick $PdSe_2$ in the channel, and the thickness of WSe_2 at the contacts is a trilayer. The channel length and width are L = 11.2 μm and W = 3.7 μm for the device in (a) and L = 7.8 μm and W = 3.7 μm for the device in (b). (a, b) 2D conductivity measured down to 77 K at V_{ds} = 1 V. The insets in (a) and (b) display optical micrographs of the respective devices. (c, d) Effective mobility defined as $\mu_{eff} = \sigma_{2D}/C_{gs}(V_{gs} - V_{th})$. (e, f) Temperature dependence of the peak and maximum effective mobility (μ_{eff}) of the two devices in (c) and (d). The insets in (e) and (f) show the corresponding log−log plots. The equivalent capacitance (C_{gs}) is 11.8 nF/cm^2 for both devices, based on the dielectric stack of 12 nm hBN and 280 nm SiO_2.

carriers is zero. However, the presence of a substantial SBH can significantly shift the threshold voltage. Given that a much larger SBH is likely present in the $PdSe_2$ device than in the $PdSe_2$/WSe_2 device, as indicated by the substantial positive threshold voltage shift in the former, we used the threshold voltage of the $PdSe_2$/WSe_2 device to estimate the electron density for both devices. Since both devices are based on 4 nm-thick $PdSe_2$ nanosheets exfoliated from the same $PdSe_2$ crystal and fabricated on the same SiO_2/hBN dielectric stack, we expected them to exhibit nearly identical carrier densities at a given gate voltage. This approach helps avoid underestimating the electron density in the $PdSe_2$ device due to the threshold shift.

As shown in Figure 1f, the effective mobility of the $PdSe_2$/WSe_2 device closely matches its field-effect mobility, suggesting that the device performance is primarily governed by the channel rather than contact effects. In contrast, the effective mobility of the $PdSe_2$ device is several times lower than its field-effect mobility. This discrepancy indicates the presence of a gate-tunable, non-negligible SB in the $PdSe_2$ device. The rapid increase in drain current as the SB thickness decreases with gate voltage results in an artificially enhanced slope of the transfer characteristics. The effective mobilities of both $PdSe_2$ and $PdSe_2$/WSe_2 devices also exhibit qualitatively different gate dependencies. While the effective mobility of the $PdSe_2$ device increases monotonically with gate voltage, reaching ∼35 cm^2 V^{-1} s^{-1} at ∼80 V, the effective mobility of the $PdSe_2$/WSe_2 device initially rises quickly with gate voltage and then slightly decreases after reaching a maximum value of ∼130 cm^2 V^{-1} s^{-1} at ∼30 V. The monotonic increase in effective mobility in the $PdSe_2$ device can be attributed to the thinning of the SB as the gate voltage becomes more positive. In contrast, the slight decrease in effective mobility with gate voltage in the $PdSe_2$/WSe_2 device cannot be explained by SB tuning. We attribute this decrease to increased channel/dielectric interfacial scattering, as electrons are pulled closer to the channel/dielectric interface by the increasingly positive gate voltage. This interface scattering is likely caused by impurities introduced during the fabrication process, as the devices were fabricated in ambient conditions. We anticipate that fabricating the devices in an inert environment, such as a glovebox, will yield a cleaner channel/dielectric interface and reduce interfacial scattering, an effect that may be explored in future studies. In particular, $PdSe_2$/WSe_2 devices fabricated under inert conditions are expected to exhibit higher mobility and a weaker carrier density dependence of mobility, owing to suppressed interface scattering resulting from a substantial reduction in impurities at the channel/dielectric interface.

Notably, a crack in the WSe_2 layer results in incomplete coverage of the channel region in the $PdSe_2$/WSe_2 device shown in Figure 1. Consequently, the drain-source current flows primarily through the $PdSe_2$ layer in the $PdSe_2$/WSe_2 device depicted in Figure 1a. Similar behavior, both qualitatively and quantitatively, is observed in $PdSe_2$/WSe_2 devices where the WSe_2 layer fully covers the channel as well as the drain and source regions (see Figure S1 in the Supporting Information). This observation suggests that $PdSe_2$ serves as the active current-carrying layer in $PdSe_2$/WSe_2 heterostructure devices. To confirm that the current contribution from the WSe_2 layer is negligible in these heterostructures, we measured

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the transfer characteristics of a WSe_2 FET fabricated from the same piece of WSe_2 used to form the $PdSe_2/WSe_2$ heterostructure in Figure S1. The electron current in the WSe_2-only device is approximately 5 orders of magnitude smaller than that in the $PdSe_2/WSe_2$ heterostructure device (see Figure S2 in the Supporting Information), indicating that the current flow in the WSe_2 layer is negligible and that the primary role of the WSe_2 layer is to reduce the SBH and contact resistance in $PdSe_2/WSe_2$ devices. Using a $PdSe_2/WSe_2$ heterostructure as the channel material instead of $PdSe_2$ significantly reduces the SBH at the drain/source contacts, leading to improved device performance.

To eliminate possible alternative current pathways—for instance, lateral carrier transport within the WSe_2 layer followed by injection into $PdSe_2$ in the gap regions—and to further evaluate the influence of the WSe_2 layer on the electrical characteristics of $PdSe_2/WSe_2$ FETs, we measured the temperature-dependent transfer characteristics of two FETs sharing the same channel material, differing primarily in that one employed $PdSe_2/WSe_2$ and the other $PdSe_2$ in the drain and source regions. In one, Ti metal is in direct contact with $PdSe_2$, while in the other, Ti metal contacts a $PdSe_2/WSe_2$ heterostructure in the drain and source regions. To fabricate the devices, a trilayer WSe_2 with a gap in between was dry-transferred onto a few-layer $PdSe_2$, creating a structure where the drain and source regions consist of a $PdSe_2/WSe_2$ heterostructure, while the channel is composed solely of $PdSe_2$ (inset of Figure 2a). To ensure that the effective channel width and length are chiefly determined by the geometry of the $PdSe_2$ nanosheet and to exclude the possibility of lateral carrier transport within the WSe_2 layer prior to entering the $PdSe_2$ channel, we fabricated metal contacts positioned near the inner edges of the gap in the WSe_2 layer. This device configuration ensures that the active channel consists predominantly of $PdSe_2$, while WSe_2 functions solely as a buffer layer in the contact regions. After completing all measurements, we fabricated a second device by extending the metal electrodes slightly into the $PdSe_2$ channel region using additional e-beam lithography and e-beam deposition of Ti and Au, thereby creating direct $Ti/PdSe_2$ contacts in the drain and source regions (inset of Figure 2b). The channel length of the $PdSe_2$ device is slightly shorter than that of the $PdSe_2/WSe_2$ device. Figure 2a,b shows the transfer characteristics of these two devices measured at different temperatures, down to 77 K. Since both devices share essentially the same $PdSe_2$ channel, any variations in doping or gating effects within the channel material can be disregarded.

As the electron concentration increases, the device with only $PdSe_2$ at drain and source contacts appears to exhibit a transition from an insulating regime for $V_{gs} < \sim 60$ V, where the current increases with temperature, to a metallic regime for $V_{gs} > \sim 60$ V, where the current decreases with temperature as shown in Figure 2b.[40] In contrast, the device with $PdSe_2/WSe_2$ at drain and source contacts exhibits a vanishingly small insulating regime as shown in Figure 2a. Because the two devices essentially share the same $PdSe_2$ nanosheet in the channel region, except that the $PdSe_2$ device has a slightly shorter channel due to inward electrode extensions, the observed differences in the temperature-dependent transfer characteristics can be primarily attributed to the stronger suppression of drain current by a larger SBH at the $Ti/PdSe_2$ contacts, especially at lower carrier concentrations. As the temperature decreases, the thermionic and thermally assisted current over the SB of the device with $Ti/PdSe_2$ contacts becomes increasingly suppressed, especially at relatively low carrier concentrations. Consequently, a higher gate voltage is required to turn on the device at lower temperatures, as the larger SBH at the drain and source contacts shifts the threshold voltage increasingly positively. Therefore, the observed crossover from an apparently insulating regime at low gate voltages to an apparently metallic regime at high gate voltages in the device shown in Figure 2b is most likely a contact effect rather than a true metal−insulator transition of the channel.[41]

On the other hand, the threshold voltage of the device with a $PdSe_2/WSe_2$ heterostructure in the drain and source regions is nearly temperature-independent, indicating a negligibly small SBH that does not limit current flow in the on state of the device (Figure 2a). The smaller SBH also results in higher 2D conductivity with a more pronounced temperature dependence, consistent with phonon-scattering-limited electron transport in the channel. Notably, the $PdSe_2$ device exhibits a significant positive shift in threshold voltage compared to the $PdSe_2/WSe_2$ device, indicating that the SB plays a significant role in modulating the threshold voltage.

Next, we compare the effective mobility of the two devices as a function of gate voltage at different temperatures. Figure 2c shows that the effective mobility of the device with $PdSe_2/WSe_2$ at drain and source contacts first rapidly increases to a maximum value with gate voltage and then gradually decreases as the gate voltage further increases. On the other hand, the effective mobility in the device with $PdSe_2$ at drain and source contacts keeps increasing with gate voltage until $V_{gs} = 80$ V as shown in Figure 2d. This qualitative difference between the gate dependences of the effective mobilities of the two devices suggests that the intrinsic channel mobility may slightly decrease at higher gate voltages (due to increased scattering at the dielectric/channel interface) and that the monotonous increase in the effective mobility in the device with $Ti/PdSe_2$ contacts as shown in Figure 2d is likely an artifact caused by the gate modulation of a substantial SB at the contacts.

Another key difference between the two devices lies in the temperature dependence of their effective mobility. For the device with $PdSe_2$ at drain and source contacts, the effective mobility increases with temperature at gate voltages below ∼60 V but decreases with temperature at higher gate voltages. In contrast, the device with $PdSe_2/WSe_2$ at drain and source contacts exhibits a monotonic decrease in effective mobility with temperature across the entire on-state gate voltage range. The increase in effective mobility with temperature at lower gate voltages in the $PdSe_2$ device in Figure 2d suggests that its two-terminal mobility is limited by the SB, which is nearly negligible in the $PdSe_2/WSe_2$ device in Figure 2c. Furthermore, at 77 K, the peak effective mobility of the $PdSe_2/WSe_2$ device inFigure 2c reaches ∼680 $cm^2 V^{-1} s^{-1}$, which is more than five times higher than the maximum effective mobility of the $PdSe_2$ device in Figure 2d (∼115 $cm^2 V^{-1} s^{-1}$ at $V_{gs} = 80$ V), further underscoring the influence of the SBH on two-terminal effective mobility.

The temperature dependence of the peak (maximum) two-terminal effective mobility for both devices is shown in Figure 2e,f. In the device with $PdSe_2/WSe_2$ at drain and source contacts, the peak effective mobility increases from ∼200 $cm^2 V^{-1} s^{-1}$ at room temperature to ∼680 $cm^2 V^{-1} s^{-1}$ at 77 K, following a $\mu \sim T^{-1.1}$ dependence in the temperature range between 160 K and room temperature. The maximum two-terminal effective mobility of the device with $PdSe_2$ at drain

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and source contacts is significantly lower and exhibits a much weaker temperature dependence, following $\mu \sim T^{-0.4}$. The stronger temperature dependence of two-terminal effective mobility of the former suggests that phonon scattering in the channel is the dominant limiting factor. By contrast, the lower two-terminal effective mobility and weaker temperature dependence of the latter can be attributed to a relatively large SBH, which increasingly limits current flow as temperature decreases.

Next, we quantitatively compare the SBH of the FET devices consisting of $PdSe_2$ and $PdSe_2/WSe_2$ at the drain-source regions shown in Figure 2. The FETs are modeled as two back-to-back Schottky diodes connected by a $PdSe_2$ channel. Our SBH extraction method is based on the thermionic emission current through a reverse-bias Schottky diode at the flat-band voltage.[42] The thermionic emission current density is given by

$$I_{ds} = A^*_{2D} T^{3/2} e^{(-q\Phi_B/k_B T)}[1 - e^{(-qV/k_B T)}] \quad (4)$$

where A^*_{2D} is the 2D equivalent of Richardson's constant, T is the temperature, q is the electron charge, V is the applied voltage at the junction, and Φ_B is the effective barrier height.[43] To extract the SBH, the drain voltage is biased such that $|qV| \gg k_B T$, which makes the term in brackets in eq 4 approximately 1 for the reverse-bias Schottky contact. Rearranging eq 4 and taking the natural log of $I_{ds}/T^{3/2}$ yields

$$\ln\left(\frac{I_{ds}}{T^{3/2}}\right) = \ln(A^*_{2D}) - \Phi_B\left(\frac{q}{k_B T}\right) \quad (5)$$

From eq 5, the slope of $\ln\left(\frac{I_{ds}}{T^{3/2}}\right)$ vs $1/T$ is proportional to Φ_B for a given gate voltage. Since the gate voltage effectively tunes the charge doping at the contacts, thermally assisted tunneling and tunneling current through the SB may become significant at high positive gate voltages (i.e., higher carrier densities) for an electron SB. In this regime, the extracted Φ_B based on the themionic emission model is expected to be smaller than the actual SBH. Conversely, as the gate voltage becomes increasingly negative, the channel barrier height rises, leading to a higher extracted Φ_B. Consequently, a transition in slope occurs at the flat-band voltage, reflecting a change in the transport mechanism across the SB. At the flat-band voltage, the extracted Φ_B approaches the actual SBH.

Figure 3a,c shows Arrhenius plots for FETs with $PdSe_2$ and $PdSe_2/WSe_2$ at the contact regions as shown in Figure 2. In the $PdSe_2$ device, the Arrhenius plots exhibit negative slopes across the entire temperature range (Figure 3a). In contrast, for the $PdSe_2/WSe_2$ device, the slopes are negative at temperatures below 140 K but become positive at higher temperatures (Figure 3c).

The observed positive slopes in Figure 3c cannot be explained by thermionic emission or thermally assisted tunneling over an SB and is likely limited by the phonon scattering in the channel, which is consistent with larger 2D conductivity, higher two-terminal effective mobility, and more pronounced temperature dependence of two-terminal effective mobility observed in $PdSe_2/WSe_2$ devices. When the total resistance of an FET device is dominated by the channel instead of contacts, its current decreases with temperature due to increased phonon scattering at higher temperatures giving rise to a positive slope of the Arrhenius plots. As the temperature decreases, the reduction of channel resistance

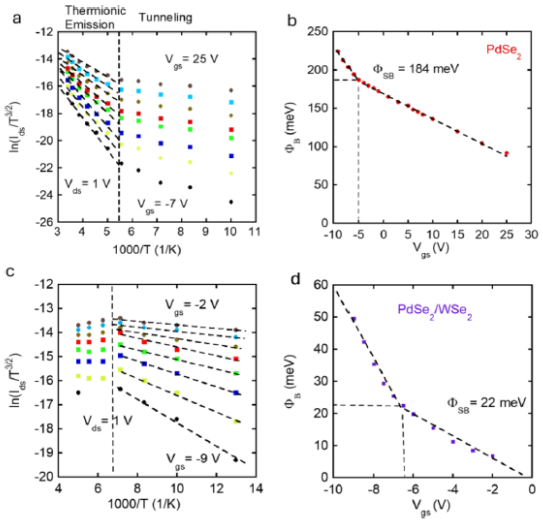

Figure 3. Flat-band Schottky barrier height extraction. (a, c) Arrhenius plots of (a) $PdSe_2$ and (c) $WSe_2/PdSe_2$ FETs contacted by Ti/Au metal for various gate voltages. (b, d) Extracted n-type effective barrier height at various gate voltages, where the flat-band SBH is measured to be (b) 184 meV and (d) 22 meV in the $PdSe_2$ and $WSe_2/PdSe_2$ FETs, respectively.

causes contact resistance to dominate, resulting in activation behavior with negative slopes. Therefore, we extracted the Φ_B of the $PdSe_2/WSe_2$ device from the temperature region below 140 K. By contrast, the current of the $PdSe_2$ device is contact-limited in the entire temperature region as signified by negative slopes of the Arrhenius plots (Figure 3a). The absolute value of the slope for the $PdSe_2$ device decreases below 180 K, which corresponds to a transition from thermionic emission at higher temperatures to tunneling and/or thermally assisted tunneling at lower temperatures. Therefore, we extracted the Φ_B of the $PdSe_2$ from the temperature region above 180 K.

Figure 3b,d shows the extracted Φ_B as a function of gate voltage for the $PdSe_2$ and $PdSe_2/WSe_2$ devices. The SBH is defined as Φ_B at the flat-band voltage. For gate voltages above (i.e., more positive than) the flat-band voltage, thermally assisted tunneling current across the SB becomes significant, weakening the dependence of the extracted Φ_B on the gate voltage. Using this technique, SBHs of 184 and 22 meV are determined for $PdSe_2$ and $PdSe_2/WSe_2$ devices at the point where the slope changes in Figure 3b,d. Consistently larger SBH values were obtained in $PdSe_2$ devices than in $PdSe_2/WSe_2$ devices (see Figure S3 of the Supporting Information). The drain/source contacts of our $PdSe_2/WSe_2$ devices can be modeled as metal−semiconductor−semiconductor (MSS) or metal−insulator−semiconductor (MIS) contacts. Several different mechanisms have been proposed to explain the reduction of SBH in MIS contacts including attenuation of metal-induced gap states (MIGS), formation of electronic dipole at the insulator−semiconductor interface, passivation of interfacial defects, and interfacial doping.[44−48] Alternatively, the drastic reduction of SBH in our $PdSe_2/WSe_2$ devices can be attributed to the synergy of Fermi-level pinning to WSe_2 and the favorable conduction-band offset between the WSe_2 and $PdSe_2$ layers.[38] Among these possible mechanisms, the

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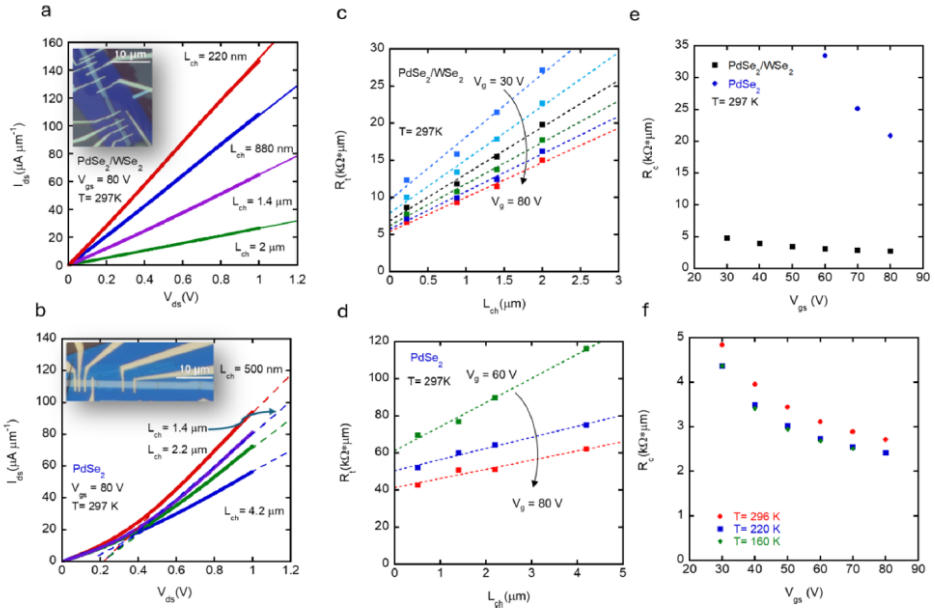

Figure 4. Contact resistance of $WSe_2/PdSe_2$ and $PdSe_2$ FETs with Ti/Au metal contacts. (a, b) Room-temperature $I_{ds}-V_{ds}$ output curves for different channel lengths at V_{gs} = 80 V for (a) $WSe_2/PdSe_2$ and (b) $PdSe_2$ FETs. The thicknesses of $PdSe_2$ in the $WSe_2/PdSe_2$ and $PdSe_2$ devices are 8.1 and 9.0 nm, respectively. (c, d) Total resistance normalized by width (R_t) as a function of channel length for each type determined by the slopes from (a, b) at different gate voltages for the (c) $WSe_2/PdSe_2$ and (d) $PdSe_2$ FETs. The *y*-intercept yields twice the contact resistance ($2R_C$). (e) Comparison of extracted contact resistance for the $WSe_2/PdSe_2$ and $PdSe_2$ devices as a function of carrier density (gate voltage bias). (f) Contact resistance of the $WSe_2/PdSe_2$ devices as a function of carrier density measured at different temperatures. The equivalent capacitance is 11.0 nF/cm^2 for both devices, based on the dielectric stack of 30 nm hBN and 280 nm SiO_2.

synergistic effect of Fermi-level pinning to WSe_2 and the favorable conduction-band offset between the WSe_2 and $PdSe_2$ layers appears to be most consistent with the present data. Other mechanisms, such as the formation of an interfacial dipole or interfacial doping, are less likely since the threshold voltages of devices with WSe_2 only at the drain and source contacts are comparable to those of devices in which WSe_2 fully covers the $PdSe_2$ channel. Furthermore, Fermi-level pinning is commonly observed between deposited metals such as Ti and TMDs like WSe_2. The relatively low electron affinity of WSe_2 compared to $PdSe_2$ favors a band alignment that reduces the SBH between the Ti contact and $PdSe_2$, as schematically illustrated in the band alignment diagrams (see Figure S3 of the Supporting Information). However, it is beyond the scope of this work to pinpoint the exact mechanism behind the significantly reduced SBH in our $PdSe_2/WSe_2$ devices, as the main goal of this study is to demonstrate the superior performance of $PdSe_2/WSe_2$ compared to $PdSe_2$ and WSe_2 as a channel material in n-type FETs. Future experiments that systematically investigate devices based on heterostructures composed of $PdSe_2$ and various TMD nanosheets with different band alignments, as well as contact metals with different work functions, may help elucidate the underlying mechanism.

To quantify the impact of reduced SBH on contact resistance, the transfer length method (TLM) was used to extract the contact resistance of FET devices with $PdSe_2/WSe_2$ and $PdSe_2$ channels. Figure 4a,b shows the output characteristics of the $PdSe_2/WSe_2$ and $PdSe_2$ devices for different channel lengths at V_{gs} = 80 V. Optical micrographs of the devices used for TLM measurements are shown in the insets of Figure 4a,b. Because the electron current in the WSe_2 layer is approximately 5 orders of magnitude lower than that in the $PdSe_2$ layer (see Figure S2 in the Supporting Information), the channel length and width of the $PdSe_2/WSe_2$ device are effectively defined by the geometry of the $PdSe_2$ nanosheet, where electron transport predominantly occurs. The slight super linear behavior observed in the output characteristics of the $PdSe_2$ device can be attributed to the substantial SBH at the drain and source contacts. Figure 4c,d shows the total resistance normalized by width (R_t) for the $PdSe_2/WSe_2$ and $PdSe_2$ devices, which was derived from the slope of the $I-V$ characteristics in Figure 4a,b and plotted as a function of channel length at various gate voltages. The reasonably good linear fit to the data across different gate voltages suggests minimal variability among the contacts and channels in each device. Since all devices with different channel lengths exhibit nearly identical threshold voltages in each TLM structure (see Figure S6 of the Supporting Information), they are expected to have the same carrier density at a given gate voltage. The *y*-intercept of the linear fit yields the total contact resistance $2R_C$. It is important to ensure that the total resistance of the device with the shortest channel is not significantly larger than $2R_C$ in order to minimize errors in contact resistance extraction.[49,50] As shown in Figure 4c,d, the total resistance of the shortest channel device is dominated by the total contact resistance, suggesting that the error in the extracted contact resistance is relatively small. The TLM measurements at V_{gs} = 80 V yield a contact resistance of 2.8 kΩ μm for $PdSe_2/WSe_2$ and 20 kΩ μm for $PdSe_2$ per contact, which is qualitatively consistent with

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the corresponding disparities in their SBH. The difference in the contact resistance between $PdSe_2/WSe_2$ and $PdSe_2$ increases as the electron concentration (gate bias voltage) decreases, as shown in Figure 4e. This trend is expected due to their SBH difference: the larger SBH at the contacts of $PdSe_2$ leads to progressively higher contact resistance at lower carrier densities. In contrast, the contact resistance in $WSe_2/PdSe_2$ devices is significantly less sensitive to the carrier density, owing to the substantially smaller SBH at the contacts. In addition, the relatively small SBH at the contacts in $PdSe_2/WSe_2$ devices results in a relatively weak temperature dependence of the contact resistance, as shown in Figure 4f. The TLM structure comprising FETs with different channel lengths also enables extraction of the intrinsic channel mobility, independent of contact resistance. A channel mobility of 195 $cm^2 V^{-1} s^{-1}$ is obtained from the inverse of the slope in Figure 4c as a function of gate voltage (see Figure S7 in the Supporting Information). This value is consistent with the two-terminal mobility observed in similar devices in this study, confirming that carrier transport in $PdSe_2/WSe_2$ devices is limited primarily by the channel rather than by the contacts. We anticipate that further improvements in $PdSe_2$ material quality and fabrication processes—such as device assembly in an inert glovebox environment—will yield even higher two-terminal mobilities.

To further emphasize the advantages of the $PdSe_2/WSe_2$ heterostructure over pure $PdSe_2$ as a channel material in FET performance, we systematically investigated multiple $PdSe_2$ and $PdSe_2/WSe_2$ devices with varying $PdSe_2$ thicknesses. These devices were fabricated using $PdSe_2$ nanosheets of different thicknesses combined with bilayer or trilayer WSe_2 nanosheets to form the $PdSe_2/WSe_2$ heterostructures. Because the WSe_2 buffer layer also functions as a tunneling barrier for carrier injection, the current transmitted through it decreases exponentially with both the tunneling barrier thickness and the square root of the barrier height.[51] To minimize contact resistance and improve device performance, it is therefore essential to minimize both the barrier height and thickness. However, the WSe_2 layer must also be sufficiently thick to suppress Fermi-level pinning between the metal contact and the $PdSe_2$ active layer. A monolayer WSe_2 is often too thin to effectively decouple the metal–$PdSe_2$ interactions and, in addition, exhibits a lower electron affinity than its bilayer or trilayer counterparts, resulting in a higher tunneling barrier height. Consequently, bilayer or trilayer WSe_2 nanosheets were selected as the buffer layer to construct the $PdSe_2/WSe_2$ heterostructures. Figure 5 summarizes the room-temperature on/off ratio and two-terminal effective mobility as a function of $PdSe_2$ thickness in these devices. As the $PdSe_2$ thickness decreases, the on/off ratios of both $PdSe_2$ and $PdSe_2/WSe_2$ devices increase, which is expected due to the corresponding increase in the $PdSe_2$ bandgap.[27,31,52] However, as shown in Figure 5a, the on/off ratio in $PdSe_2/WSe_2$ devices is consistently higher and increases more rapidly with decreasing $PdSe_2$ thickness compared to $PdSe_2$ devices. As the thickness of $PdSe_2$ decreases to approximately 2 nm, the $PdSe_2/WSe_2$ device achieves a high on/off ratio of 10^7, which is about 2 orders of magnitude higher than that of the $PdSe_2$ device fabricated from the same ~2 nm-thick $PdSe_2$, but without WSe_2 (see Figure S4 of the Supporting Information). In addition, the two-terminal effective mobility of the $PdSe_2/WSe_2$ devices is consistently higher than that of the $PdSe_2$ devices across all $PdSe_2$ thicknesses as shown in Figure 5b. The

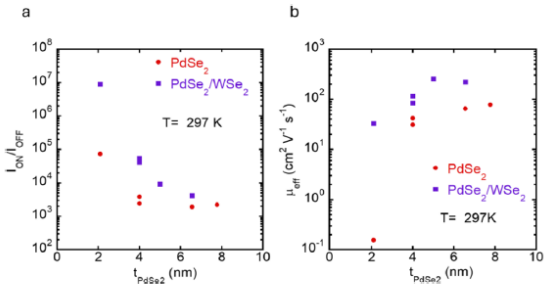

Figure 5. (a) On/off ratios of the $PdSe_2/WSe_2$ and $PdSe_2$ FETs as a function of $PdSe_2$ thickness. (b) Effective mobility of $PdSe_2/WSe_2$ and $PdSe_2$ FETs with varying $PdSe_2$ thicknesses. The thickness of WSe_2 in $PdSe_2/WSe_2$ FETs is 2–3 layers.

mobility of our $PdSe_2/WSe_2$ device, incorporating an ~2 nm-thick (~3 layers) $PdSe_2$, is 2 orders of magnitude higher than that of the $PdSe_2$ device without WSe_2 (see Figure S5 of the Supporting Information) and nearly an order of a magnitude higher than that of a trilayer $PdSe_2$ FET reported in the literature.[53] A high two-terminal effective mobility of ~250 $cm^2 V^{-1} s^{-1}$, along with an on/off ratio approaching 4 orders of magnitude, is concurrently observed in a $PdSe_2/WSe_2$ heterostructure FET consisting of an ~5 nm-thick $PdSe_2$. These results are consistent with the lower SBH and, consequently, the reduced contact resistance in the $PdSe_2/WSe_2$ devices.

The $PdSe_2/WSe_2$ devices developed in this work exhibit two-terminal mobility values substantially higher than the average field-effect mobility reported for $PdSe_2$ FETs and are comparable to or even exceed the maximum mobilities achieved in optimized $PdSe_2$ devices (see Table S6 in the Supporting Information for details).[27,31,53] Moreover, the on/off current ratios of the $PdSe_2/WSe_2$ heterostructure FETs reach 10^4–10^7, surpassing those of previously reported $PdSe_2$ devices, which typically exhibit much lower ratios ($\approx 10^2$–10^3). It is worth noting that most literature reports only field-effect mobilities, which can be significantly overestimated due to gate-induced modulation of the SB and thus may not accurately reflect the intrinsic device performance. In our $PdSe_2$ devices with Ti/Au contacts, a clear discrepancy is observed between μ_{FE} and the effective mobility (μ_{eff}), with μ_{FE} being substantially higher. In contrast, the $PdSe_2/WSe_2$ heterostructures exhibit close agreement between μ_{FE} and μ_{eff}, together with markedly higher overall mobility values than the $PdSe_2$-only devices. This consistency indicates that the high two-terminal mobility observed in $PdSe_2/WSe_2$ FETs is reliably achieved. Furthermore, the contact resistance of $PdSe_2/WSe_2$ devices is among the lowest reported for $PdSe_2$-based FETs, highlighting efficient charge injection across the $PdSe_2/WSe_2$ heterostructure relative to bare $PdSe_2$.

Stacking two different 2D semiconductors as the channel material of FETs is a simple yet effective approach to enhancing device performance. This technique significantly reduces contact resistance by reducing SBH at the metal–semiconductor interface, leading to improved device performance. Moreover, this method is broadly applicable to a wide range of 2D semiconductors and their heterostructures, where the top layer acts as a buffer that modifies the energy alignment between the metal Fermi level and the conduction (or valence) band edge of the active layer. As a result, the electron (or hole)

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SBH can be reduced for n-type (or p-type) transistors. Additionally, the top 2D semiconductor layer acts as a protective barrier, enhancing the chemical and environmental stability of the active bottom layer while shielding it from damage or contamination during the fabrication process. Compared to other interface engineering techniques, this method offers a straightforward and practical way to achieve superior electrical performance and reliability in next-generation nanoelectronic devices.

4. CONCLUSIONS

In conclusion, we report the fabrication of high-performance n-type FETs by using a $PdSe_2/WSe_2$ nanosheet-based heterostructure as a channel material to overcome the high SBH at the metal/$PdSe_2$ contacts and the relatively low intrinsic electron mobility of WSe_2. The addition of a bilayer or trilayer WSe_2 nanosheet to a few-layer $PdSe_2$ nanosheet significantly lowers the SBH at the contacts and contact resistance. The improvement in drain/source contacts leads to enhanced device performance including higher on-current, higher on/off ratio, and enhanced two-terminal mobility. This contact engineering strategy of using the $PdSe_2/WSe_2$ nanosheet-based heterostructure in place of the individual $PdSe_2$ or WSe_2 nanosheet is air-stable and thermally stable and compatible with conventional semiconductor processes. It may be implemented in the production of flexible electronics by incorporating large-scale $PdSe_2/WSe_2$ nanosheet-based heterostructures.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsanm.5c04263.

Electrical properties of additional $PdSe_2/WSe_2$ heterostructure, $PdSe_2$, and WSe_2 devices; methods used to extract the effective capacitance of the SiO_2/hBN dielectric stack; comparison of $PdSe_2/WSe_2$ FETs with $PdSe_2$ devices reported in the literature (PDF)

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Notes

The authors declare no competing financial interest.

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